令　和　四　年　度　　修　士　論　文

Analysis and Application of Dual RESURF 40 V N-LDMOS with Grounded Field Plate

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ABSTRACT OF THE THESIS

We proposed a 0.18 μm CMOS compatible dual RESURF 40 V N-LDMOS transistor with a grounded field plate for automotive applications, which showed a wide SOA, high hot carrier endurance, and low specific on-resistance, and low switching loss. The LDMOS transistor that we proposed to reduce the switching loss for buck type and boost type DC-DC converters used in automotive applications.

We have analyzed the switching characteristics of the proposed device in detail by changing the load resistance R_L and the gate resistance R_G. The field plate of the proposed device connects to the ground, which significantly makes the Miller capacitance smaller, causing much lower switching loss. We have also optimized the length of the field plate L_{FP} and the oxide thickness between the field plate and the drift region T_{OX1} to obtain the breakdown voltage (BV_{DS}) between the drain and the source of more than 60V with keeping low switching loss by simulation.

We have verified the feasibility of the actual conditions in the TCAD simulation software to clarify the scope for mass production of LDMOS in practice.

Keywords: LDMOS, RESURF, switching loss, grounded field plate, DC-DC converter

Chapter 1: Introduction

1.1 Research background

LDMOS (See Fig.1) stands for laterally-diffused metal-oxide semiconductor. LDMOS is a planar double-diffused MOSFET (metal–oxide–semiconductor field-effect transistor); LDMOS is one type of double-diffused MOSFET (DMOS), which was reported in the 1960s and is made using a double diffusion process. LDMOS was reported in 1969 by Tarui et al. of the Electrotechnical Laboratory (ETL).

LDMOS for RF applications was proposed in the early 1970s by Cauge et. al. In the early 1990s, Radio Frequency (RF) LDMOS eventually displaced RF bipolar transistors as RF power amplifiers for cellular network infrastructure because RF LDMOS provides superior linearity, efficiency, and gain along with lower costs. With the introduction of the 2G digital mobile network, LDMOS became the most widely used RF power amplifier technology in 2G and 3G mobile networks. By the late 1990s, the RF LDMOS had become the dominant RF power amplifier technology in markets such as cellular base stations, broadcasting, radar, and Industrial, Scientific, and Medical (IMS) band applications; LDMOS has enabled most of the world's cellular voice and data traffic.

In the mid-2000s, RF power amplifiers based on single LDMOS devices suffered from relatively low efficiency when used in 3G and 4G (LTE) networks due to the higher peak-to-average power of the modulation schemes and CDMA and OFDMA access techniques used in these communication systems. In 2006, the efficiency of LDMOS power amplifiers was boosted using typical efficiencies enhancement techniques, such as Doherty topologies and envelope tracking.

As of 2011, RF LDMOS is the dominant device technology used in high-power RF power amplifier applications for frequencies ranging from 1 MHz to over 3.5 GHz and also it is the dominant RF power device technology for cellular infrastructure. As of 2012, RF LDMOS is the leading technology for a wide range of RF power applications. As of 2018, LDMOS is the de facto standard device technology for power amplifiers in mobile networks such as 4G and 5G.

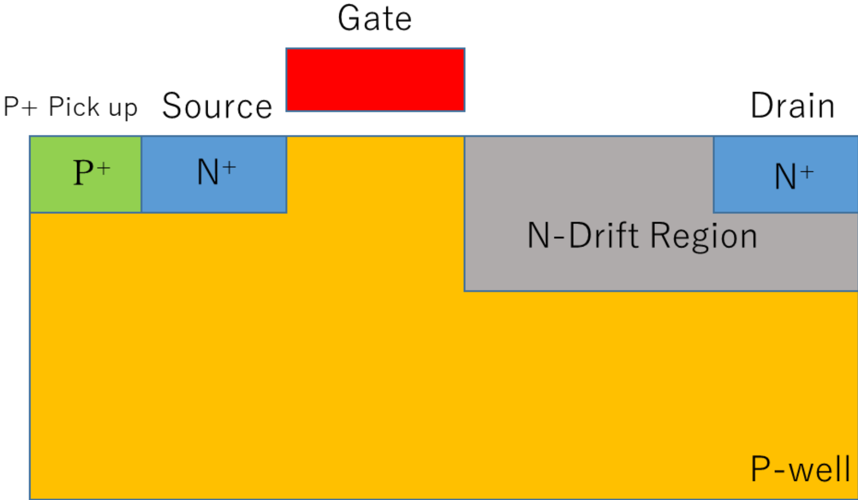

Fig.1 Cross-sectional device structure of N-ch LDMOS

1.2 Research Objective

LDMOS is not only used in RF applications but also widely used in the automotive industry, industry, radar, and other fields. In this paper, we focus on the characteristics of LDMOS for the application of DC-DC converters in the automotive industry.

DC power supply applications always require smaller volume of DC-DC converters with low power dissipation by using smaller-sized passive devices. In this case, we need to operate DC-DC converters at a high switching frequency under Pulse Width Modulation (PWM) control, resulting in high switching loss. Therefore, we proposed a 40 V operation N-channel LDMOS transistor with a grounded field plate as an integrated switching device to reduce the switching loss even at a high switching frequency for buck type and boost type DC-DC converters used in automotive applications. This device also has a dual Reduced Surface Field (RESURF) structure [1], yielding to low on-resistance and high breakdown voltage [2] between the drain and the source, and high hot carrier endurance [3], whose characteristics are suitable especially for automotive applications.

So in this paper, based on the conventional LDMOS field plate connected to the gate, we propose an LDMOS that the field plate is connected to the ground. The proposed device has a wide Safe Operating Area (SOA) [4] and high hot carrier endurance thanks to the dual RESURF structure and the field plate. In addition, compared with a conventional LDMOS transistor whose field plate connects to the gate, the proposed device shows a much lower (superior) figure of merit (FOM) of switching loss, Ron,sp × QG (specific on-resistance times gate charge), mainly due to a much lower Miller effect [5] caused by the grounded field plate. Since it needs to investigate under many conditions by considering actual use cases, a detailed evaluation of the switching loss is required. We also optimize the grounded field plate and investigate the process feasibility of the grounded field plate from the viewpoint of mass production.

1.3 Reduced Surface Field (RESURF)

Appels and Vaes proposed the first RESURF concept in 1979 [1]; the frequently used method to design high voltage devices on thin epitaxial layer with low on-resistance is the RESURF. The RESURF concept gives the best trade-off between the breakdown voltage and the on-resistance of lateral devices. It has been successfully used for lateral high voltage devices such as diodes and LDMOS transistors for 20-1200V, and this technology provides an efficient way to integrate high voltage devices with low voltage circuitry. Devices working on higher voltage require a thick and low-doped epitaxial layer, which makes them difficult to integrate with low voltage circuitry; because of high resistivity epi layer, on-resistance is large. The traditional RESURF structure is constructed by a lateral p+/ n diode that defines the on-resistance characteristics of the device and a vertical p/ n diode that supports a charge depletion region enabling high breakdown voltage (BV).

Fig. 2 defines the on-resistance characteristics of the device and a vertical diode which supports a space charge depletion region enabling increased breakdown voltage. The lateral breakdown voltage of this structure depends on the net charge of the drift region. The maximum BV is determined by the BV of the vertical diode (p-substrate/n-epitaxial).

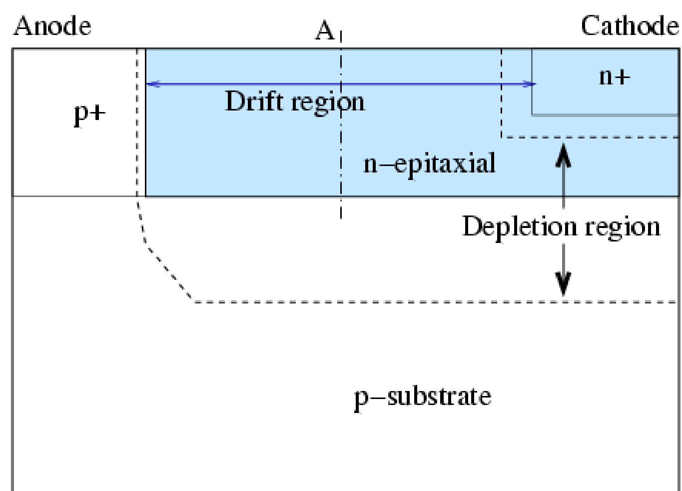

Fig.2 Lateral RESURF structure at full depletion

Net charge in this region is inversely proportional to the drift region-resistance. Because of the vertical junction of the RESURF structure, a second electric field peak forms at the cathode end of the device.

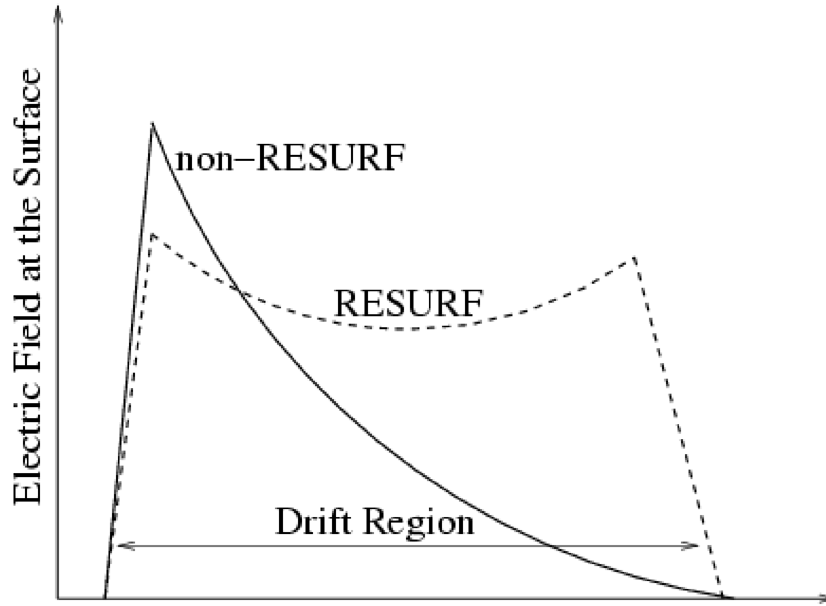

Fig.3 Electric field comparison at the surface

RESURF structures assume a parabolic form. This helps to reduce the electric field at the surface of the device during off. The basic properties of RESURF structures are determined by the p-substrate doping concentration, n-epilayer doping concentration (Nepi), and n-epi layer thickness (tnepi). An approximate net charge Qn of Fig.3 is determined by

$$Q_n = N_{epi} * t_{nepi}$$

The lateral electric field is reduced, as the vertical space charge width extends and interacts with the lateral junction space charge region allowing the lateral depletion width to span a more considerable distance effectively. For high breakdown voltage in the RESURF structure, the n-epi region must be fully depleted before the lateral electric field reaches a critical value.

1.4 Breakdown Voltage

Materials are often classified as conductors or insulators based on their resistivity. A conductor is a substance that contains many mobile charged particles called charge carriers which are free to move around inside the material. An electric field is created across a piece of the material by applying a voltage difference between electrical contacts on different sides of the material. The force of the field causes the charge carriers within the material to move, creating an electric current from the positive contact to the negative contact.

However, if a strong enough electric field is applied, all insulators become conductors. If the voltage applied across a piece of the insulator is increased at a particular electric field strength, the number of charge carriers in the material suddenly increases enormously, and its resistivity drops, causing a solid current to flow through it. This is called electrical breakdown. Breakdown occurs when the electric field becomes strong enough to pull electrons from the molecules of the material, ionizing them. The field accelerates the released electrons and strikes other atoms, creating more free electrons and ions in a chain reaction, flooding the material with charged particles. This occurs at a characteristic electric field strength in each material, measured in volts per centimeter, called its dielectric strength.

When a voltage is applied across a piece of insulator, the electric field at each point is equal to the gradient of the voltage. The voltage gradient may vary at different points across the object due to its shape or local variations in composition. Electrical breakdown occurs when the field first exceeds the dielectric strength of the material in some region of the object. Once one area has been broken down and becomes conductive, that area has almost no voltage drop. The total voltage is applied across the remaining insulator length, resulting in a higher gradient and electric field, causing additional areas in the insulator to break down. The breakdown quickly spreads in a

conductive path through the insulator until it extends from the positive to the harmful contact. The voltage at which this occurs is called the breakdown voltage of that object, and the breakdown voltage varies with the material composition, an object's shape, and the material's length between the electrical contacts [2].

1.5 Hot Carrier Effect

The term “hot carrier effect” usually refers to the effect in MOSFETs, where a carrier is injected from the conducting channel in the silicon substrate to the gate dielectric, which generally is made of silicon dioxide (SiO2) [3].

To become “hot” and enter the conduction band of SiO_2, an electron must gain kinetic energy of ~3.2 eV. For holes, the valence band offset, in this case, dictates they must have a kinetic energy of 4.6 eV. The term "hot electron" comes from the effective temperature term used when modeling carrier density and does not refer to the bulk temperature of the semiconductor.

The term “hot electron” was initially introduced to describe non-equilibrium electrons (or holes) in semiconductors. More broadly, the time describes electron distributions describable by the Fermi function but with an effective elevated temperature. This more incredible energy affects the mobility of charge carriers and, consequently, how they travel through a semiconductor device. Hot electrons can tunnel out of the semiconductor material instead of recombining with a hole or being conducted through the material to a collector. Consequent effects include increased leakage current and possible damage to the encasing dielectric material if the hot carrier disrupts the atomic structure of the dielectric (Fig. 4).

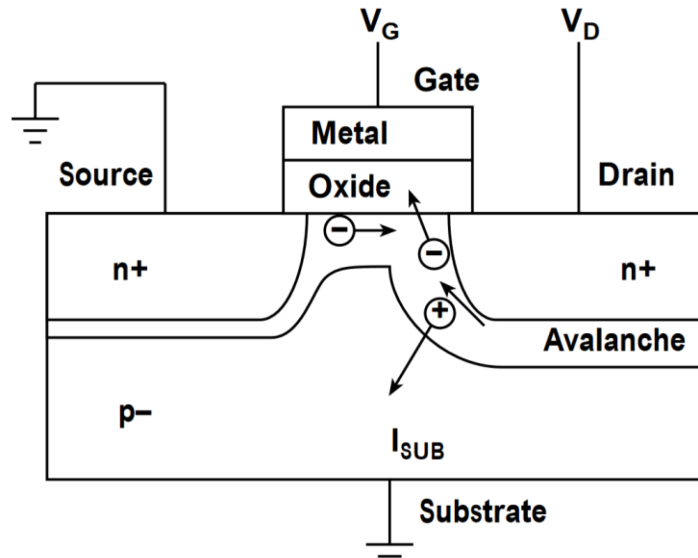

Fig.4 Evaluating hot carrier-induced degradation of MOSFET devices

1.6 Safe Operating Area (SOA)

The safe operating area (SOA) is defined as the current and voltage conditions over which an IGBT can be expected to operate without self-damage or degradation [4]. In practice, it is necessary not only to use an IGBT within the safe operating area but also to derate its area for temperature. There are forward-bias and reverse-bias safe operating areas (FBSOA and RBSOA). The forward-bias safe operating area defines the usable current and voltage conditions for the period while the IGBT is on. The reverse-bias safe operating area defines the MOSFET's usable current and voltage conditions during the turn-off period.

Fig. 5 shows an example of a forward-bias safe operating area, which consists of four regions: (1) a region limited by the maximum collector current rating, (2) a region limited by collector power dissipation (thermal breakdown), (3) a region limited by secondary breakdown, and (4) a region limited by the maximum collector-emitter voltage rating. Care should be exercised in the region limited by secondary breakdown because it differs depending on the device design.

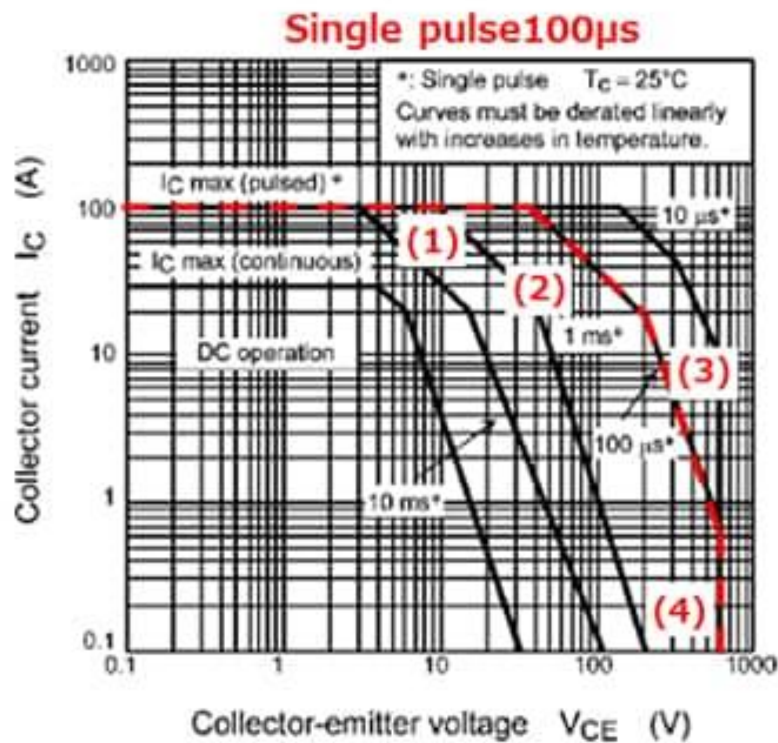

Fig.5 Forward-bias SOA

Fig. 6 shows an example of a reverse-bias safe operating area, which consists of three regions: (1) a region limited by the maximum collector current rating (ICP), (2) a region limited by the inherent characteristics of a device, and (3) a region limited by the maximum collector-emitter voltage rating (VCES). In the second region, the maximum current is inverse to VCE. Hard-switching applications, in particular, should be designed to satisfy this SOA region's limit.

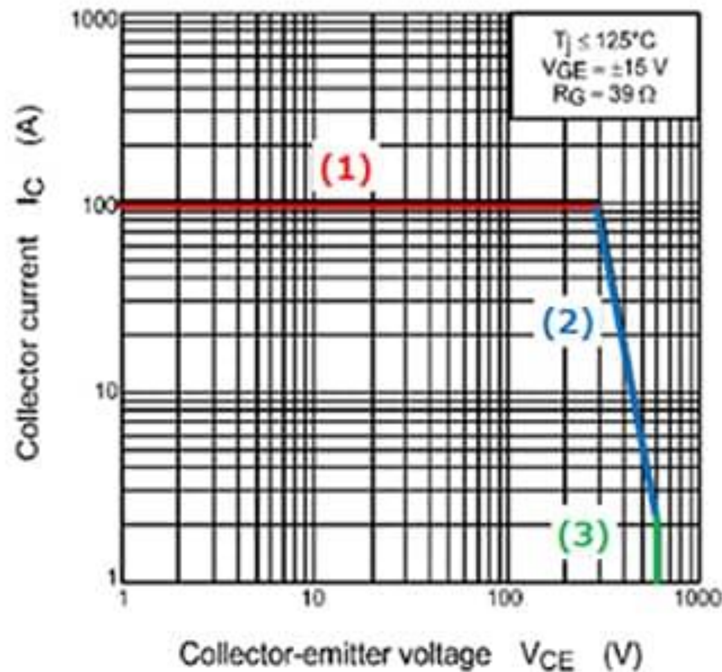

Fig.6 Reverse-bias SOA

1.7 Miller effect

The Miller effect in MOSFET will be like an increase in input capacitance at the input gate caused by the gain of the MOSFET stage [5]. The feedback capacitance comprises the gate to drain capacitance and the added circuit capacitance between the output and input of the MOSFET amplifier stage. It will reduce the gain at the high frequencies.

The Miller capacitance is due to in-build capacitance between input and output of active devices like MOSFETs, BJT, and IGBT. This must be a significant limitation to their gain at higher frequency operation. That is the effective capacitance at their input and output due to the Miller effect.

The Miller effect badly affected the gain of the active device at high frequency (Fig. 7). This will result from the amplifier's bandwidth reduction, and they will restrict the range of operation to a lower frequency. The tiny junction between the base to the collector at the transistor will increase drastically with the Miller effect.

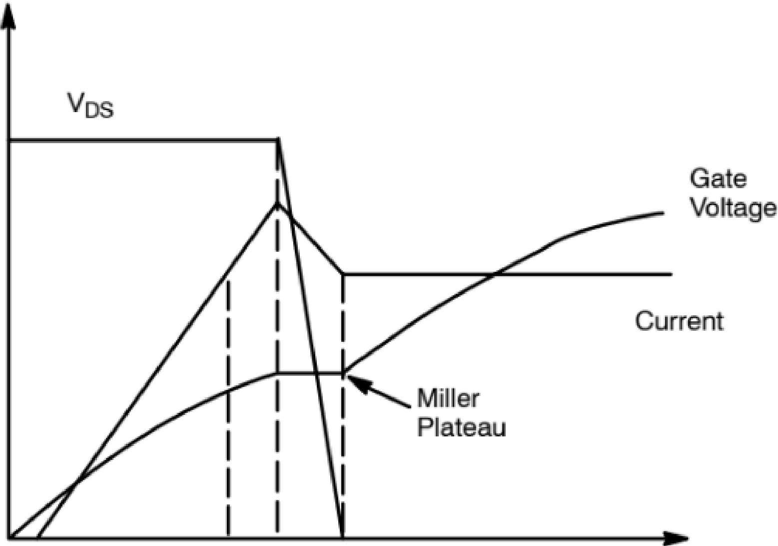

Fig.7 Dynamic changes in gate capacitance during startup cause the Miller plateau

Chapter2: Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Grounded Field Plate

2.1 Conventional and Proposed LDMOS transistor

Figs. 8 and 9 show rough cross-sectional views of the conventional and the proposed LDMOS transistors. The structures inside the silicon of both devices are the same. Two P-type buried layers, PBL1 and PBL2, for both devices form a dual RESURF structure which reduces the electric field in the drift region adequately. The difference between both devices is how the field plate is connected. The field plate in the conventional device is connected to the gate, while one in the proposed device to the ground. Therefore, the proposed device has a much lower Miller capacitance than the conventional device, leading to a lower switching loss. The specific on-resistances of the conventional and the proposed devices are 39.8 mΩmm2 and 40.8 mΩmm2, respectively. This lower on-resistance of the former device is due to the field plate connected to the gate, which reduces the resistance in the drift region in the on-state. The extrapolated threshold voltages of the conventional and the proposed devices are the same, 1.05 V.

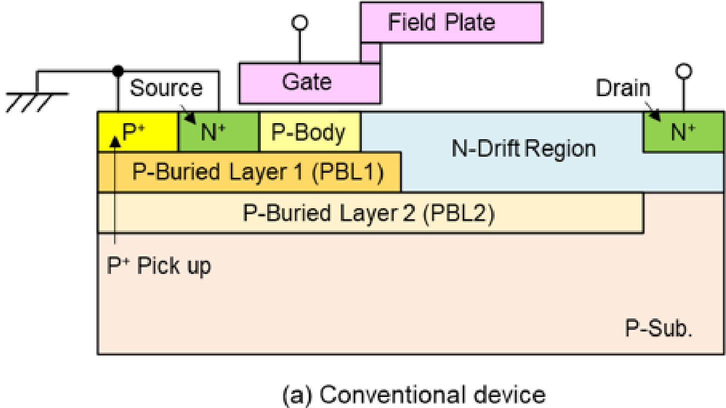

Fig.8 Rough cross-sectional views of the conventional

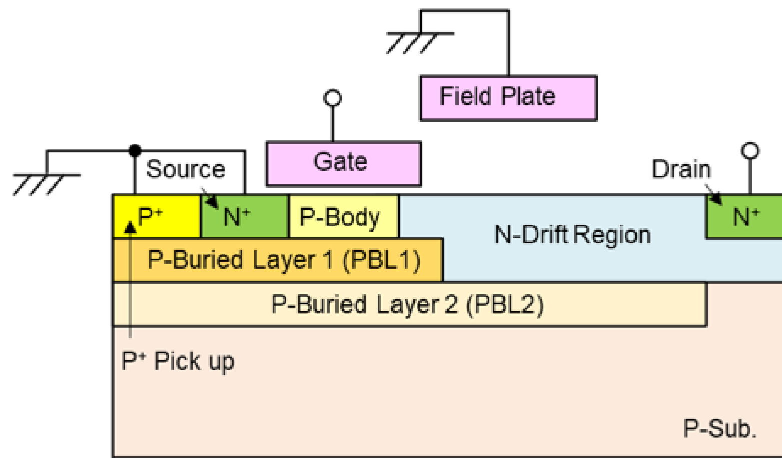

Fig.9 Rough cross-sectional views of the proposed devices.

2.2 Measurement Circuit and Parasitic Capacitances

We have analyzed the switching characteristics of the proposed device in detail by changing the load resistance R_L and the gate resistance R_G as shown in Fig. 10. We change R_L from 2.13 Ωmm^2 to 10.7 Ωmm^2 and R_G from 1.07 Ωmm^2 to 5.33 Ωmm^2 for a unit LDMOS layout area of 1 mm^2.

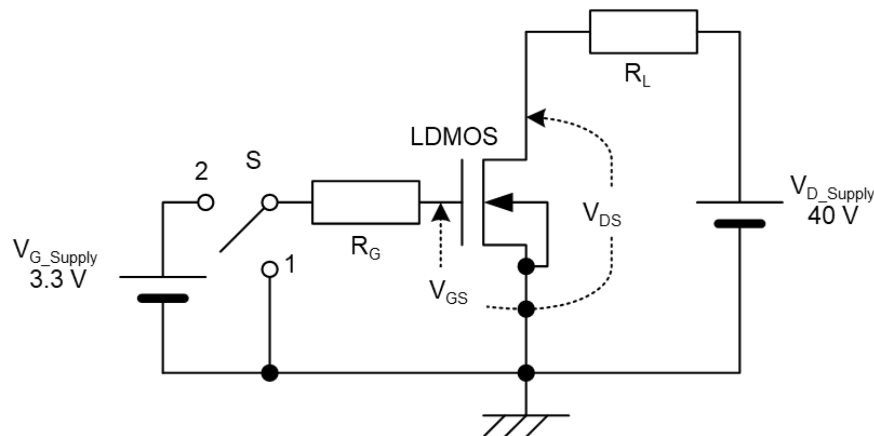

Fig.10 Circuit for device simulation (TCAD)

We greatly appreciate AdvanceSoft Corporation for providing us with some licenses for using the 3D TCAD simulator. Japan Science and Technology Agency (National Research and Development Agency) assisted in the development of the simulator by using the A-STEP program.

We use the device simulator in 3D TCAD developed by Advancesoft Corporation (Fig. 11). With the TCAD simulation software, Hot Carrier Effect, Breakdown Voltage, etc. can also be observed in the simulation results.

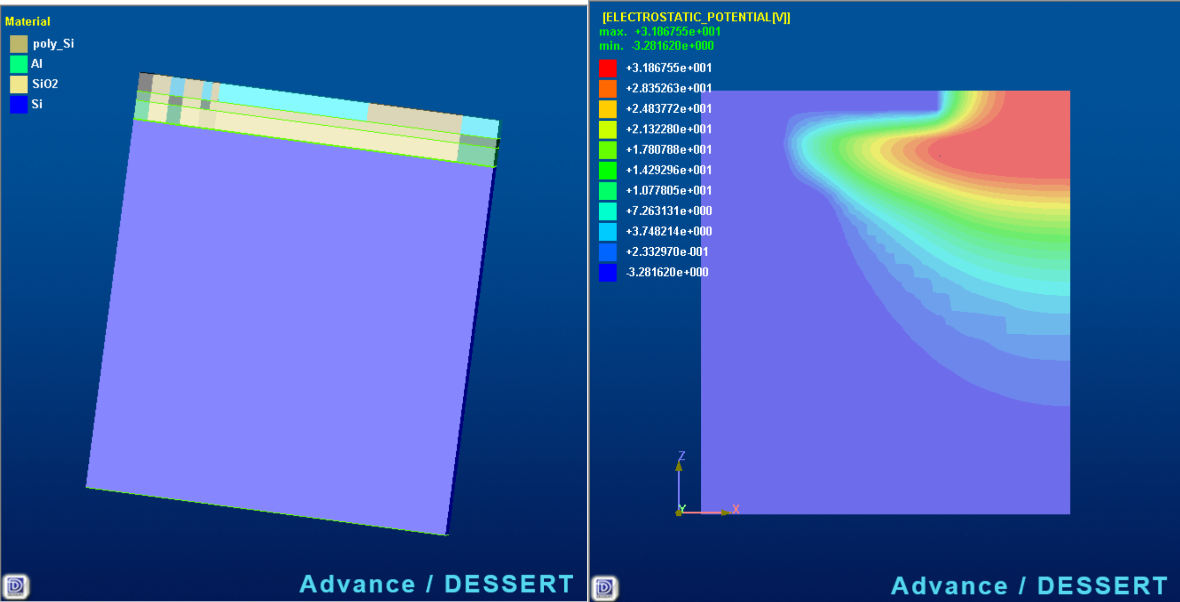

Fig.11 Simulator in 3D TCAD developed by Advancesoft Corporation

In TCAD we have simulated the circuit with different load resistance R_L and gate resistance R_G. Using the TCAD simulation, we can obtain the experimental data, which can be analyzed and calculated. The switching losses of the gate and drain can be plotted separately. In calculating the switching loss we use Simpson's rule(see Fig.12).

$$\int_b^a f(X)dx = \frac{h}{3}[f(a) + 4f(a+h) + 2f(a+2h) + \cdots]$$

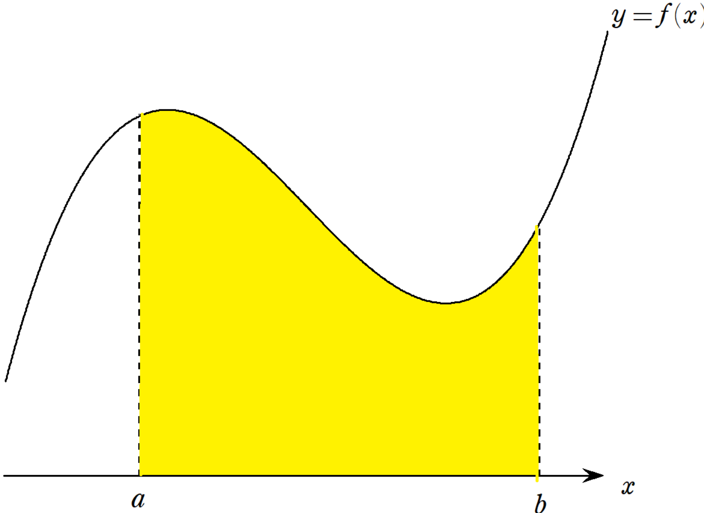

Fig.12 Simpson's rule

2.3 Simulation Results

2.3.1 Turn-on Process

Fig. 13 shows the turn-on characteristics of the conventional and the proposed devices. Turn-on characteristics of the former device divide into four regions (See Fig. 13 (a)). Region A is in the off-state due to the gate-source voltage V_{GS} less than the threshold voltage V_T where V_{GS} increases and the gate current I_G, the gate current density J_G, flows, charging the input capacitance (C_{GS}), the feedback capacitance (the Miller capacitance: C_{GD}+C_{FD}), and the output capacitance (C_D) (See Table 1 for the capacitances). Region B is in the gate plateau state due to charging C_{GD}+C_{FD}, where the drain-source voltage V_{DS} decreases and the drain current density J_D increases, causing a long and intense Miller effect and discharging C_D (See Fig. 14 (a)). Region C is also in the gate plateau state, but the RESURF effect in the gate-side drift region around the drain of the intrinsic MOSFET disappears in this region, leading to a steep decrease in the drain voltage of the intrinsic MOSFET VDS_INT. Region D is in the on-state.

Turn-on characteristics of the proposed device are divided into four regions (See Fig. 13 (b)). Region A is in the off-state due to $V_{GS} < V_T$, where V_{GS} increases and I_G flows, charging the input capacitance (C_{GS}+C_{FG}), the feedback capacitance (C_{GD}), and the output capacitance (C_D+C_{FD}) (See Table 1 for the capacitances). Region B is in the J_D increasing and V_{DS} decreasing state with increasing V_{GS}, where the increase in the displacement current density (J_{FP}+J_{PB}+J_{Sub}) due to discharging C_D+C_{FD} causes a gradual decrease in V_{DS_INT}. Therefore, C_{GD} mainly charges by increasing V_{GS}, resulting in a weak Miller effect (See Fig. 14 (b)). Region C is in the gate plateau state, or a convex-shape gate plateau state, due to charging C_{GD} caused by a steep decrease in V_{DS_INT}, indicating a short but slightly intense Miller effect. This decrease is because the RESURF effect in the gate-side drift region around the drain of the intrinsic MOSFET disappears. Region D

is in the on-state. The characteristics of V_{DS} and J_D in Regions B and C of the proposed device are significantly different from those of the conventional device. This difference is because the field plate of the proposed device is the output capacitance, while that of the conventional one is the feedback capacitance.

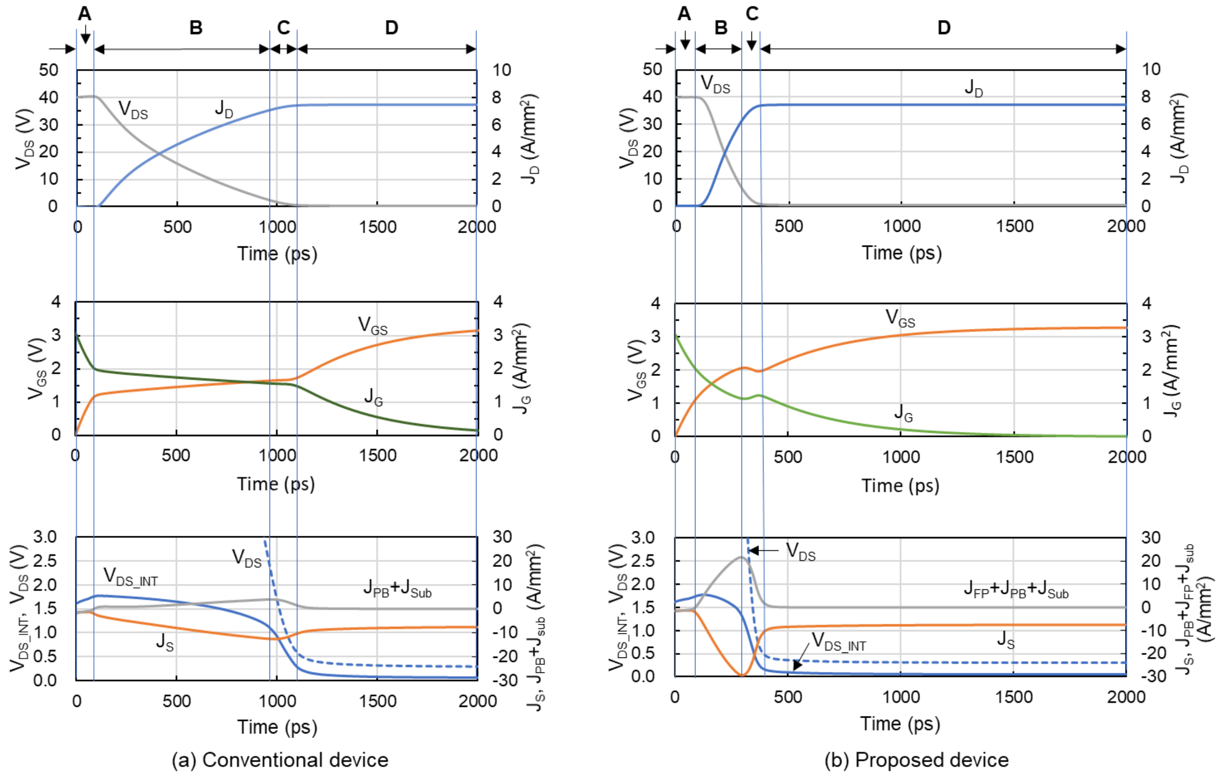

Fig. 13. Changes in turn-on characteristics with time at a low R_G of 1.07 Ωmm^2 and a middle R_L of 5.33 Ωmm^2 with a unit LDMOS layout area of 1 mm^2. The above characteristics are similar to those obtained under other conditions simulated in this paper.

Table 1. Parasitic capacitances in the LDMOS transistor. C_{GC} practically works when $V_{GS} > V_T$.

Capacitance	Conventional	Proposed
Input capacitance	$C_{GS}+C_{GC}$	$C_{GS}+C_{GC}+C_{FG}$
Feedback capacitance	$C_{GD}+C_{FD}$	C_{GD}
Output capacitance	C_D	C_D+C_{FD}

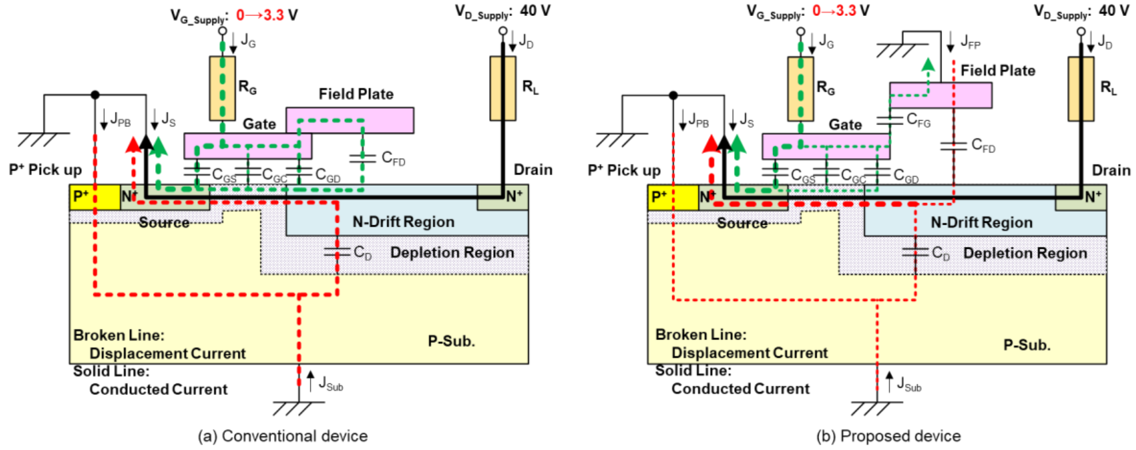

Fig. 14 Current paths for turn-on process when $V_{GS} > V_T$. After V_{GS} attaining the gate supply voltage V_{G_Supply}, displacement currents through parasitic capacitances disappear, and the conduction current from the drain to the source leaves.

2.3.2 Turn-off Process

Fig. 15 shows the turn-off characteristics of the conventional and the proposed devices. The turn-off process takes much longer than the turn-on process. Turn-off characteristics of the former device is divided into four regions (See Fig. 15 (a)). Region A is in the on-state due to $V_{GS} > V_T$, where V_{GS} decreases and $|J_G|$ also decreases, discharging the input capacitance (C_{GS}+C_{GC}) and the feedback capacitance (C_{GD}+C_{FD}), and then the increase in V_{DS_INT} and V_{DS} charges the output capacitance (C_D). At the end of Region A, the RESURF effect occurs in the gate-side drift region around the drain of the intrinsic MOSFET. Region B is in the gate plateau state where V_{DS} increases and J_D decreases, charging C_D and C_{GD}+C_{FD}; charging C_{GD}+C_{FD} causes a long and intense Miller effect (See Fig. 16 (a)). Region C is in the off-state of the intrinsic MOSFET due to almost no source current density J_S, where V_{DS} still increases, charging C_D and C_{GD}+C_{FD}. Region D is the off-state.

Turn-off characteristics of the proposed device is divided into four regions (See Fig. 15 (b)). Region A is in the on-state due to $V_{GS} > V_T$. The process of this region is almost similar to that of the conventional device. Here, the decrease in V_{GS} discharges the input capacitance (C_{GS}+C_{GC}+C_{FG}) and the feedback capacitance (C_{GD}), and the increase in V_{DS_INT} and V_{DS} charges the output capacitance (C_D+C_{FD}) mainly. At the end of Region A, the RESURF effect occurs in the gate-side drift region around the drain of the intrinsic MOSFET. Region B is in the beginning stage of turn-off due to $V_{GS} \gtrsim V_T$, where V_{DS} starts to increase and J_D decrease. In this region, a slight increase in V_{DS_INT} and a slight decline in V_{GS} cause a short and weak Miller effect, no gate plateau is observed, and the displacement current density (J_{FP}+J_{PB}+J_{Sub}) charges the output capacitance (C_D+C_{FD}) (See Fig. 16 (b)). Region C is in the off-state of the intrinsic MOSFET due to almost no source current density J_S, where V_{DS} increases significantly, charging C_D+C_{FD} mainly. Region D is the off-state. In the turn-off process, the energy loss of the proposed device mainly occurs in Region C due to charging the output capacitance (C_D+C_{FD}), while that of the conventional ones, in Region B due to charging two capacitances of the output capacitance (C_D) and the feedback capacitance (C_{GD}+C_{FD}).

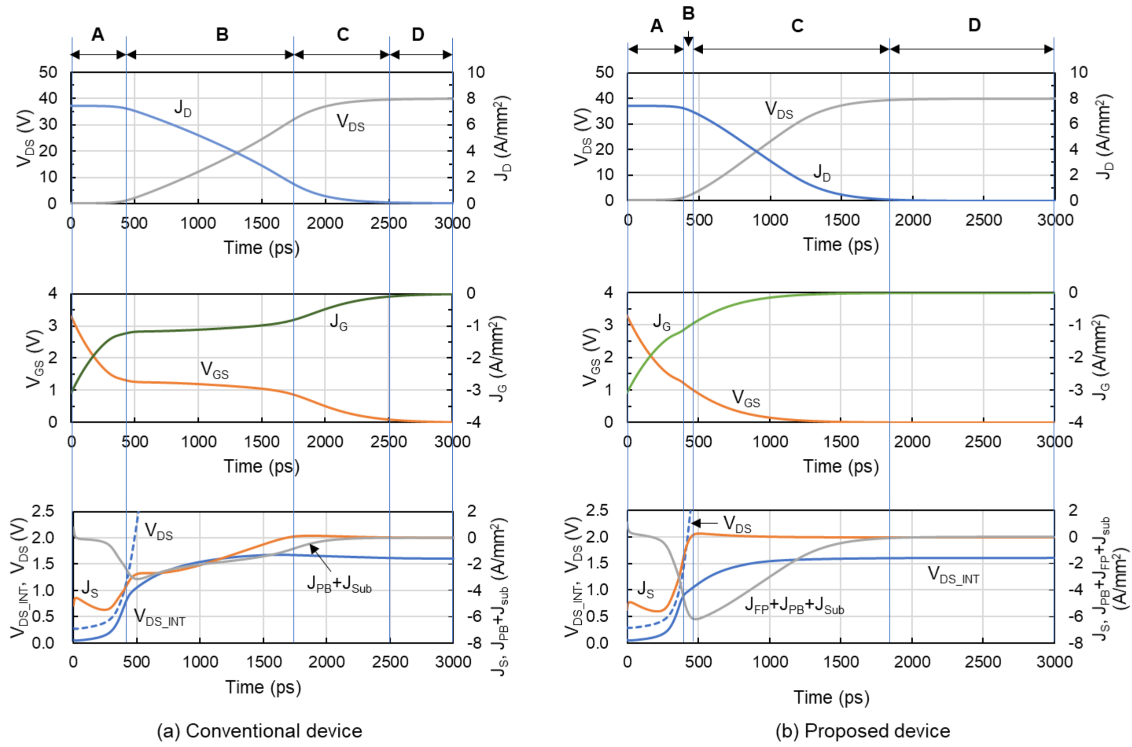

Fig. 15 Changes in turn-off characteristics with time at a low R_G of 1.07 Ωmm^2 and a middle R_L of 5.33 Ωmm^2 with a unit LDMOS layout area of 1 mm^2. The above characteristics are similar to those obtained under other conditions simulated in this paper.

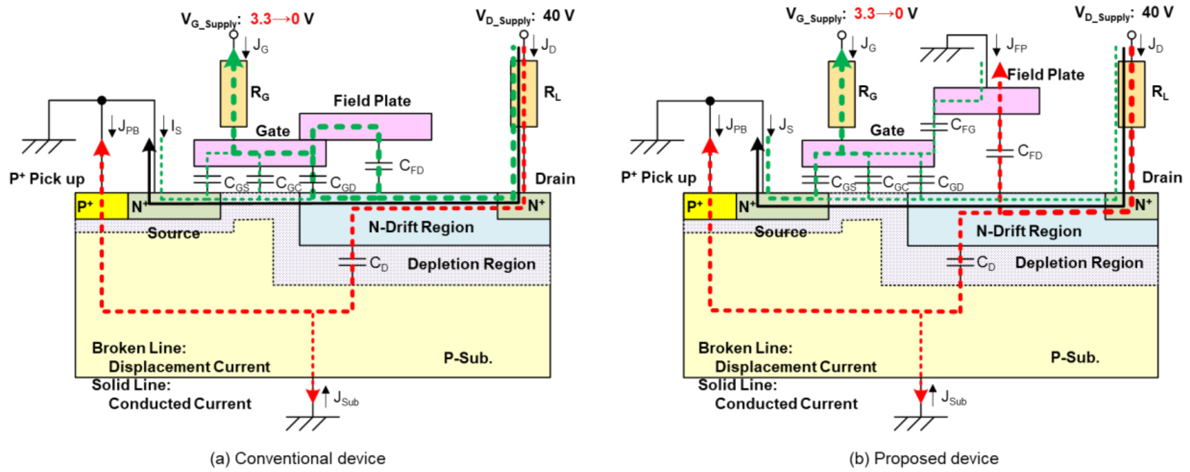

Fig. 16 Current paths in Region B for turn-off process. In Region C of both devices, the conducted current and the current through C_{GC} disappear.

Chapter 3: Low Switching Loss Dual RESURF 40 V N-LDMOS with Grounded Field Plate for DC-DC Converters

3.1 Device Structure and Measurement Circuit

Fig. 17 shows the rough cross-sectional view of the proposed 40 V operation N-channel LDMOS transistor made by a 0.18 μm CMOS compatible process. The field plate of the proposed LDMOS transistor is connected to the ground, while that of the conventional one connects to the gate. This field plate structure of the proposed device reduces the Miller capacitance drastically, leading to low switching loss. The length of the drift region L_D fixed is 2650 nm, that of the field plate L_{FP}, 1625 nm at standard L_{FP_std}, the thickness of the oxide interlayer between the field plate and the drift region T_{OX1}, 308 nm at standard T_{OX1_std}, and that of the oxide interlayer between the field plate and the gate T_{OX2}, 100 nm at standard T_{OX2_std}. The breakdown voltage between the drain and the source BVDS is 61 V above standard size. The optimized LFP and TOX1 (or TOX2) range should meet $BV_{DS} > 60$ V with the lowest possible switching loss. P-buried layer 1 (PBL1) and P-buried layer 2 (PBL2) have a dual RESURF structure. PBL1 reduces the electric field in the drift region around the gate edge, and PBL2 makes the electric field in the drift region uniform.

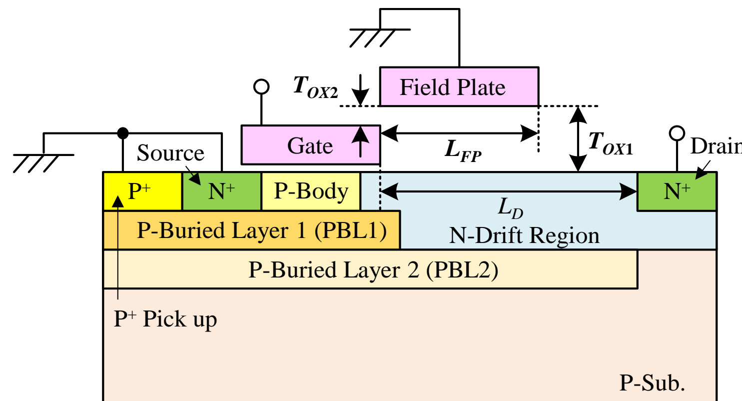

Fig. 17 Rough cross-sectional view of the proposed LDMOS transistor

3.2 Measurement Circuit and Parasitic Capacitances

Fig. 18 shows the circuit measuring switching characteristics for the proposed LDMOS transistor. The specific on-resistance of the device is 40.8 mΩmm^2, and the load resistance and the gate resistance are 5.33 Ωmm^2 and 1.07 Ωmm^2, respectively. The drain supply voltage V_{D_supply} and the gate supply voltage V_{G_supply} are 40 V and 3.3 V, respectively. The extrapolated threshold voltage is 1.05 V.

Fig. 19 shows parasitic capacitances and the definition of current densities. The input capacitance is the sum of the gate-source capacitance C_{GS}, the gate-channel capacitance C_{GC}, and the field plate-gate capacitance C_{FG}. The output capacitance is the sum of the field plate-drift capacitance C_{FD} and the depletion capacitance C_D, and the feedback capacitance is the gate-drain capacitance C_{GD}, while J expresses current density.

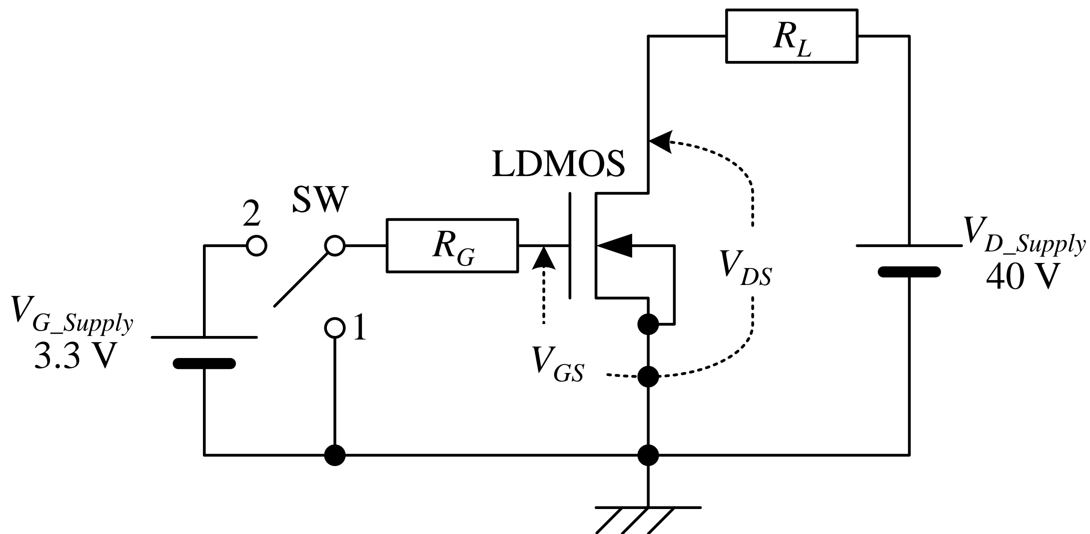

Fig. 18 Measurement circuit

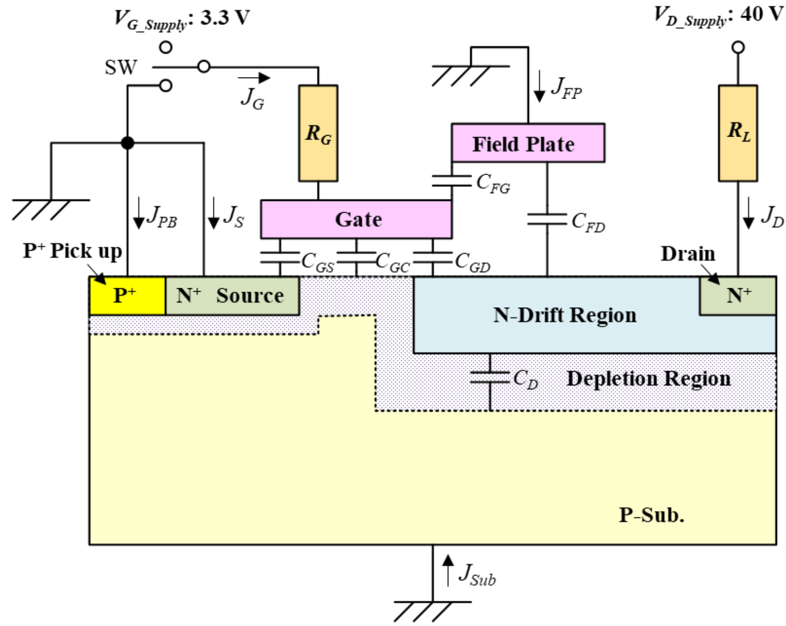

Fig. 19 Parasitic capacitances and the definition of current densities.

3.2 Simulation Results

3.2.1 L_{FP} and T_{OX1} Dependence on Switching Loss

Fig. 20 shows the dependence of L_{FP} on the drain energy dissipation density per switching cycle (or drain loss) E_{D_Loss} with T_{OX1} as a parameter. Here, the horizontal axis is ΔL_{FP} (=L_{FP} - L_{FP_std}) instead of L_{FP}, and the parameter, ΔT_{OX1} (=T_{OX1} - T_{OX1_std}) instead of T_{OX1}. E_{D_Loss} increases with increasing in ΔL_{FP} at any ΔT_{OX1} and in ΔT_{OX1} at any ΔL_{FP}. These characteristics are because the displacement current through the output capacitance increases with increasing in ΔL_{FP} or decreasing in ΔT_{OX1} during turn-on and turn-off.

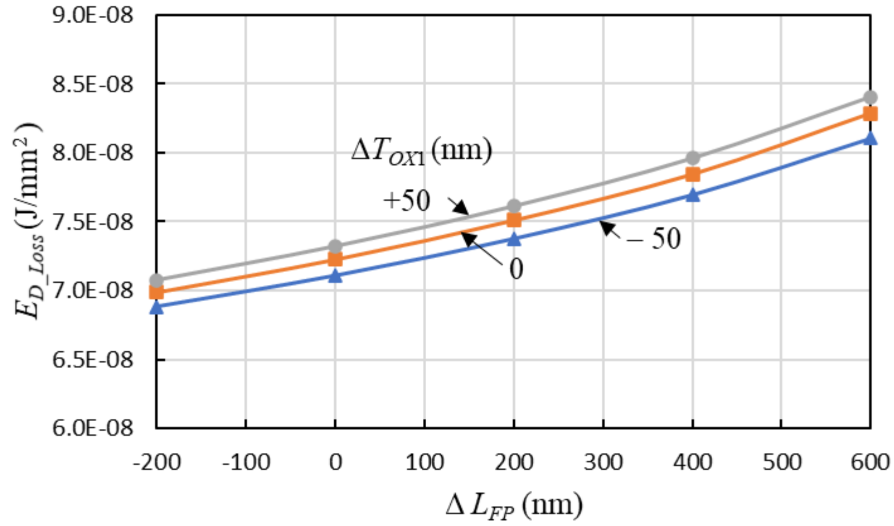

Fig. 20 L_{FP} dependence on E_{D_Loss} with T_{OX1} as a parameter.

Fig. 21 shows the dependence of L_{FP} on the gate driving energy dissipation density per switching cycle (or gate loss) E_{G_Loss} with T_{OX1} as a parameter. Also, the horizontal axis is ΔLFP, and the parameter is ΔT_{OX1}. These characteristics are because when seeing from the gate, only a part of the input capacitance C_{FG}, increases with decreasing in ΔT_{OX1}.

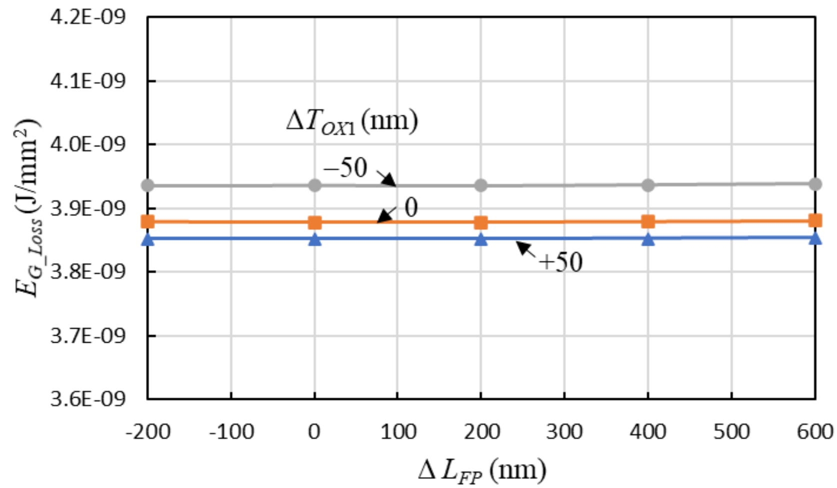

Fig. 21 L_{FP} dependence on E_{G_Loss} with T_{OX1} as a parameter.

Fig. 22 shows the dependence of L_{FP} on the total energy dissipation density per switching cycle (or drain and gate losses) E_{T_Loss} with T_{OX1} as a parameter. Also, the horizontal axis is ΔL_{FP}, and the parameter is ΔT_{OX1}. It is noticed from Figs. 20 and 21 that the amount of E_{G_Loss} is about 1/20 lower than that of E_{D_Loss}. Therefore, E_{T_Loss} expresses almost E_{D_Loss}.

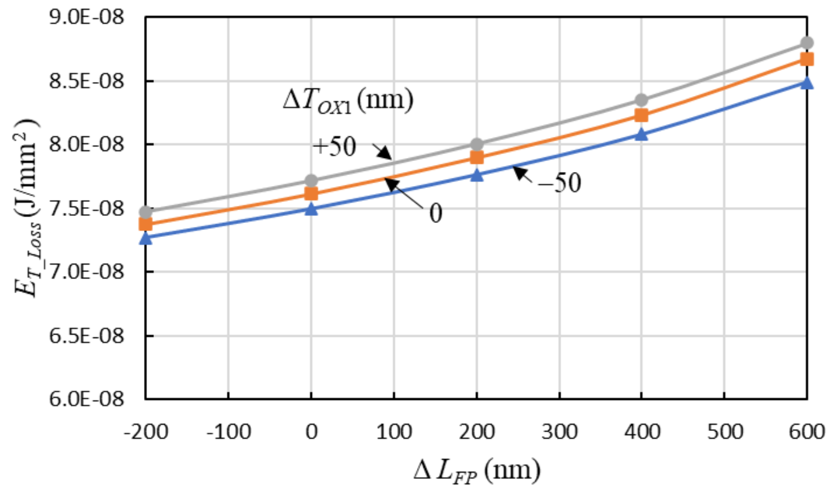

Fig 22 L_{FP} dependence on E_{T_Loss} with T_{OX1} as a parameter.

3.2.2 Breakdown Voltage

Fig. 23 shows the dependence of L_{FP} on BV_{DS} with T_{OX1} as a parameter. Here, the horizontal axis is ΔL_{FP}, and the parameter is ΔT_{OX1}. Each BV_{DS} characteristic for -50 nm $\leq \Delta T_{OX1} \leq +50$ nm has one peak, while that for $\Delta T_{OX1} = +100$ nm increases monotonically. As for -50 nm $\leq \Delta T_{OX1} \leq$ $+50$ nm, the location of breakdown moves from the neighborhood of the PBL1 edge to that of the PBL2 edge with increasing ΔL_{FP} (See Fig.24). This phenomenon is because with increasing ΔL_{FP}, the electric field near PBL1 edge decreases by the increased RESURF effect and that near PBL2 edge increases. If the location of breakdown is the neighborhood of the PBL1 edge, ESD (Electro

Static Discharge) endurance may decrease due to the generation of filamentation in the drift region. Therefore, the breakdown near the PBL2 edge is preferable to enhance ESD endurance, resulting in that $\Delta L_{FP} \geq 0$ nm for $\Delta T_{OX1} = 0$ nm and $\Delta T_{OX1} = -50$ nm needed (See Fig.24).

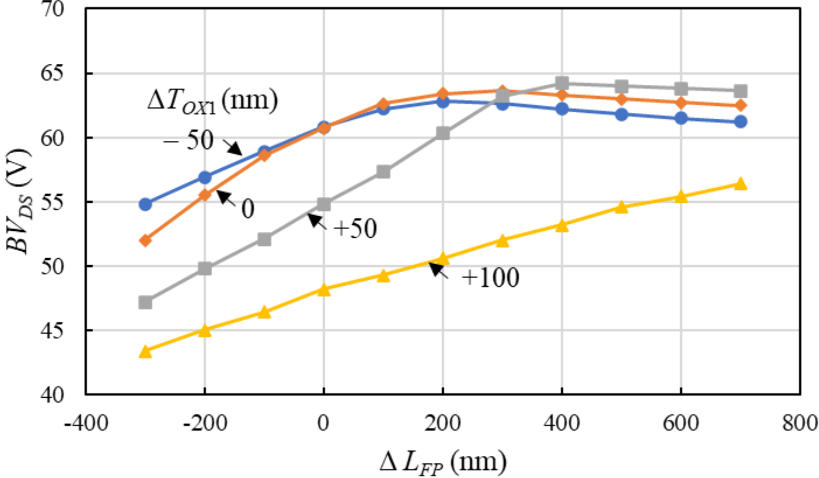

Fig. 23 L_{FP} dependence on BV_{DS} with T_{OX1} as a parameter.

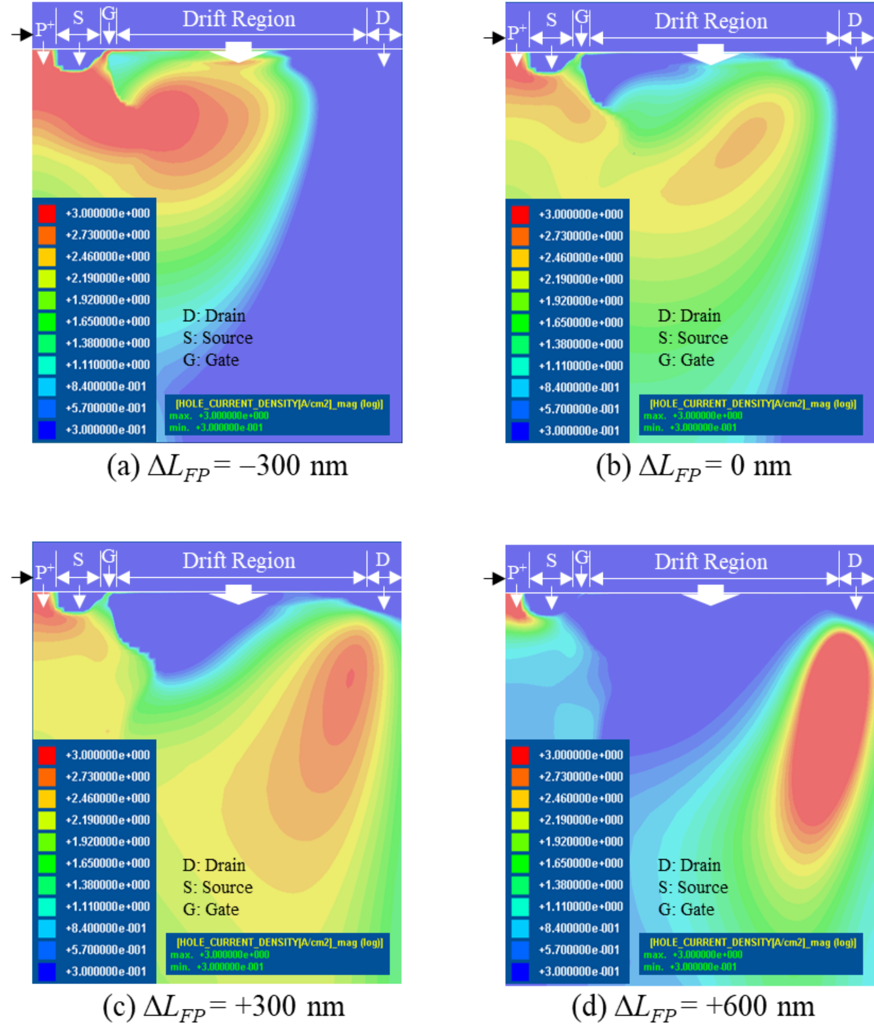

Fig. 24 Change in the hole current density distribution upon breakdown depending on ΔL_{FP} for $\Delta T_{OX1} = 0$ nm. Almost the same distribution is observed for $\Delta T_{OX1} = -50$ nm. As for $\Delta T_{OX1} = +50$ nm, the field plate for $\Delta L_{FP} \geq 400$ nm causes a high hole current density region near the PBL2 edge. The location of the higher hole current density under the drift region expresses breakdown.

The range of ΔT_{OX1} and ΔL_{FP} meeting $BV_{DS} > 60$ V is (1) 0 nm $\leq \Delta L_{FP} \leq$ 700 nm for −50 nm $\leq \Delta T_{OX1} \leq$ 0 nm, and (2) 200 nm $\leq \Delta L_{FP} \leq$ 700 nm at ΔT_{OX1} = +50 nm. Here, the range (1) is better to minimize the switching loss. In this case, the standard condition of ΔL_{FP} = 0 nm is the minimum. If the range of the mass production variation of ΔL_{FP} is 0 nm $\leq \Delta L_{FP} \leq$ 200 nm and that of ΔT_{OX1}, −50 nm $\leq \Delta T_{OX1} \leq$ 0 nm, which sufficiently meets the process variation tolerance of the sub-micron

process, the minimum value of E_{T_Loss} is 7.49×10^{-8} J/mm^2, and the maximum value of E_{T_Loss} is 7.90×10^{-8} J/mm^2; namely, the maximum goes up 5.4 % from the minimum. E_{T_Loss} at the center of the variation range is 7.69×10^{-8} J/mm^2. E_{T_Loss} at the standard condition (ΔL_{FP} = 0 nm and ΔT_{OX1} = 0 nm) reduces to 53.2 % that of the conventional LDMOS transistor, whose field plate connecting to the gate is only different from the proposed device [3]. The proposed device also shows a switching loss of 0.077 W/mm^2 at a high switching frequency of 1 MHz with the center value of $E_{T_Loss.\ It}$ has a conduction loss of 1.115 W/mm^2 at a duty ratio of 0.5, where on-current density is 7.45 A/mm^2 and on-voltage 0.3 V. Therefore, the proposed device has significantly lower switching loss.

Chapter 4: Discussion

4.1 Discussion of Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Grounded Field Plate

The proposed device showed unique switching characteristics, the convex-shape gate plateau in the turn-on process and no gate plateau in the turn-off process, caused by the considerably lower feedback capacitance (C_{GD}) despite the higher output capacitance (C_D+C_{FD}). This unique capacitance structure of the proposed device decreases the total energy loss than the conventional one under actual usage conditions significantly.

Fig. 25 (a) shows the dependences of switching losses of R_L under a low R_G of 1.07 Ωmm^2 (high-speed switching), and Fig. 26 (b) shows those of R_G under a high R_L of 10.7 Ωmm^2 (light load). Fig. 25 (a) states that the switching loss of the conventional device is much higher than that of the proposed device as R_L decreases (or load becomes heavy). This result is because the switching loss of the conventional device mainly increases in the long gate plateau region as R_L decreases, while that of the proposed device gradually increases as R_L decreases due to the weak Miller effect in a short time. Fig. 26 (b) states that the switching loss of the conventional device is much higher than that of the proposed device as R_G increases. This result is because the gate plateau region for the conventional device affecting the switching loss becomes longer as R_G increases, while the switching loss of the proposed device is almost constant even as R_G increases due to the weak Miller effect.

Fig. 27 shows the switching frequency f dependence of the total energy loss of the proposed device E_{Loss_P} divided by that of the conventional device E_{Loss_C}. The total energy loss consists of

the switching loss (turn-on and turn-off) and the conduction loss. Fig. 9 picks up Case A (a low R_G of 1.07 Ωmm^2.

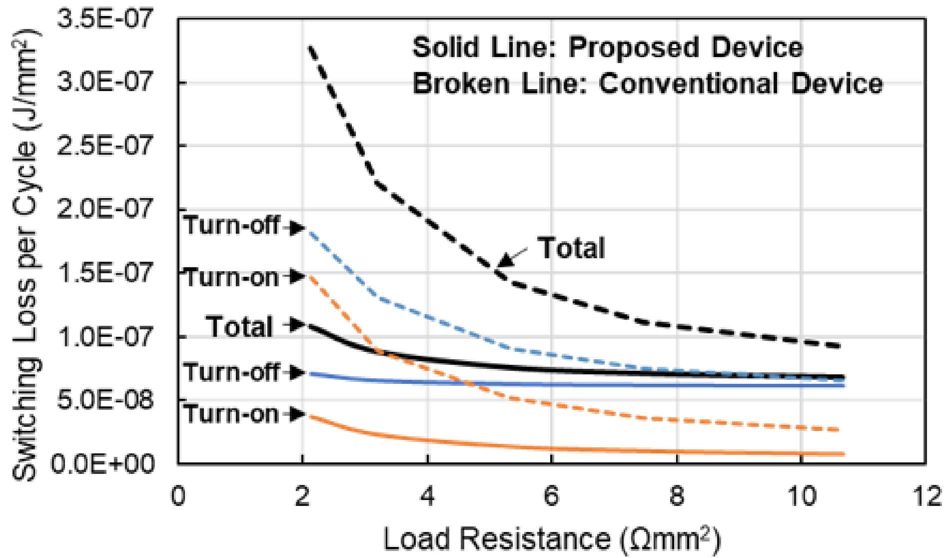

Fig. 25 Dependences of switching losses of (a) R_L under a low R_G of 1.07 Ωmm^2 (high-speed switching) at a unit LDMOS layout area of 1 mm^2.

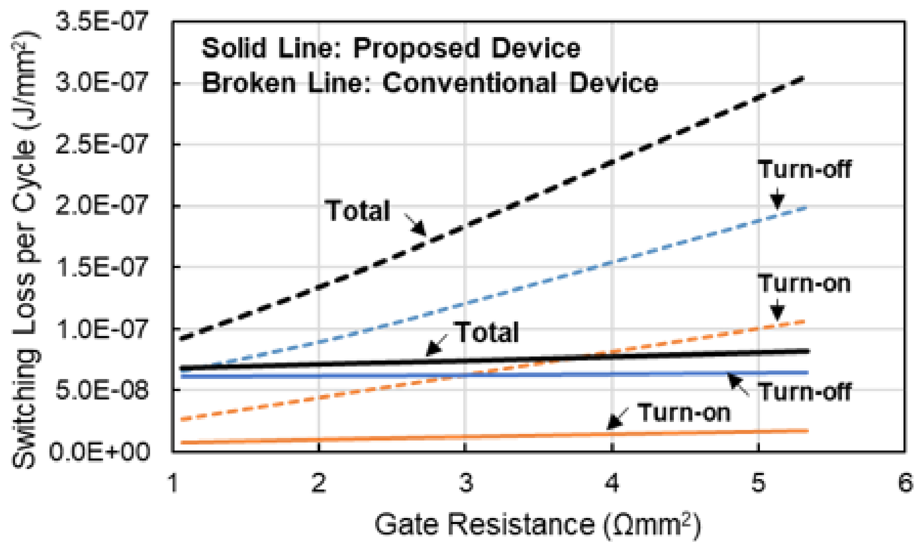

Fig. 26 Dependences of switching losses of (b) R_G under a high R_L of 10.7 Ωmm^2 (light load) at a unit LDMOS layout area of 1 mm^2.

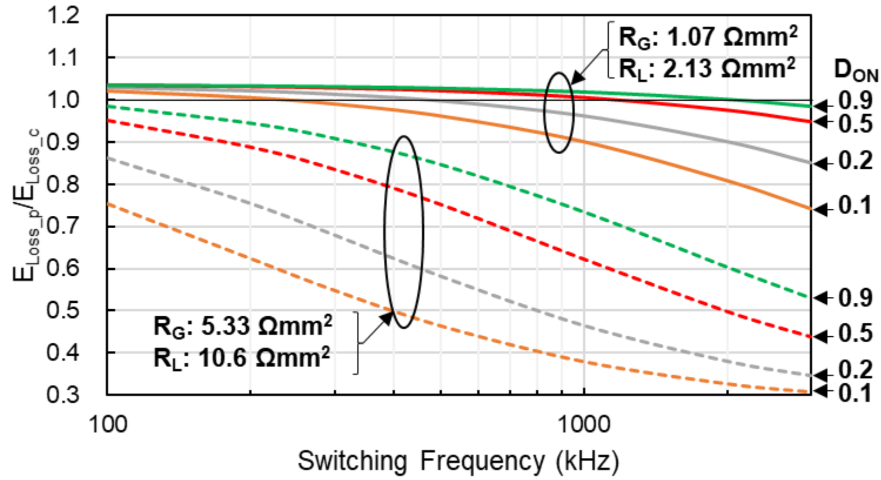

Fig. 27 The switching frequency dependence of the total energy loss ratio E_{Loss_P}/ E_{Loss_C} at a unit LDMOS layout area of 1 mm^2.

and a low R_L of 2.13 Ωmm^2) and Case B (a high R_G of 5.33 Ωmm^2 and a high R_L of 10.6 Ωmm^2) at a device layout area of 1 mm^2. Case A is a good example of containing a high conduction loss, while Case B is a good example of containing a high switching loss. In Case A, although E_{Loss_P}/ E_{Loss_C} decreases with increasing f, E_{Loss_P}/ E_{Loss_C} is higher than one until a high switching frequency range when duty ratio D_{ON} is high. This result is because the specific on-resistance of the proposed device is higher than that of the conventional device. In Case B, E_{Loss_P}/ E_{Loss_C} also decreases with increasing f, and E_{Loss_P}/ E_{Loss_C} attains the lowest value of 0.31 at f = 3 MHz and D_{ON} = 0.1. Therefore, in the actual use condition range, the total energy loss of the proposed device is much lower than that of the conventional device.

4.2 Discussion of Low Switching Loss Dual RESURF 40 V N-LDMOS with Grounded Field Plate for DC-DC Converters

4.2.1 L_{FP} Dependence on Turn-on Characteristics

Fig. 28 shows the change in the drain-source voltage V_{DS} and the drain current density J_D with time for ΔL_{FP} of 0 nm and +600 nm during turn-on. The J_D for ΔL_{FP} = +600 nm is lower than that for ΔL_{FP} = 0 nm, and the V_{DS} for ΔL_{FP} = +600 nm is higher than that for ΔL_{FP} = 0 nm. The lower J_D for ΔL_{FP} = +600 nm is caused by a higher displacement current density $J_{PB}+J_{FP}+J_{Sub}$ for ΔL_{FP} = +600 nm, where mainly J_{FP} is higher due to a larger C_{FD}. Since the intrinsic MOSFET in the LDMOS transistor is in the saturation state from 100 ps until about 320 ps, only V_{GS} determines the channel current for that duration. Therefore, when $J_{PB}+J_{FP}+J_{Sub}$ is flowing into the channel in the saturation state increases, J_D decreases. Since $J_{PB}+J_{FP}+J_{Sub}$ also flows in the drift region, the higher $J_{PB}+J_{FP}+J_{Sub}$ for ΔL_{FP} = +600 nm increases the voltage drop in the drift region, resulting in a higher V_{DS}.

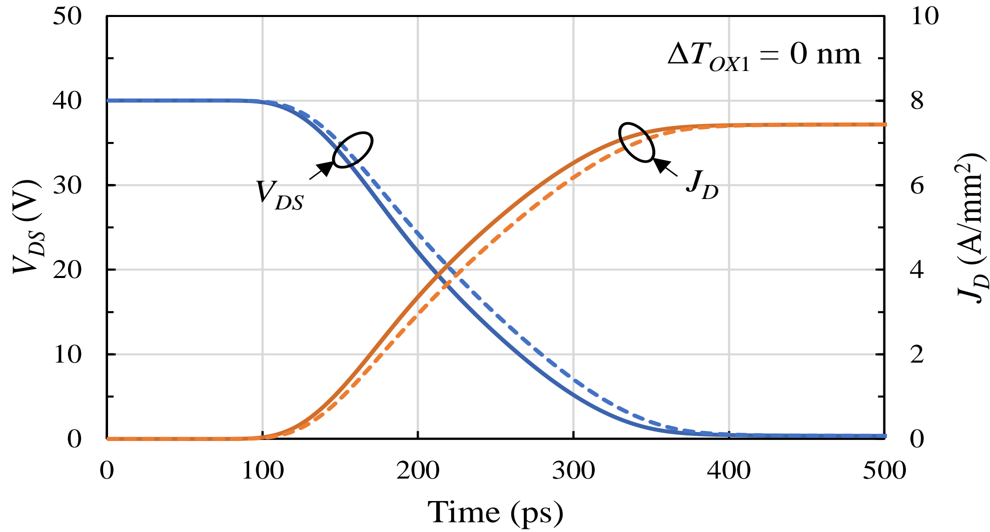

Fig. 28 Change in V_{DS} and J_D with time during turn-on. The solid line is for ΔL_{FP} = 0 nm, and the broken line, for ΔL_{FP} = +600 nm.

Fig. 29 shows the change in the power dissipation density $P_{D_t\text{-}on}$ (= $J_D \times V_{DS}$) and the accumulated energy dissipation density $E_{ACC_t\text{-}on}$ with time for ΔL_{FP} of 0 nm and +600 nm during turn-on. The $P_{D_t\text{-}on}$ for ΔL_{FP} = +600 nm is lower than that for ΔL_{FP} = 0 nm in the rising stage of $P_{D_t\text{-}on}$, but it is higher than that for ΔL_{FP} = 0 nm in its falling stage. This characteristic is mainly caused by the above-mentioned higher V_{DS} due to the increased voltage drop in the drift region for ΔL_{FP} = +600 nm, resulting in that $E_{ACC_t\text{-}on}$ for ΔL_{FP} = +600 nm is higher than that for ΔL_{FP} = 0 nm.

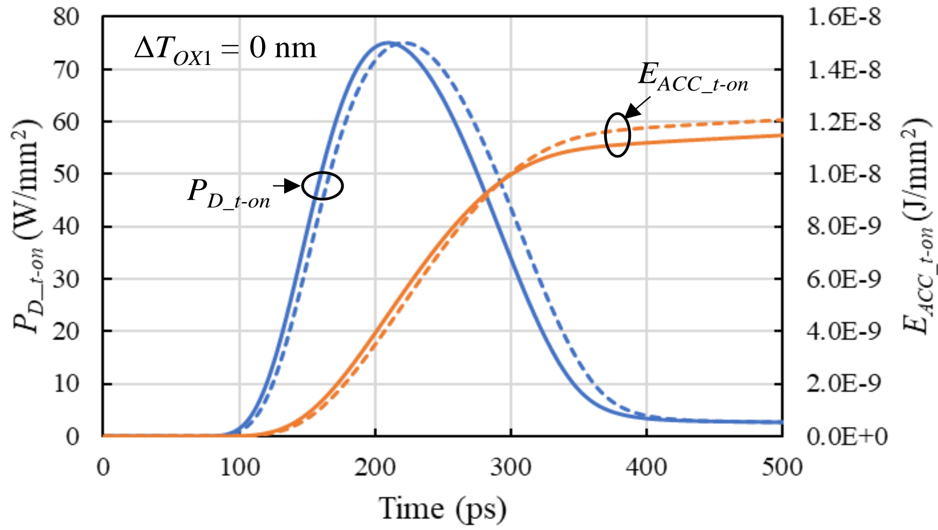

Fig. 29 Change in $P_{D_t\text{-}on}$ and $E_{ACC_t\text{-}on}$ with time during turn-on. The solid line is for ΔL_{FP} = 0 nm, and the broken line, for ΔL_{FP} = +600 nm.

4.2.2 L_{FP} Dependence on Turn-off Characteristics

Fig. 30 shows the change in the V_{DS} and the J_D with time for ΔL_{FP} of 0 nm and +600 nm during turn-off. The J_D for ΔL_{FP} = +600 nm is higher than that for ΔL_{FP} = 0 nm, and the V_{DS} for ΔL_{FP} = +600 nm is lower than that for ΔL_{FP} = 0 nm. The higher J_D for ΔL_{FP} = +600 nm is caused by the higher displacement current density J_{PB}+J_{FP}+J_{Sub} for ΔL_{FP} = +600 nm, where mainly J_{FP} is higher due to the larger C_{FD}. Since the intrinsic MOSFET is in the saturation state from about 320

ps until about 2000 ps, only V_{GS} determines the channel current for that duration. Therefore, the channel current determined by V_{GS} flows from the drain, and the displacement current density $J_{PB}+J_{FP}+J_{Sub}$ adds to the drain current density J_D, resulting in the higher J_D for ΔL_{FP} = +600 nm. The lower V_{DS} for ΔL_{FP} = +600 nm is caused by the shorter current path from the drain to the field plate through the drift region; namely, this short current path decreases the voltage drop in the drift region, resulting in the lower V_{DS}.

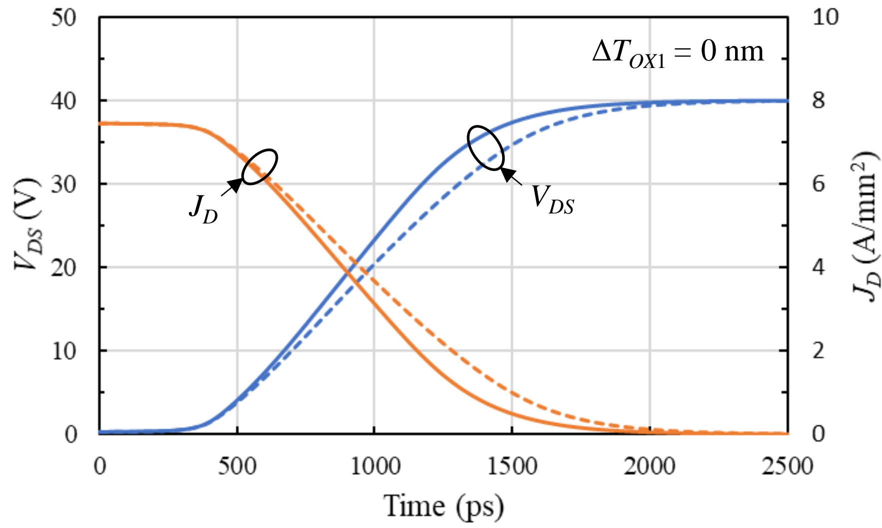

Fig. 30 Change in V_{DS} and J_D with time during turn-off. The solid line is for ΔL_{FP} = 0 nm, and the broken line is for ΔL_{FP} = +600 nm.

Fig. 31 shows the change in the power dissipation density $P_{D_t\text{-}off}$ and the accumulated energy dissipation density $E_{ACC_t\text{-}off}$ with time for ΔL_{FP} of 0 nm and +600 nm during turn-off. The $P_{D_t\text{-}off}$ for ΔL_{FP} = +600 nm is lower than that for ΔL_{FP} = 0 nm in the rising stage of $P_{D_t\text{-}off}$, but it is higher than that for ΔL_{FP} = 0 nm in its falling stage. This characteristic is mainly caused by the above-mentioned higher J_D due to the higher displacement current density $J_{PB}+J_{FP}+J_{Sub}$ for ΔL_{FP} = +600 nm.

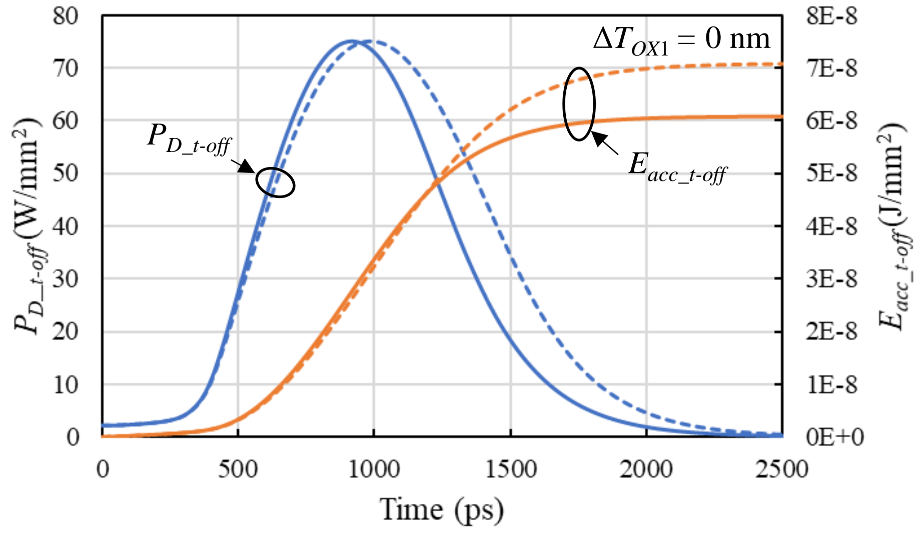

Fig. 31 Change in $P_{D_t\text{-off}}$ and $E_{ACC_t\text{-off}}$ with time during turn-off. The solid line is for ΔL_{FP} = 0 nm, and the broken line is for ΔL_{FP} = +600 nm.

4.2.3 T_{OX1} Dependence on Turn-on Characteristics

The dependence of T_{OX1} on turn-on characteristics is similar to that of L_{FP} on turn-on characteristics. During turn-on(Fig. 32), the J_D for ΔT_{OX1} = –50 nm with a larger C_{FD} is lower than that for ΔT_{OX1} = +50 nm with a lower C_{FD}. This lower J_D is caused by a higher J_{PB}+J_{FP}+J_{Sub} due to the larger C_{FD} under the saturation operation of the intrinsic MOSFET. Here, although the J_{PB}+J_{FP}+J_{Sub} flowing in the drift region raises the V_{DS}, the increment of the V_{DS} is small due to no change in the L_{FP}, resulting in a lower $E_{ACC_t\text{-on}}$ for ΔT_{OX1} = –50 nm(Fig. 33).

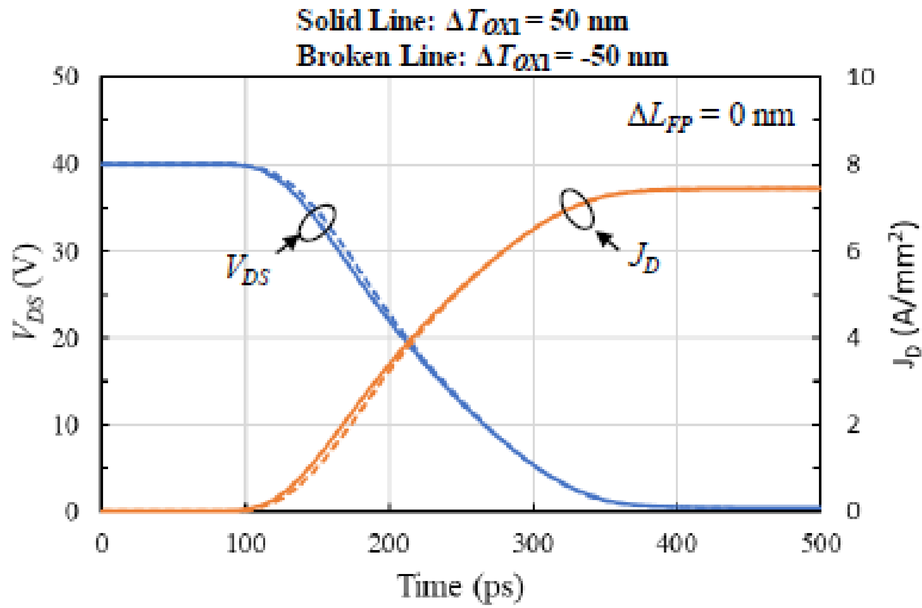

Fig. 32 Change in V_{DS} and J_D with time during turn-on. The solid line is for ΔT_{ox1} = 50 nm, and the broken line, for ΔTox_1 = -50 nm

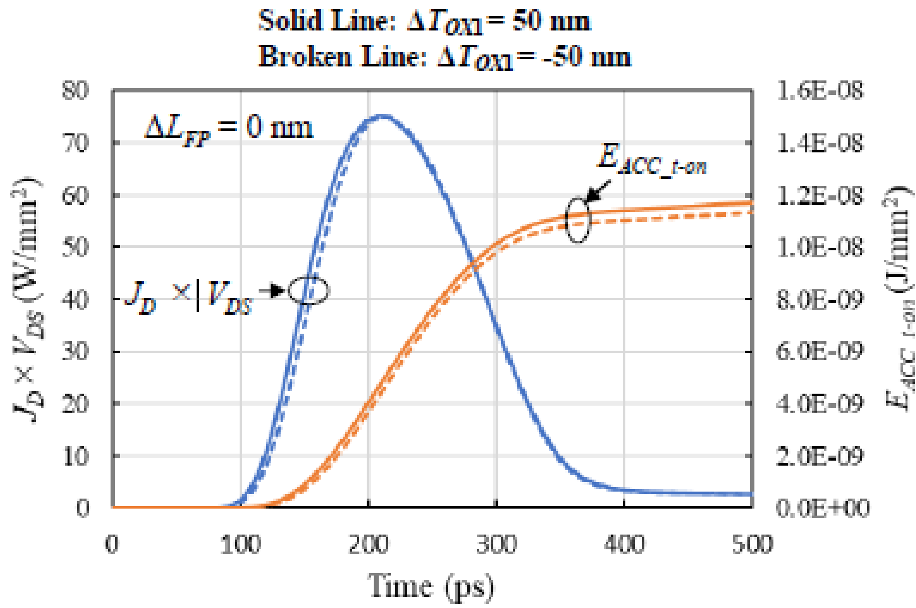

Fig. 33 Change in P_{D_t-off} and E_{ACC_t-off} with time during turn-on. The solid line is for ΔT_{ox1} = 50 nm, and the broken line, for ΔTox_1 = -50 nm

4.2.4 T_{OX1} Dependence on Turn-off Characteristics

The dependence of T_{OX1} on turn-off characteristics is similar to that of L_{FP} on turn-off characteristics (Fig. 34). In the initial stage of the turn-off, the J_D for $\Delta T_{OX1} = -50$ nm is higher than that for $\Delta T_{OX1} = +50$ nm. This higher J_D is caused by a higher $J_{PB}+J_{FP}+J_{Sub}$ due to the larger C_{FD} under the saturation operation of the intrinsic MOSFET. In the latter stage of the turn-off, the J_D for $\Delta T_{OX1} = -50$ nm gradually becomes lower than that for $\Delta T_{OX1} = +50$ nm with time. This change is because the higher V_{DS} in the latter stage causes the drift region-resistance to be higher for $\Delta T_{OX1} = -50$ nm. As a result, $E_{ACC_t\text{-}off}$ for $\Delta T_{OX1} = -50$ nm is slightly lower than that for $\Delta T_{OX1} = +50$ nm(Fig. 35).

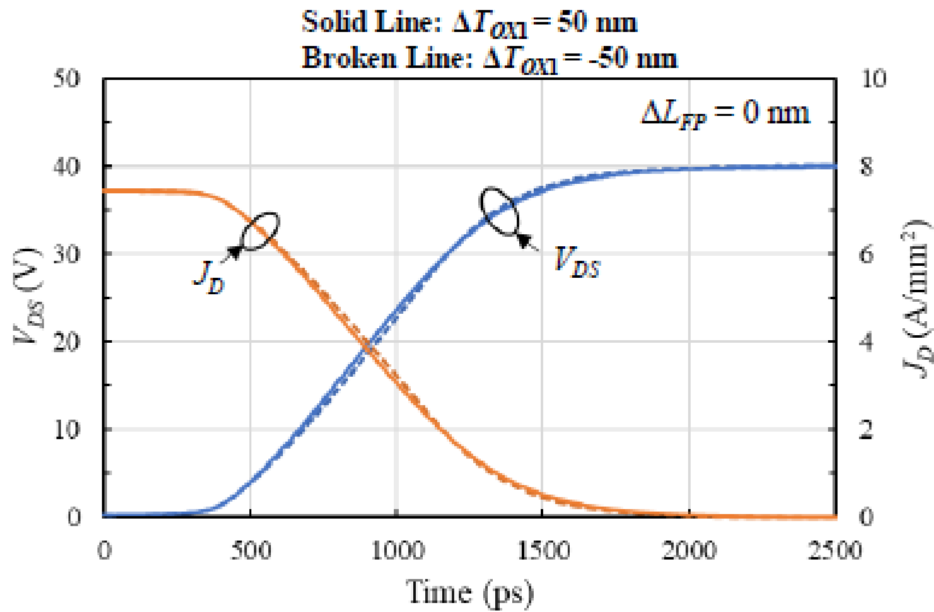

Fig. 34 Change in V_{DS} and J_D with time during turn-off. The solid line is for $\Delta T_{ox1} = 50$ nm, and the broken line, for $\Delta T_{ox1} = -50$ nm

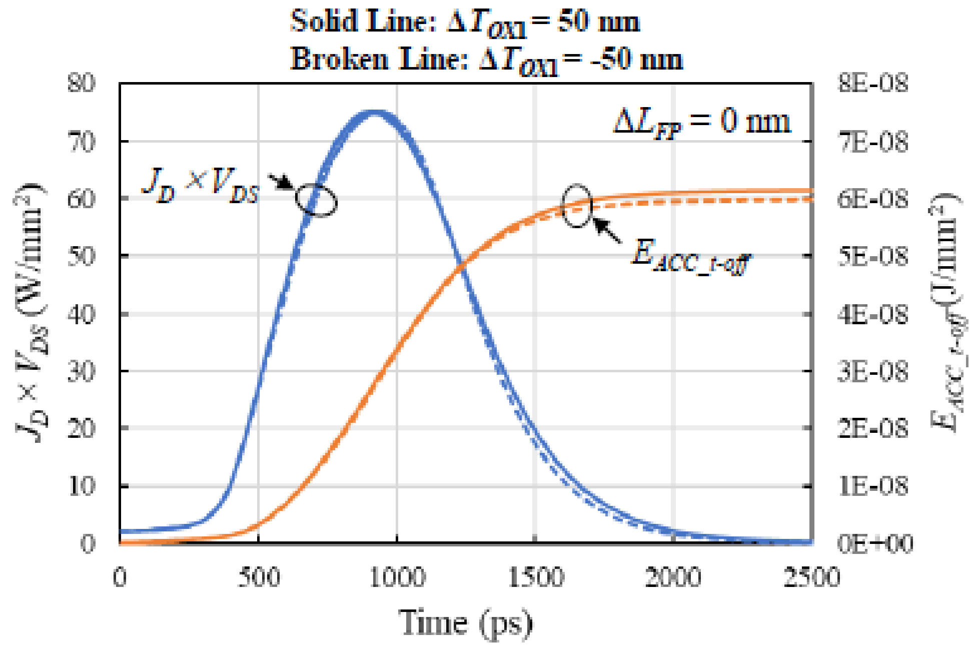

Fig. 35 Change in V_{DS} and J_D with time during turn-off. The solid line is for ΔT_{ox1} = 50 nm, and the broken line, for ΔTox_1 = -50 nm

Chapter 5: Conclusion

We have analyzed the switching characteristics of the proposed device in detail by changing R_L and R_G compared with those of the conventional device. The proposed device has a considerably lower feedback capacitance (C_{GD}), although it has a higher output capacitance (C_D+C_{FD}). Under the actual usage condition, this unique capacitance structure decreases the switching loss of the proposed device compared with that of the conventional device significantly. The lowest value of E_{Loss_P}/ E_{Loss_C} is 0.31 at f = 3 MHz and D_{ON} = 0.1. The proposed device promises drastically low switching loss under the actual use condition. We have also obtained the optimized range of ΔL_{FP} and ΔT_{OX1} for the field plate formation of the proposed 40 V operation N-channel LDMOS transistor to attain BV_{DS} > 60 V with holding low switching loss by simulation. In the range of 0 nm ≤ ΔL_{FP} ≤ 200 nm and −50 nm ≤ ΔT_{OX1} ≤ 0 nm, which satisfy sub-micron process variation tolerance, although the maximum value of E_{T_Loss} goes up 5.4 % from the minimum value, E_{T_Loss} of the proposed device reduces to about 50 % that of the conventional one. Also, since the proposed device has a much lower switching loss even at a high switching frequency than the conduction loss, it realizes buck type and boosts type DC-DC converters with significantly low switching loss for automotive applications. Furthermore, the proposed device may have a high ESD endurance in the optimized range.

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Publication List

[1]. **H.Y. Du**, J. Matsuda, A. Kuwana, and H. Kobayashi, “Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Ground Field Plate,” in Proc. ICTSS, Kiryu, Japan, IPS-02-a (Dec. 2021)

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Award

[1]. **BEST STUDENT PRESENTATION AWARD**

The research entitled “Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Ground Field Plate”, presented by Hao Yang DU at the International Conference on Technology and Social Science 2021 (ICTSS 2021) , held ONLINE on 7-9 December 2021. See Appendix 1.

Appendix 1

ICTSS 2021

CERTIFICATE OF RECOGNITION

Upon diligent deliberation and evaluation based on the predetermined criterion, the Conference Committee is unanimous to recognize as

BEST STUDENT PRESENTATION AWARD

the research entitled

"Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Grounded Field Plate"

authored by

Hao Yang DU, Jun-ichi Matsuda, Anna Kuwana, Haruo Kobayashi (Gunma U)

presented during the International Conference on Technology and Social Science 2021 (ICTSS 2021) held ONLINE on 7-9 December 2021.

Conference General Co-Chair:

Prof. Y. Fujii | Prof. G. Magdaraog Jr. | Prof. S. Serikawa

Appendix 2

1.ビュー画面の上で左ボタンをダブルクリックしてこんなの画面に表示される(図 1)。基板材料を選んで、O ボタンを押す。

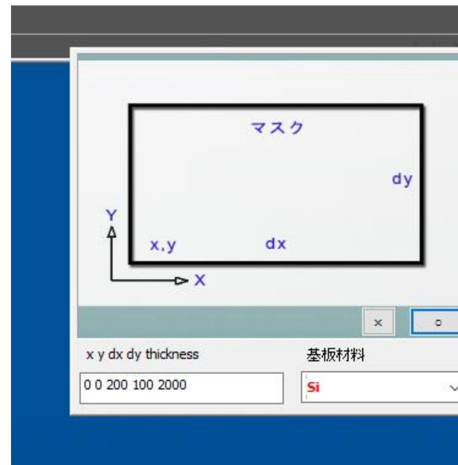

図 1

2.基板にマウスを当て、スペースキーを押すと、その部分の材質が黄色で表示される(図 2)。

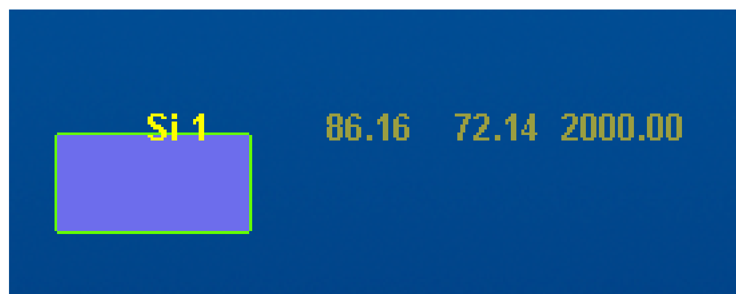

図 2

3.ビューで、モデルの TOP 面を選択する。

4.ルーラ付きのパターン平面が表示される、ダイアログが表示される。（例：SiO_2 を選択して、O ボタンを押す。

5.パターン平面を選択し、このパターン平面上で右クリックを行い、ポップアップメニューを起動し、「膜形成（全面）」を選択する。

6.SiO_2膜が形成される(図 3)。

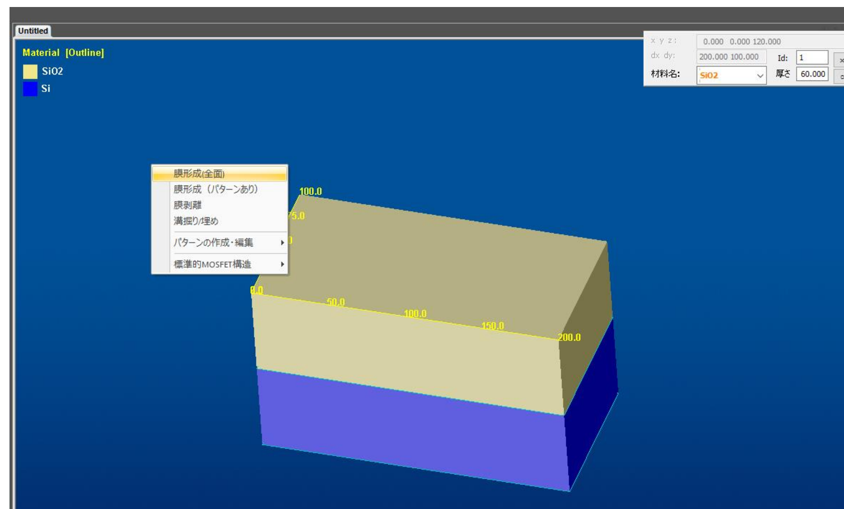

図 3

7.目標パターン平面を選択してから、右クリックして、「標準 MOSFET 構造」「ゲート追加」を選択する(図 4)。

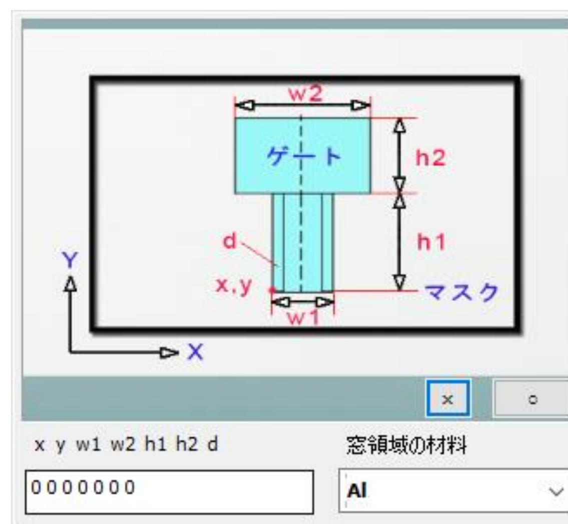

図 4

8.マスクにゲート枠が作成される。

9.パターン平面を選択し、「溝掘り/埋め」を選択する(図 5)。

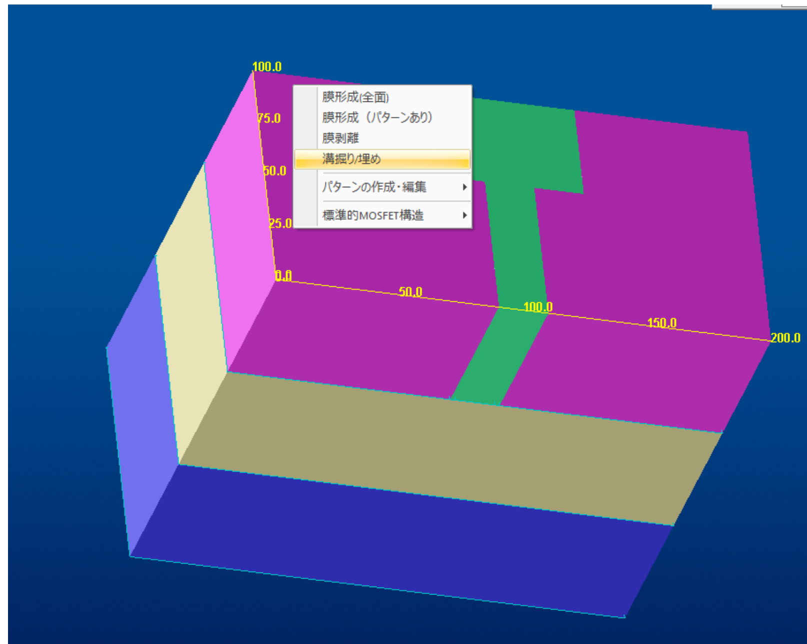

図 5

10.ゲートが作成される。

11.最上面のパターン平面を選択する。これを右クリックして、「標準 MOSFET 構造」「コンタクトビア（S/D）追加」を選択する(図 6)。

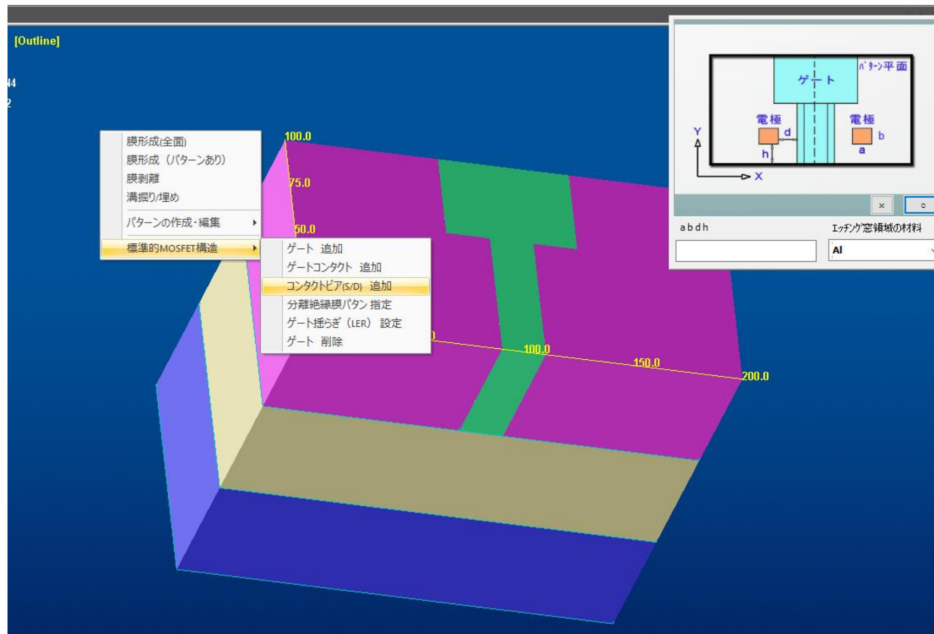

図 6

12.パターン平面にコンタクトビアの枠が作成される。

13.ゲート電極の時と同様に、「溝掘り/埋め」を選択すると、コンタクトビアが作成される(図 7)。

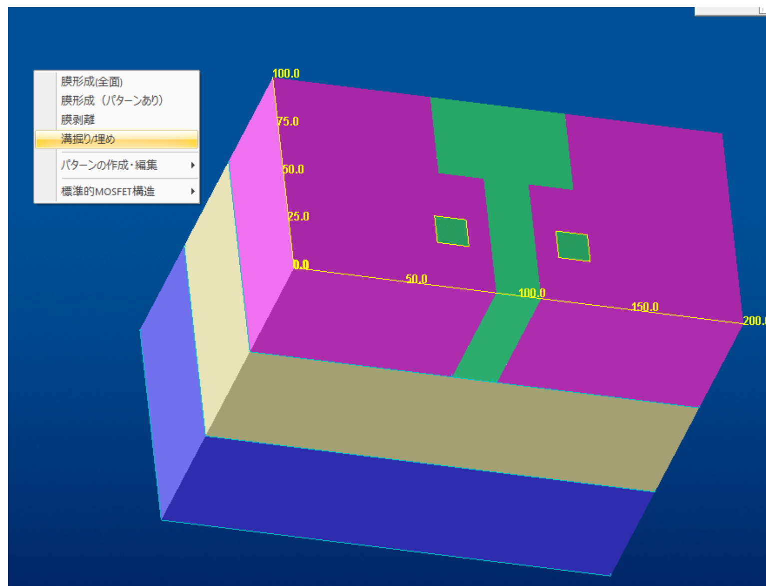

図 7

14.最上面のパターン平面を選択する。これを右クリックして、「標準 MOSFET 構造」「ゲートコンタクト追加」を選択する(図 8)。

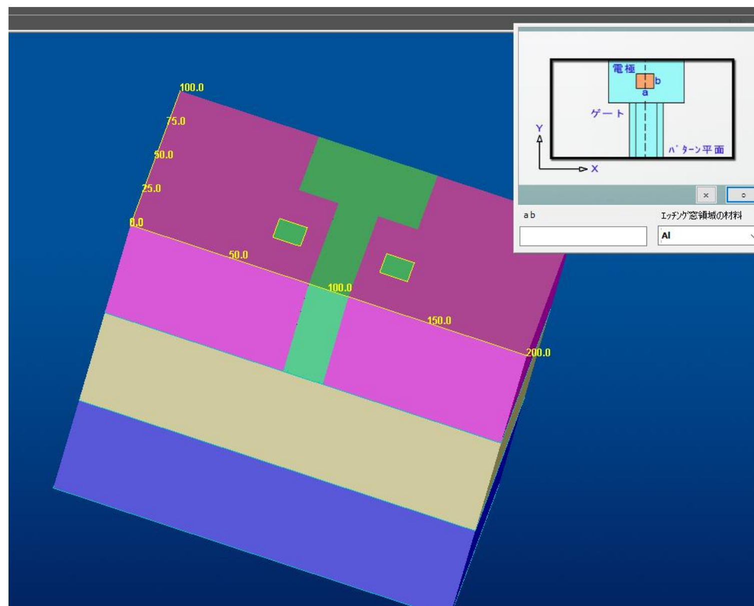

図 8

15.ゲートコンタクトの枠が作成される。

16.同様に、ポップアップメニューを起動し、「膜形成（パターンあり）」を選択すると、最上面と同じ基板材料とともにゲートコンタクトが作成される(図 9)。

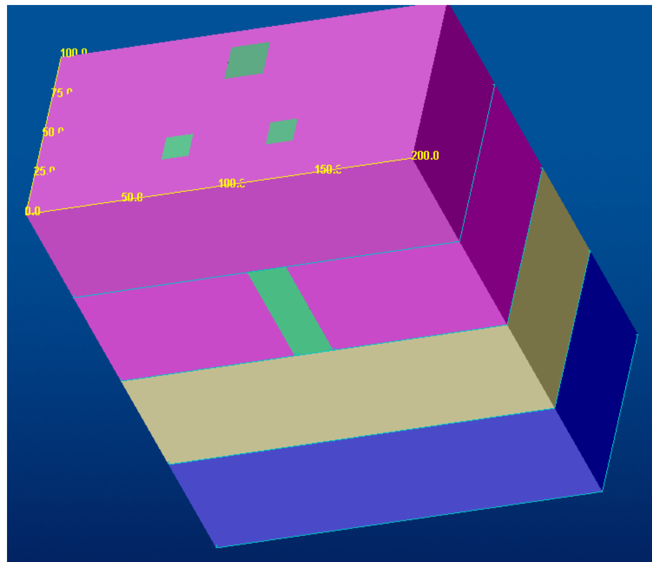

図 9

17.Tree View から、「ドーピング」の項目を右クリックし、「設定ダイアログ」を選択する(図 10)。

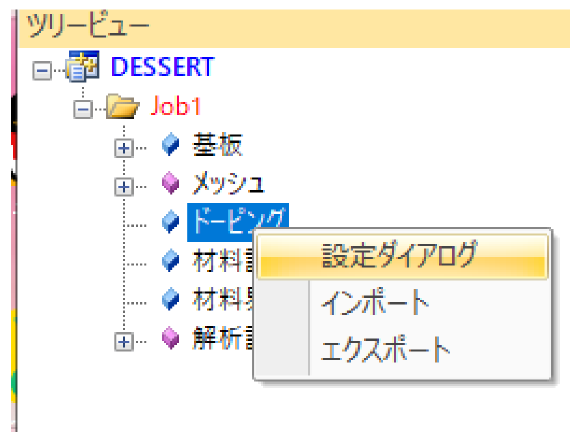

図 10

18.ビューの不純物プロファイルの設定のダイアローグが表示される.

18.不純物：ドーパントを選択する。

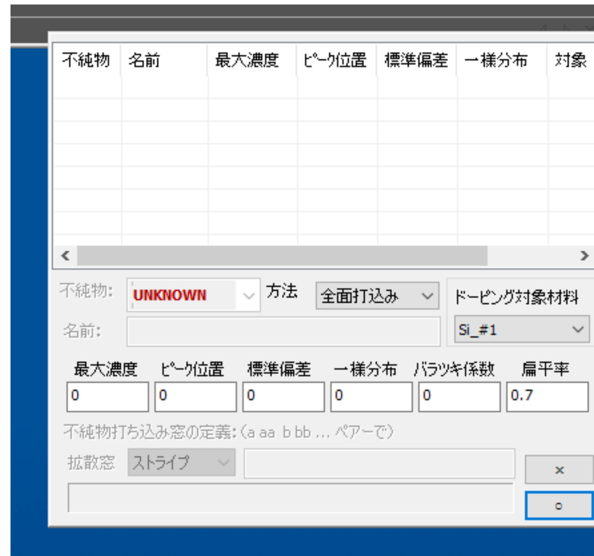

図 11

19.イオン注入領域を選択する。

20.説明欄に内容が重複しないように名前は「1」を入力する。

21.最大濃度，ピーク位置，標準偏差、初期濃度（一様分布）、ばらつき係数を入力する。

22.ドーピング対象を選択する(図 12)。

不純物	名前	最大濃度	ﾋﾟｰｸ位置	標準偏差	一様分布	対象
B	substrate	1.00e+018	10.0	20.000	5.00e+015	21
Sb	sb	1.00e+020	0.0	5.000	0.00e+000	21
As	extension	1.00e+019	0.0	3.000	0.00e+000	21

図 12

23.例、n−channel MOSFET,注入領域は以下のように選択した。B は、全面打ち込み。sb は、サイドウォール。As はゲートマスクである。

24.ドーパントの濃度を、色の変化および、ガウス関数で確認できる。

25.ドーパント合計のプロファイルが表示される。

26.イオン注入設定ダイアログから、各注入イオンをクリックすると、そのイオン飲みの不純物プロファイルが表示される(図 12)。

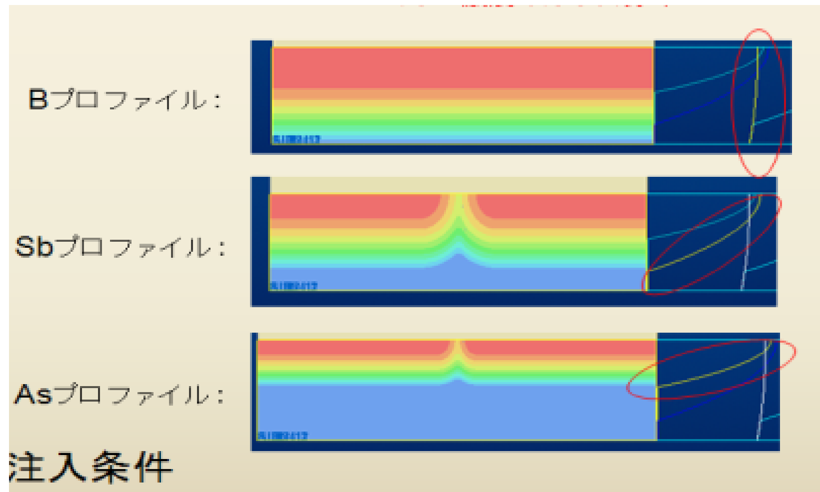

図 12

27.メニューから、ファイル開くをクリックして、「Diode_tese_1.det」をクリックする。

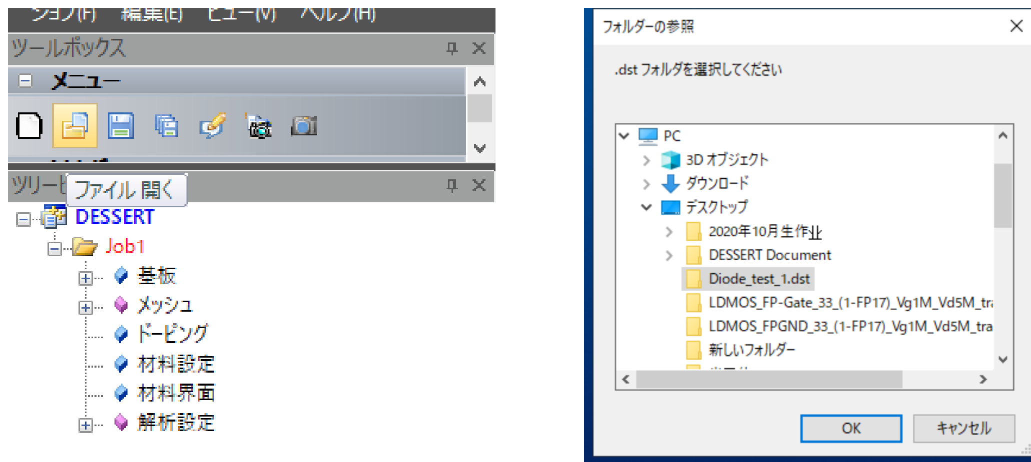

図 13

28.「解析開始」をクリックして、「新規計算」をクリックして、「ok」をクリックする。

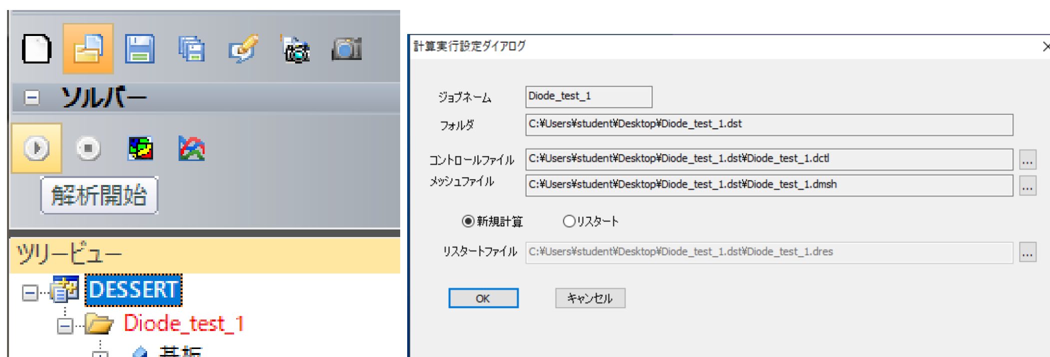

図 14

29.「ソルバー」の下「x—y グラフ」のボタンをクリックする。「Diode_test_1.dst」フアルダの中の「～.div」というファイル指定する。「xlabel」から「Electtode_Al_1-VOLTAGE[V]」。「ylabel」から「Electtode_Al_1-CURRENT[A]」を選択する(図 15.16)。

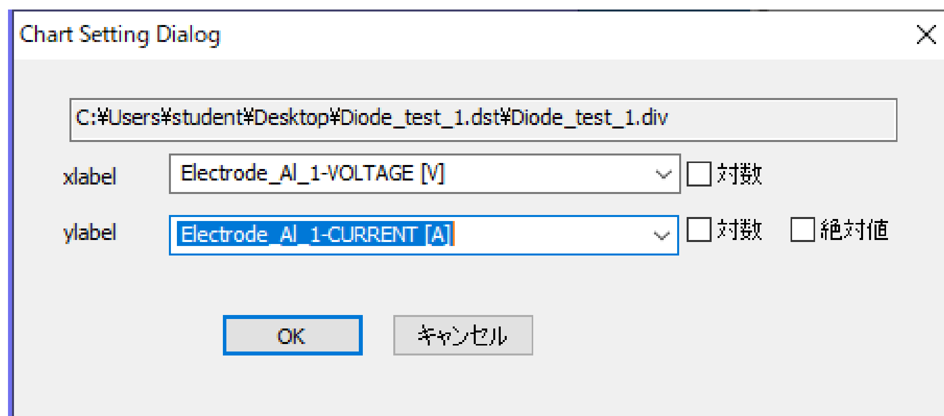

図 15

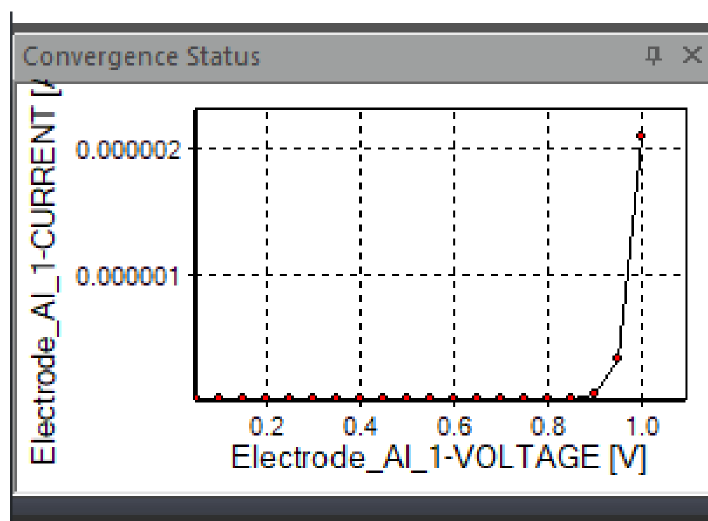

図 16