Histogram Method for ADC Linearity Test: Code Selective Method and Optimal Frequency Ratio

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PhD Dissertation

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DISSERTATION

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Declaration

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Abstract

The histogram approach for the ADC linearity test is the subject of this dissertation. Here, two methods of testing the histogram approach for low cost and high accuracy are proposed. This dissertation describes two improvement technologies in the histogram method for analog-to-digital converter (ADC) linearity test; the first one is the code selective histogram method and the second is selection of the optimal frequency ratio between the input signal and sampling frequencies. The focus of this work is acquiring short time histogram method for ADC linearity test at mass production shipping stage, because test cost is proportional to the test time. Their theoretical analysis and simulation verification are shown.

The first proposal is the code selective histogram method for successive-approximation-register (SAR) ADC with a two-tone sine wave input. The differential non-linearity (DNL) of the codes corresponding to the output voltage of the most significant bits (MSBs) of the internal digital-to-analog converter (DAC) in the SAR ADC under test can be large when the internal DAC employs a binary-weighted configuration. ADC linearity must often be assured around MSB bit (the center code in the histogram data). Histogram ADC testing with the sine wave input takes long time to measure the linearity accurately around the center of the ADC output range, because DNL measurement accuracy is proportional to the number of data samples in the bin. Therefore, to improve the accuracy of the nonlinearity evaluation, the amount of data in the corresponding histogram bin should be increased.

The number of samples at the corresponding amplitude positions (codes) the obtained ADC output data increases with the gentler the slope of the input signal waveform. Therefore, we consider using a two-tone sine wave to make the slope softer at the corresponding amplitude locations. These two-tone sine wave have no inverse function, and hence it is difficult to calculate the probability density function (PDF). However, the histogram method requires the PDF to be known, and then we use PDF obtained by simulation. As a result, the proposed method raises the frequency at which the codes appear in order to make the data amount of the bins relatively large with two-tone sine wave input. It can perform low-cost and high-quality linearity test. Also, we have written a program to test our algorithm, and the

outcomes of our simulations have demonstrated the efficiency and performance of the code selected histogram method.

The second proposal uses classical number theory to decide the ratio of the input signal and sampling frequencies; it uses the metallic ratio or the theory of prime numbers to determine the ratio. The sinusoidal input signal frequency and sampling clock frequency for the histogram method are defined as f_{sig}, f_{CLK}, respectively. We have found that with a limited number of histogram data (in other words, with short test time), accurate test results can be obtained if the sequence distributes pseudo-randomly, and accordingly, the ratio between f_{CLK} and f_{sig} is important. On the contrary, if the selected ratio is not appropriated, the DNL measurement with the histogram is not accurate. We have investigated the histogram method of ADC linearity test with the metallic ratio sampling and prime numbers ratio sampling as well as other ratios, and found that for many cases of the total data number N, the DNL measurement accuracy is good in the metallic ratio and prime number ratios, though the best choice of the metallic ratio and prime numbers depends on N. In many cases of the ADC linearity testing, "f_{CLK} is constant and f_{sig} is varied" and "f_{sig} is constant and f_{CLK} is varied" and if we change their ratio to satisfy the metallic ratio and prime number ratio conditions (which are many), the accurate test result can be obtained with the small number of N.

We have investigated the histogram method for the ADC linearity test which is a mature technology, but still we could have shown their new algorithms and findings in this dissertation that are regarded as being favorable to industry.

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PART 1

Chapter 1 Introduction

1.1 Research Background and Motivation

With the development of digital signal processing and digital computing technology, modern society enjoys life in the "digital" world more and more [1, 2]. Compared with analog circuits, digital circuits have the advantages of being less affected by noise, high reliability, and easier to integrate into chips to realize complex functions. However, the signals touched in the real world are analog signals such as sounds and images. Therefore, as an interface between an analog signal and a digital signal in a circuit, it is necessary to realize the process of converting the analog signal into a digital signal conveniently. The circuit that realizes this function is an A/D Converter (Analog-to-Digital Converter, ADC) [3].

For IoT-related ADCs high quality and rapid linearity testing has become more important at mass production shipping stage for keeping IoT system’s quality and reliability, with the attention of the Internet of Things (IoT) in recent years.

The histogram method for ADC linearity test is widely used in industry [4-11]. Unfortunately, the histogram test is often omitted at the mass production shipping stage due to the relatively long time it takes. However, ADC linearity test is required due to recent demands for higher reliability in IoT systems and automotive applications, but low-cost test is essential.

Various methods for test time reduction of ADC linearity test have been proposed [12, 13]. Chen et al. proposed the segmented non-parametric model, a model-based method [14, 15]. Laraba et al. proposed reduced-code linearity test for pipeline ADC [16]. This method reduces the static test time utilizing the fact that there exist different output transitions between consecutive codes that are due to the same comparator being exercised in one of the pipeline stages [17]. Regarding to SAR ADC linearity test, Feitoza et al. proposed reduced-code linearity tests for the different DAC architectures [18, 19]. These methods perform major code transition (MCT)-based test methodology with extra behaviors for the test. Huang et al. also proposed an MCT test-based approach characterizing the static linearity of a capacitive SAR ADC [20]. These methods for SAR ADC require extra area for extra behavior for the on-chip BIST implementation. On the other hand, because our method is histogram test-based approach, extra hardware is not required

The code selective histogram method and choosing selection of the optimal frequency ratio between the input signal and sampling frequencies are the two advancements in the histogram method for ADC linearity test that are covered in this dissertation. Because test cost is proportional to test time, the purpose of this work is to acquire a short time histogram method for ADC linearity test at mass production shipping stage. Their theoretical analysis and simulation verification are shown.

1.2 Organization

The research background and motivation are introduced and dissertation organization in Chapter 1. In Chapter 2, the AD conversion principle, the evaluation criteria for ADCs, and the structure and application scenarios of different ADCs are introduced. Chapter 3 proposes that the two-tone sine wave input for code selective histogram method, which is the first proposal. Chapter 4 presents decision of the ratio between input and sampling frequencies based on classical number theory, which is the 2nd proposal. Chapter 5 summarizes this part and future work.

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Chapter 2 ADC&DAC and Performance Index

A digital-to-analog converter's (DAC) or analog-to-digital converter's (ADC) fundamental operation can be divided into a series of simple elementary steps. An ADC is depicted as a cascade of four functions in Fig. 2.1: continuous time anti-aliasing filtering, sampling, quantization and data coding.

The DAC performs two basic functions: a transcoding stage, which converts the digital input into an equivalent analog signal, and a reconstruction stage. We shall see that a sampled-data analog signal's high-frequency component are taken out using the reconstruction method. Reconstruction is performed in two steps as shown in Fig. 2.2: a sample-and-hold followed by a low-pass reconstruction filter.

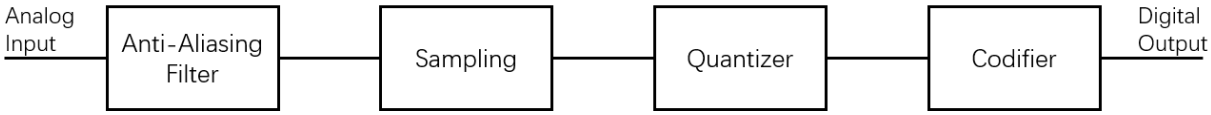


Fig. 2.1 Block diagram of the basic functions of an ADC.

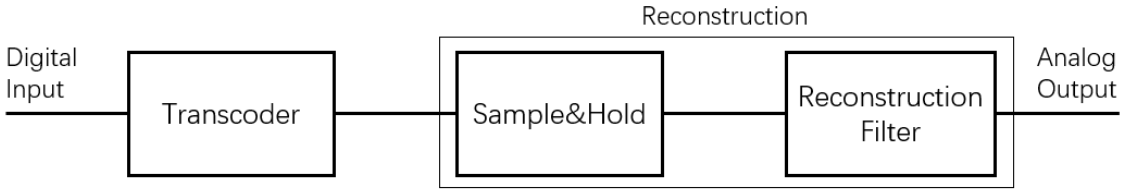


Fig. 2.2 Block diagram of the basic functions of a DAC.

2.1 Sampling

To ensure that the ADC works properly, it is necessary to understand the frequency response characteristics of the ADC. Suppose a frequency response of the analog input signal, and the maximum frequency of the analog input signal is f_B. Then when the analog input signal is sampled at a frequency of f_S, and the spectrum of the input signal is repeated at the sampling frequency as well as at each of its harmonics. If the signal bandwidth f_B is larger than $0.5f_S$, the spectrum will be mixed, and there it is impossible to recover the original signal. Therefore, it must be ensured that the input signal bandwidth is less than $0.5f_S$.

As described above is the basic law of sampling, called sampling theorem [1], which describes that the sampling frequency must be more than twice the bandwidth of the input signal to guarantee the recovery of the original signal from the sampled signal, that is what the sampling frequency f_S must satisfy:

$$2f_B < f_S \tag{2-1}$$

Where f_B is the high frequency component of the input signal. In order to maximize the spectrum of the input signal, it is necessary to make f_B as close as possible to $0.5f_S$, so that a pre-filter with very steep variations is required to eliminate the signal outside the $0.5f_S$ frequency, and it is very difficult and complicated to implement such a filter. The sampling frequency is usually taken as:

$$f_S \cong (2\sim3)\, f_B \tag{2-2}$$

The Nyquist sampling theorem shows the correlation between sampling frequency and signal frequency, and ADCs that work in this way are called Nyquist ADCs. There is also another ADC with a sampling frequency much higher than two times the signal bandwidth, called an oversampling ADC.

2.2 Quantization Noise

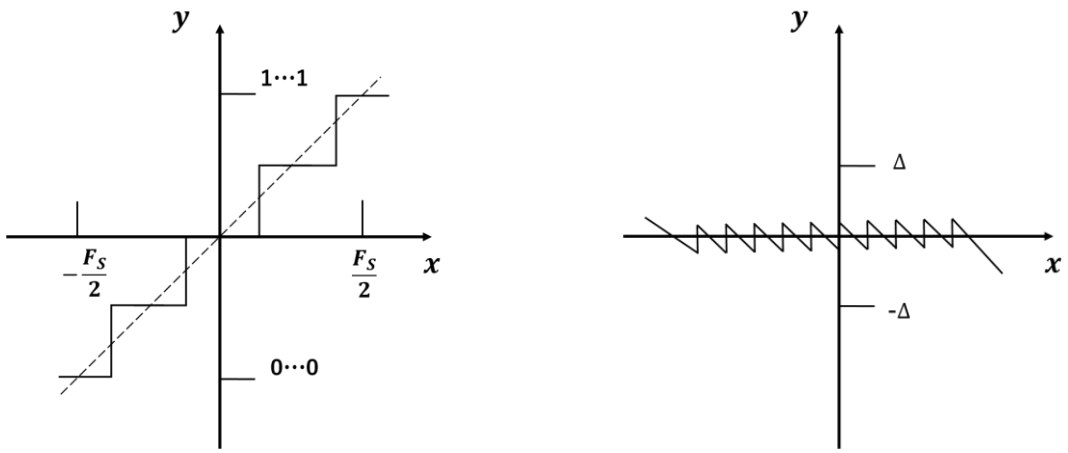
Fig. 2.3 (a) shows the input-output curve of the quantizer, which converts the input sample signal $x(n)$ into a discrete digital signal of amplitude $00\cdots0$ to $11\cdots1$, depending on the input size. Use up to N-bit digital signal. It means that the minimum input is $-F.S./2$ $(00\cdots0)$ and the maximum input is $+F.S./2$ $(11\cdots1)$. Here, $F.S.$ is the full-scale input of the quantizer. The number of N-bit in the digital signal, represents the resolution of the quantizer. The number of N-bit of the digital signal represents the resolution of the quantizer. That is, the minimum step size that the quantizer can decompose is $\Delta = F.S./2^N$. The quantization error is the difference between the input and the output, and the relationship between the input signal and the quantization is shown in Fig. 2.3(b), where the quantization error is limited to the range $[-F.S./2 \sim +F.S./2]]$ when the input signal size is limited to the range $[-\Delta/2 \sim +\Delta/2]$. Under certain conditions, such as random fluctuations of the input signal or limited input range, the quantization error can be regarded as uncorrelated random white noise, evenly distributed in $[-\Delta/2 \sim +\Delta/2]$. The Probability Density

Function (PDF) is shown in Fig. 2.4(a). The total quantization noise energy can be calculated as follows:

$$\sigma_q^2 = \int_{-\infty}^{\infty} PDF(q)dq = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \tag{2-3}$$

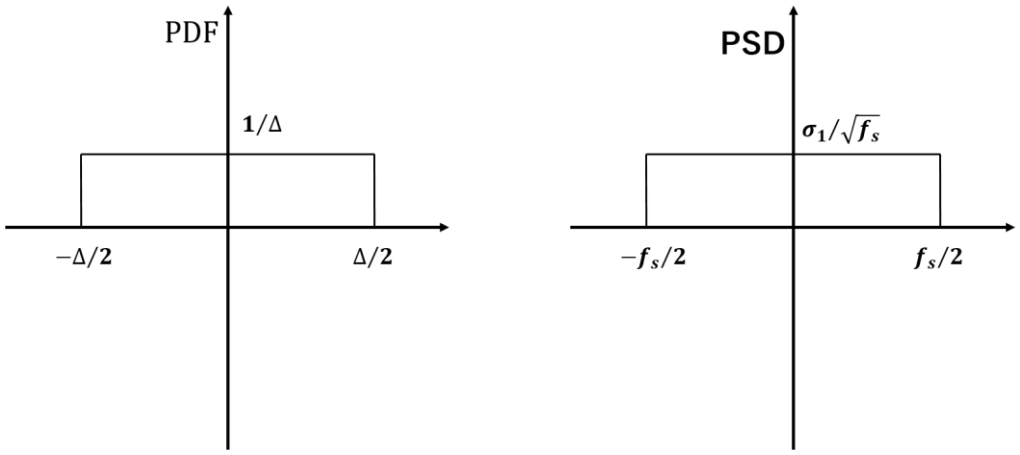
Its Power Spectral Density (PSD) is white noise evenly distributed in frequency domain over $[-f_s/2\ ,\ f_s/2]$ as shown in Fig. 2.4(b), its amplitude is $\Delta/\sqrt{12f_s}$, and the total noise energy is also obtained by integrating the PSD from $[-f_s/2\ ,\ f_s/2]$.

$$\sigma_q^2 = \int_{-f_s/2}^{f_s/2} \left(\frac{\Delta}{\sqrt{12f_s}}\right)^2 df = \frac{\Delta^2}{12} \tag{2-4}$$



(a) Quantized input/output. (b) Quantized noise.

Fig. 2.3 Quantization.



(a) Probability Density Function. (b) Power Spectral Density.

Fig. 2.4 Quantization noise.

2.3 ADC&DAC Main Structure

Nowadays, converters have been widely used in various types of System-on-Chips (SoCs), and the requirements of converter vary from application system to application system. In order to adopt to the application requirements of different SoCs, following structure types of ADCs have emerged during their continuous development.

(1) Flash type

For an n-bit flash ADC, $(2^n - 1)$ comparators are prepared for conversion as shown in Fig. 2.5. For example, if A/D conversion is performed from 0V to 15V at 1V intervals to obtain a 4-bit output, 15 comparators from 1V to 15V are prepared and compared with the input, encode their output to binary if necessary.

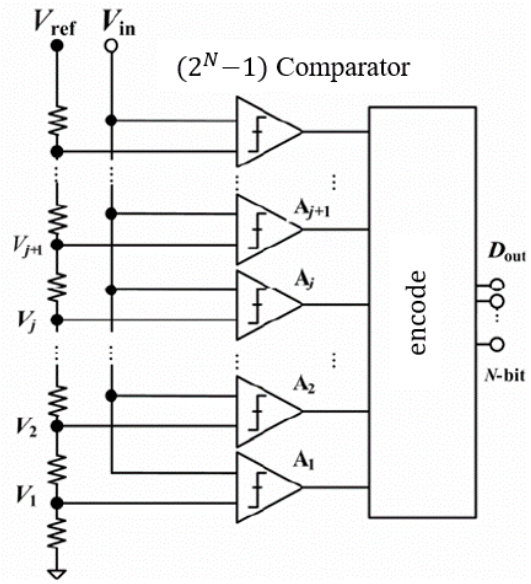


Fig. 2.5 Flash ADC structure.

(2) SAR Type (Successive Approximation Register)

The output of an accurate n-bit DAC is the reference for 2^n voltages. In other words, n-bit A/D conversion can be realized by comparing the DAC output with the input voltage. One comparison can increase the precision by 1 bit, so in the case of n bits, the result can be obtained with n comparisons as shown in Fig. 2.6.

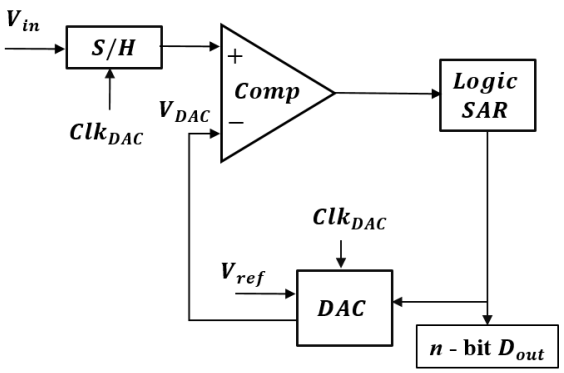


Fig. 2.6 SAR ADC structure block diagram.

(3) Pipeline Type

The pipeline type is close to SAR type. The SAR type is a method of repeatedly using a comparator for n comparisons to approximate an accurate value. The pipeline type is processed in an n-stage circuit configuration like pipeline processing. Fig. 2.7 shows pipeline ADC structure block diagram

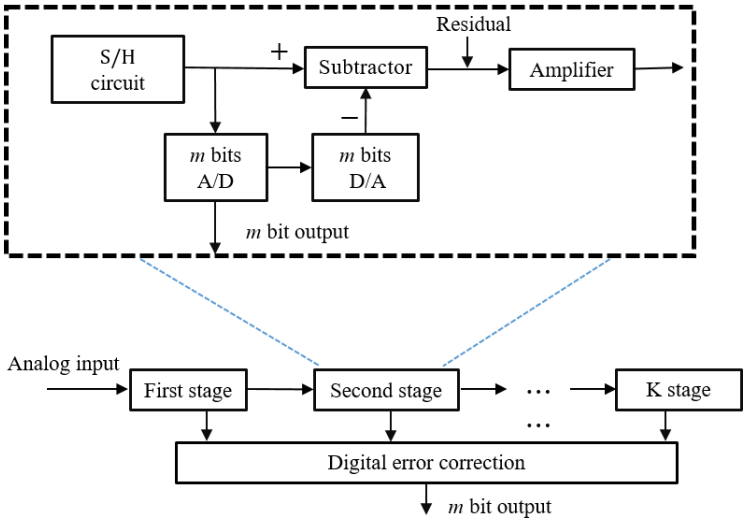


Fig. 2.7 Pipeline ADC structure block diagram.

(4) Integrating Type

First, the input voltage is integrated for a certain period of time. After that, integrate with the reference voltage of opposite sign, and measure the time until integrated value becomes 0 as shown in Fig. 2.8. Thereby, the ratio of input voltage and reference voltage can be measured as a ratio of time.

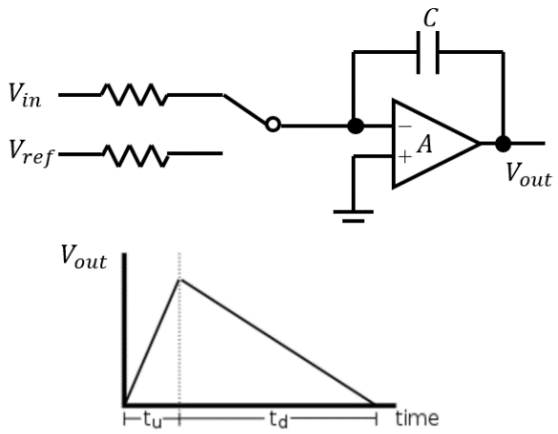


Fig. 2.8 Enhanced run-up dual-slope integrating ADC

(5) Delta-Sigma Modulator Type

The input is AD-converted by 1 bit, and this result consists of columns of +1 and -1. However, since the quantization error is accumulated by the integrator, a string of values that differ from the values obtained by simply converting the input to 1-bit AD appears. If the input changes slowly, for example, if the input is 0V, +1 and -1 are alternately output almost the same number of times, and if the voltage is high, +1 will be output more often. Output proportional to voltage. In other words, a kind of dithering is performed. If the number of +1 and -1 is counted for m steps, AD conversion of the number of bits corresponding to it is performed.

Then there are various structure types of DACs used in industry.

(1) Resistor String Type

In the case of n bits, all 2^n corresponding voltages can be obtained by dividing the reference voltage by connecting 2^n resistors in series as shown in Fig. 2.. Among them, the voltage point corresponding to the digital input is connected by an analog switch and output.

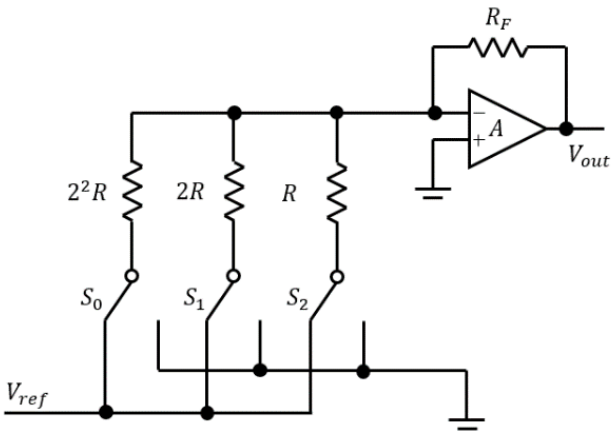


Fig. 2.9 3-bit Resistor string type structure

(2) R-2R Ladder Type

The target voltage is obtained from the ON/OFF of the resistance and the voltage application using the operation function of the operational amplifier. The one with the R-2R ladder type resistance circuit as shown in Fig. 2.10 is popular.

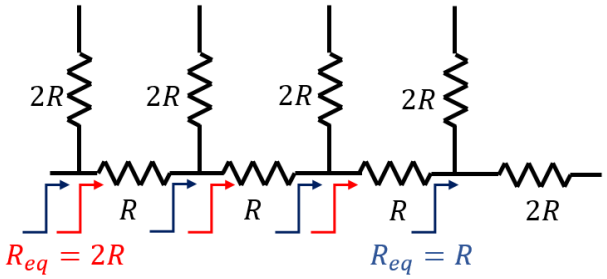


Fig. 2.10 R-2R ladder structure

(3) Current Switching Type

Resistors weighted according to bits are connected to parallel via switches as shown in Fig. 2.11. If a constant voltage is applied here, the total amount of current will be the sum of the currents flowing through the resistors turned on by the switches, resulting in a current proportional to the binary value.

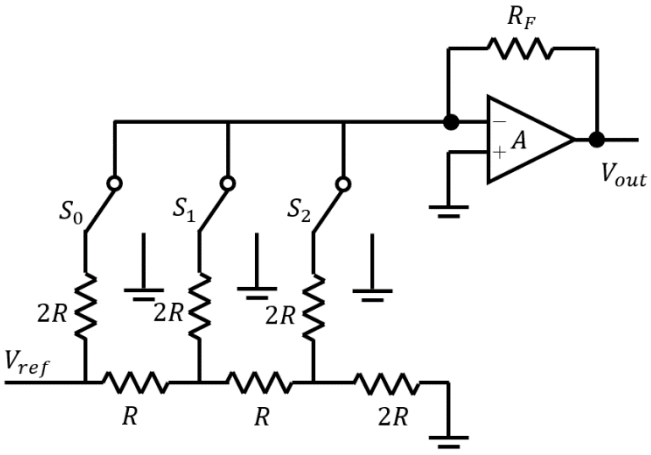


Fig. 2.11 3-bit Current switching type structure

(4) Capacity Switching Type

As a type that also uses binary weighting, charge capacitors weighted according to bits and measure the overall voltage as shown in Fig. 2.12.

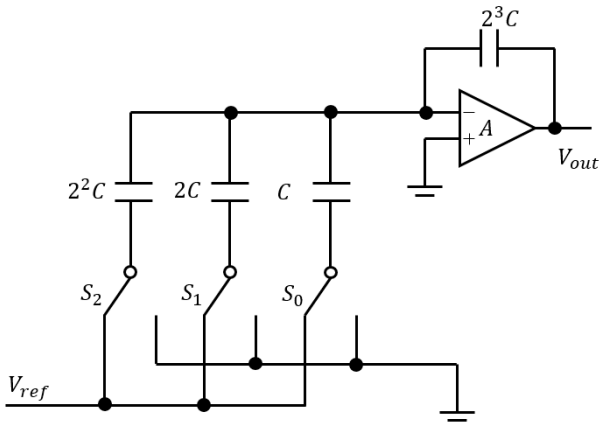


Fig. 2.12 3-bit Capacity switching type structure

(5) Delta-Sigma Modulator Type

Complementing the digital input in the time direction to increase the sampling frequency several tens of times (oversampling). This output is passed through a delta-sigma modulator to generate low-bit oversampled data. The purpose of the delta-sigma modulator is the same as for analog-to-digital conversion, but the high-bit digital input is digitally processed into a low-bit " dithered " digital output. A 1-bit output would result in an output similar to pulse width modulation, but a delta-sigma modulator would result in a better pulse shape. This low bit output is DA converted (in the case of 1 bit, it can be left as it is if the output power is sufficient), Similar to the pulse

width modulation type, the signal is passed through a low-pass filter to eliminate alias noise components and quantization error components, resulting in an analog output.

2.4 Performance Indicators

2.4.1 Dynamic Characteristics of ADC

The dynamic characteristics of an ADC are generally obtained by Fast Fourier Transform (FFT) analysis, which is related to the input frequency, input signal amplitude, and sampling frequency, and they are measured by Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SNDR), Effective Number of Bits (ENOB), Spurious-Free Dynamic Range (SFDR), and Total Harmonic Distortion (THD), etc.

(1) SNR: Signal-to-Noise

The noise effect is quantified by the signal-to-noise ratio (SNR). It refers to the ratio of the signal power to the noise power in the signal band. The signal-to-noise is given by the following formula:

$$\mathrm{SNR|dB} = 10log_{10}\frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}}} \tag{2-5}$$

where P_{signal} and P_{noise} are the signal power and the noise power in the band of interest, respectively.

In sine wave or triangular input case, it is calculated for an n-bit ADC as follows:

$$\mathrm{SNR}_{sine}|\mathrm{dB} = (6.02n + 1.76)[\mathrm{dB}] \tag{2-6}$$

$$\mathrm{SNR}_{trian}|\mathrm{dB} = (6.02n)[\mathrm{dB}] \tag{2-7}$$

Every bit (n) of resolution improves the SNR by 6.02 dB. Also, the power of the quantization noise diminishes by a factor of 4 for every additional bit. The above SNR calculation only accounts for the quantization noise. In real circuits the electronic noise of passive and active components brings about additional noise.

(2) SNDR: Signal-to-Noise and Distortion Ration

The signal distortion ratio refers to the ratio of the output signal power to the sum of all noise and harmonic power in the band, which is simply the ratio of the output signal power to the output non-signal power. It can be expressed as follows:

$$\mathrm{SNDR} = \frac{P_{signal}}{P_{noise} + P_{distortion}} \tag{2-8}$$

Where, P_{signal} is the signal power, P_{noise} is the noise power and $P_{distortion}$ is the total harmonic power.

(3) ENOB: Effective Number of Bits

The number of valid bits refers to the effective number of bits corresponding to the SNDR obtained by the ADC output at full scale input signal, with the following conversion relationship:

$$\mathrm{ENOB} = \frac{SNDR[dB] - 1.76}{6.02} \tag{2-9}$$

(4) SFDR: Spurious-Free Dynamic Range

The Spurious-Free Dynamic Range (SFDR) is defined as the ratio of the energy of the fundamental component to the maximum spurious component in the output signal of the ADC, which reflects the maximum interference to the output signal of the ADC in a certain frequency band. For a certain input frequency, the input amplitude and the sampling frequency, the SFDR can be expressed as:

$$\mathrm{SFDR} = 20\log_{10}\frac{\mathrm{A_s}}{\mathrm{A_{spr(max)}}}[\mathrm{dB}] \tag{2-10}$$

Where, $\mathrm{A_s}$ denotes the effective value of the fundamental wave component of the ADC output signal under a certain sinusoidal input condition, $\mathrm{A_{spr(max)}}$ denotes the effective value of the maximum spurious signal output of the ADC.

(5) THD: Total Harmonic Distortion

Total Harmonic Distortion (THD) is defined as the ratio of the harmonic component of the ADC output signal to the energy of the fundamental signal and it can be expressed as:

$$\mathrm{THD} = 20\log_{10}\left(\frac{\sqrt{A_{HD2}^2 + A_{HD3}^2 + \cdots + A_{HDk}^2}}{A_s}\right) \tag{2-11}$$

Where, A_s denotes the effective value of the fundamental component of the ADC output signal, and A_{HDk} denotes the effective value of the kth harmonic in the output signal, k = 2, 3, ⋯, m. Since the energy of the higher harmonic components is usually smaller, m = 6 is generally taken.

2.4.2 Static Characteristics of ADC

The static performance index of the ADC is the performance index that can be measured at low frequency input or even fixed voltage input, which includes Differential Non-linearity (DNL), Integral Non-linearity (INL), Missing Code, Monotonicity, Offset Error, Gain Error, and so on. These parameters reflect the deviation of the actual quantization curve of the ADC from the ideal curve.

One very important parameter for the ADC is the Least-Significant Bit (LSB). LSB is the lowest weighted bit of the ADC digital output code, which usually corresponds to the analog value it represents. Any ADC is limited in its ability to recognize an analog input, and the metric that characterizes this

ability is the resolution (also called precision), which can be expressed as a percentage of the ADC's full scale, or as the number of N bits, when the ADC has 2^N possible digital output codes. The LSB, resolution and ADC Full Scale Input Range (FSR) are related by the following equation:

$$1\text{LSB} = \frac{FSR}{2^N - 1} \cong \frac{FSR}{2^N} \tag{2-12}$$

Where the 1 in the denominator is not required for differential ADCs.

Corresponding to the LSB, the Most Significant Bit (MSB) refers to the highest bit of the ADC digital output code, which is generally half of the FSR.

(1) DNL: Differential Non-linearity

The ideal quantization curve digital code conversion width (the difference between two adjacent conversion levels) of the ADC is 1 LSB. DNL reflects the deviation of the actual quantization curve digital code conversion width of the ADC from the ideal value of 1 LSB as shown in Fig. 2.13.

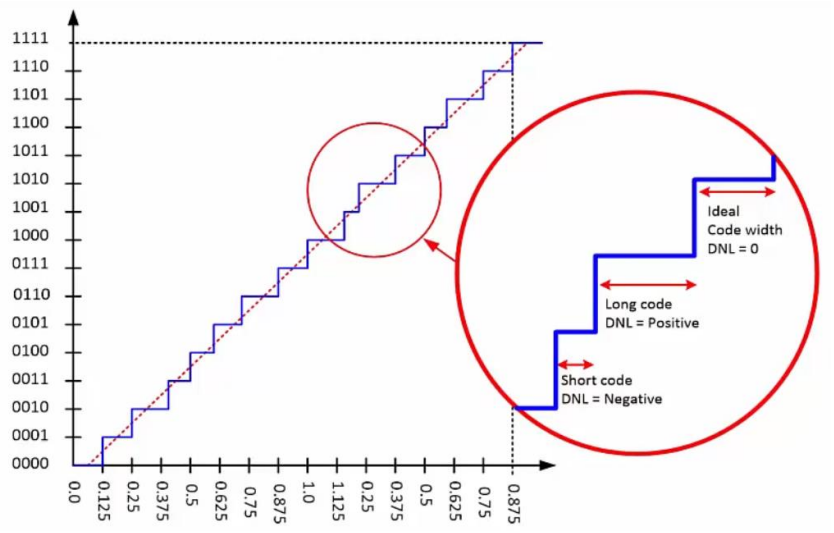


Fig. 2.13 DNL and ideal code width

(2) INL: Integral Non-linearity

All the conversion levels of the ideal quantization curve of the ADC are located at a straight line, while the actual quantization curve is not. INL reflects the deviation between the actual conversion level of the ADC and the ideal conversion level as shown in Fig. 2.14. For a certain digital output code M, its corresponding INL and DNL have the following relationship:

$$\mathrm{INL}(M) = \sum_{i=0}^{M} \mathrm{DNL}(M) \tag{2-13}$$

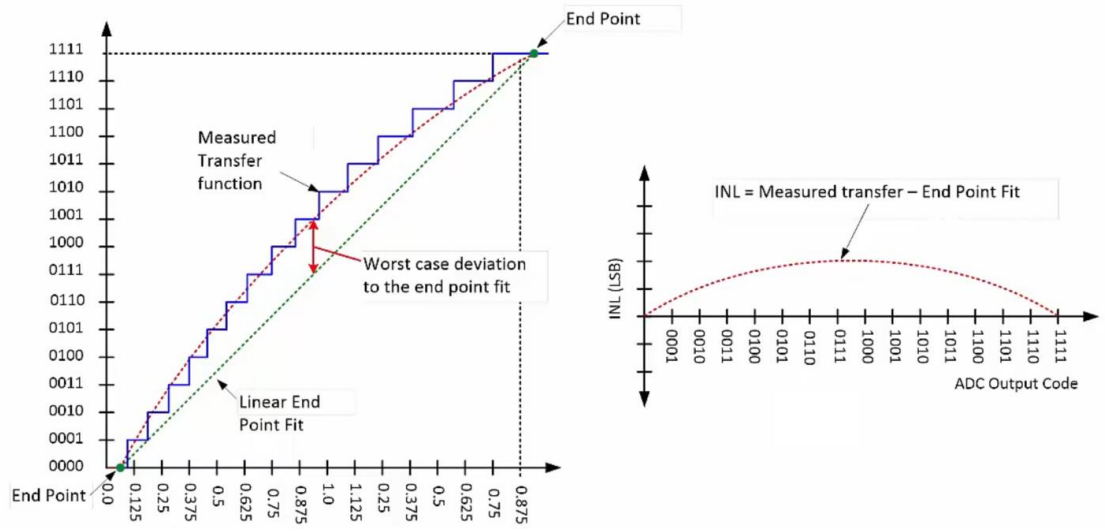


Fig. 2.14 INL and ideal conversion line

(3) Missing code

If the ADC always has a certain (or some) digital code that cannot be generated regardless of the input voltage, it is said that the ADC has missing codes as shown in Fig. 2.15. If there is a missing code, it means that the ADC appears $\mathrm{DNL} = -1$.

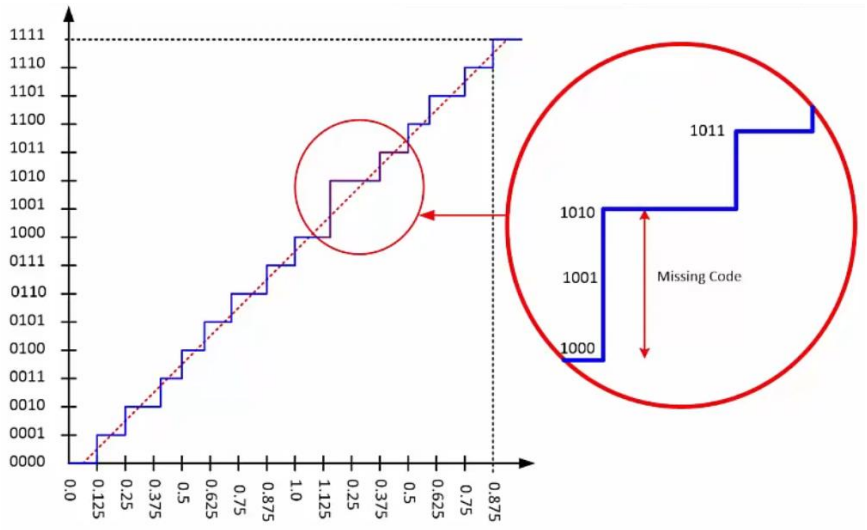


Fig. 2.15 Missing code

(4) Monotonicity

Normally, each vertical step of the ADC quantization curve is positive (one digital code pitch), which means that the magnitude of the digital output code varies in the same direction as the amplitude of the input signal. If the quantization curve of the ADC has a negative jump in the vertical direction, the ADC has non-monotonic characteristics. Non-monotonicity worsens quantization noise and, if present in a closed-loop system, affects system stability [2-4].

(5) Offset error

The first conversion level of the ideal quantization curve of the ADC (the input analog voltage when the digital output code jumps from $00\cdots0$ to $00\cdots1$) is 0.5 LSB, and the offset error of the ADC is defined as the deviation of the first conversion level of the actual quantization curve from

0.5 LSB.

(6) Gain error

The gain error reflects the deviation of the slope of the actual quantization curve of the ADC from the slope of the ideal curve, and it is often expressed in terms of the full-scale gain error, namely shifting the actual quantization curve so that its lowest conversion level is aligned with the lowest conversion level of the ideal curve, and then comparing the deviation of the actual quantization curve with the highest conversion level of the ideal curve.

2.5 Testing of ADC and DAC

2.5.1 Best-fit-line

The best-fit-line of the ADC input-output characteristics uses a sequence of n digital data Y_i, $i = 1, \cdots, n$ generated by linear input signals covering the entire dynamic range. The analog output of a DAC is converted to digital data using linear inputs that, like in the case of an ADC, cover the entire dynamic range.

The fitting line is

$$\hat{Y}(i) = G \cdot i + Y_{os} \tag{2-14}$$

where G is the gain and Y_{os} is the offset of the data converter.

The least squares method minimizes the summed square of residuals that for the i-th data point is the difference between the measured response value Y_i and the fitted response value $\hat{Y}_i$

$$r_i = Y_i - \hat{Y}_i \tag{2-15}$$

The summed square of residuals is

$$S = \sum_1^n {r_i}^2 = \sum_1^n [Y_i - (G \cdot i + Y_{os})]^2 \tag{2-16}$$

The minimum of S in the coefficients space requires that the partial derivatives of S equal to zero

$$\frac{\partial S}{\partial G} = -2 \sum_1^n i \cdot [Y_i - (G \cdot i + Y_{os})] = 0 \tag{2-17}$$

$$\frac{\partial S}{\partial Y_{os}} = -2 \sum_1^n [Y_i - (G \cdot i + Y_{os})] = 0 \tag{2-18}$$

that, using the values

$$S_1 = 2 \sum_1^n i \, ; S_2 = 2 \sum_1^n Y_i \, ; S_3 = 2 \sum_1^n i^2 \, ; S_4 = 2 \sum_1^n i Y_i \, ; \tag{2-19}$$

as intermediate variables, yields

$$G = \frac{nS_4 - S_1S_2}{nS_3 - {S_1}^2}; Y_{os} = \frac{S_2}{n} - G\frac{S_1}{n} \tag{2-20}$$

which are the gain and offset that fit the best straight line response.

2.5.2 Sine Curve Fitting

Some ADC test methods generate a digital sine wave at the output using a precise analog sine wave generator. In most cases, the ADC's possible restrictions in results that are not exactly sine waves, necessitating the extraction of the best possible sine wave approximation (often with offset) from a large measured set. The three-parameter least-squares fit is used for processing (if the frequency is known) or the four-parameter least-squares fit (if the frequency needs to be found). When the data set does not precisely represent an integer number of cycles, the three-parameter fit is utilized since the DFT may be more straightforward in this situation.

The fit method determines the values of A_0, B_0, Y_{os} (and ω_0) that minimize the sum of squared differences

$$\sum_{i=1}^{M} [y_i - A_0 \cos(\omega_0 iT) - B_0 \sin(\omega_0 iT) - Y_{os}]^2 \tag{2-21}$$

Where $y_1, y_2, \cdots, y_M$, is a sequence of M input samples taken at successive sample times.

If the frequency is known we can define the matrixes

$$D_0 = \begin{bmatrix} \cos(\omega_0 iT) & \sin(\omega_0 iT) & 1 \\ \cos(2\omega_0 iT) & \sin(2\omega_0 iT) & 1 \\ \dots & \dots & \dots \\ \cos(M\omega_0 iT) & \sin(M\omega_0 iT) & 1 \end{bmatrix}$$

$$y = \begin{bmatrix} y_1 \\ y_2 \\ \dots \\ y_M \end{bmatrix} x_0 = \begin{bmatrix} A_0 \\ B_0 \\ Y_{os} \end{bmatrix}$$

that give rise to the matrix notation of Eq. 2-21

$$(y - D_0 x_0)^T (y - D_0 x_0) \tag{2-22}$$

where T designates the transpose.

The testing procedure is divided into the following steps because the minimum of the aforementioned equations decides the outcome: apply a sine wave with specified parameters to the input of the ADC, take a record of the output data, fit a sine wave to the sequence of samples by estimating phase, amplitude, dc value, and (if needed) frequency by minimizing the sum of the squared difference expressed by Eq. 2-22.

2.5.3 Histogram Method

Using an ADC input with known magnitude distribution (or probability density function $pin(x)$ is known), a series of output samples are created. The histogram method is a statistical analysis of these data. The occurrence probability P_i of a certain output code V_i is, for an ideal ADC, the integral of the probability of having the input in the range of V_i. Therefore, an ideal

ADC with N equal quantization intervals and dynamic range V_{FS} gives rise to

$$P_i = \int_{(i-1)\Delta}^{i\Delta} pin\,(x)dx; i = 1 \ldots\ldots N; \Delta = V_{FS}/(N-1) \tag{2-23}$$

Δ is the ideal step size or the average step size. If the converter is not ideal the integral that defines the occurrence probability of the output code V_i must extend between the actual code transitions limits

$$P_{i,r} = \int_{V_{L,i}}^{V_{U,i}} pin\,(x)dx \tag{2-24}$$

where lower code ($j\,\Delta$ sums) and upper code (add i-th Δ) transitions are

$$V_{L,i} = \sum_{j=1}^{i-1} \Delta_j; V_{U,i} = V_{L,i} + \Delta_i \tag{2-25}$$

Assuming the number of samples M is large, the ideal and real occurrence probability P_i and $P_{i,r}$ are approximately the ideal and real number of samples M_i and $M_{i,r}$ divided by M that give rise to the ideal code V_i.

$$P_i = \frac{M_i}{M}; P_{i,r} = \frac{M_{i,r}}{M} \tag{2-26}$$

The number of quantization intervals and/or the probability density function are typically such that $pin(x)$ can be assumed constant within the i-th quantization interval and equal to $pin(V_{L.i})$. Therefore, using Eq. 2-24 we obtain

$$P_i = pin(V_{L.i})\Delta; P_{i,r} = pin(V_{L.i})\Delta_i \tag{2-27}$$

which combined with Eq. 2-26 yields

$$\Delta_i = \frac{M_i}{M \cdot pin(V_{L.i})} \tag{2-28}$$

Moreover, if the inputs have constant probability over the entire dynamic range (like a linear ramp or a saw tooth extended over the entire analog range) then $pin(x) = \frac{1}{V_{FS}}$, where the integral of $pin(x)$ over the $0 \sim V_{FS}$ range is 1. Therefore,

$$\frac{\Delta_i}{V_{FS}} = \frac{M_i}{M} = \frac{1}{N}; \frac{\Delta_i}{V_{FS}} = \frac{M_{i,r}}{M} \tag{2-29}$$

which determines the DNL of the i-th channel

$$DNL(i) = \frac{\Delta_i - \Delta}{\Delta} = \frac{M_{i,r} - M_i}{M_i} \tag{2-30}$$

also expressed by

$$DNL(i) = \frac{N \cdot M_{i,r}}{M} - 1 \tag{2-31}$$

The histogram method determines both DNL and INL with an accuracy that is inversely proportional to the number of samples kept in each channel since the accumulation of the DNL yields the INL.

To find the minimum number of samples needed for estimating the differential nonlinearity, a $100(1-\alpha)$ percent confidence interval of the form $(\mu - Z_{\alpha/2}\sigma,\ \mu + Z_{\alpha/2}\sigma)$ is set up. α is s chosen for the desired confidence level. $Z_{\alpha/2}\sigma$ is the precision to which the measured value differs from the true value μ. The derivation of σ and the subsequent minimum number of samples needed is carried out in [5].

In the n-bit case, the minimum number of samples N_t, needed for β bit precision and $100(1-\alpha)$ percent confidence is given by Eq. 2-32 where $Z_{\alpha/2}$ can be found in a table of the standard normal distribution function:

$$N_t = \frac{Z^2{}_{\alpha/2}\pi 2^{n-1}}{\beta^2} \tag{2-32}$$

To know the differential nonlinearity for an 8-bit converter to within 0.10 LSB with 99 percent confidence, about 268000 samples are needed.

2.6 Gain and Offset Calibration

The most commonly used in the calculation is endpoint fit. The starting point and the ending point of ADC are selected as fitting parameters, and the fitting curve is:

$$y = m_m \cdot x + b \tag{2-33}$$

The slope can be determined by the coordinates of any two points as shown in Fig. 2.16.

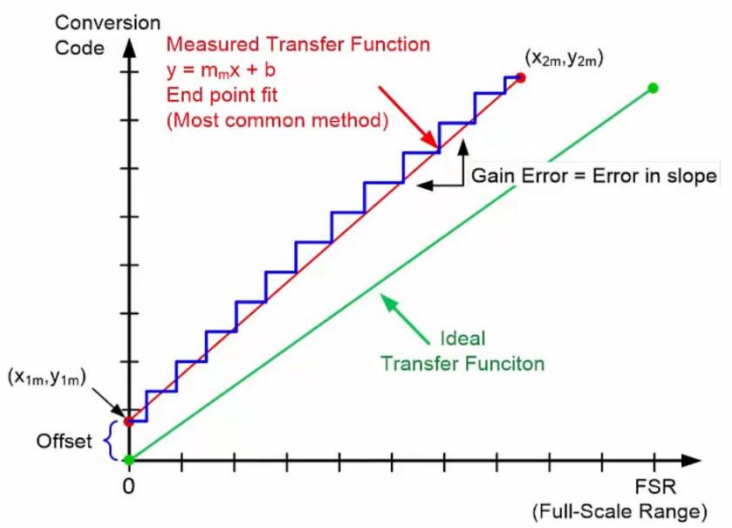


Fig. 2.16 Offset & Gain Error

$$m_m = \frac{y_{2m} - y_{1m}}{x_{2m} - x_{1m}} \tag{2-34}$$

The offset error is the intercept of vertical axis when $x = 0$.

Gain error is the percentage of difference between the ideal slope and the real slope. m_i is the slope of ideal transfer function.

$$E_G = \left(\frac{m_m - m_i}{m_i}\right) \cdot 100\% \tag{2-35}$$

2.7 Summary

This chapter first introduces sampling, quantization noise and common types of ADC・DAC, and briefly describes their operating principles, then introduces the static and dynamic characteristics of ADCs, and briefly explains the definitions of these characteristics. And the last thing to introduce is data processing.

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[2] P. Cruz, N. B. Carvalho and K. A. Remley, "Evaluation of Nonlinear Distortion in ADCs Using Multi-Sines", IEEE MTT-S International Microwave Symposium, Atlanta, GA (Jun. 2008).

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Chapter 3 Code Selective Histogram Method

3.1 ADC Output Code Prone to Nonlinearities

The linearity of the entire ADC is determined by the linearity of the DAC inside the ADC in many cases. Taking SAR ADC as an example, it uses binary search and comparison of the sampled analog voltage to the DAC output voltage to convert analog input to digital output. Fig. 3.1 provides a basic overview of SAR ADC. There the largest nonlinearity is likely to occur close to $\frac{1}{2}$ of digital code range (all switches change). The second large nonlinearities may occur around $\frac{1}{4}, \frac{3}{4}$. The actual ADC structure will determine the code that is prone to nonlinearities.

In Fig. 3.2 case, the largest nonlinearity in the 5-bit R-2R trapezoidal binary weighted DAC is likely to occur close to the digital codes 15 to 16. (all switches will change). Next, large nonlinearities may occur around 8, 24, and then around 4, 12, 20, and 28. The DAC codes prone to nonlinearity depend on the DAC architecture as shown in [1,2].

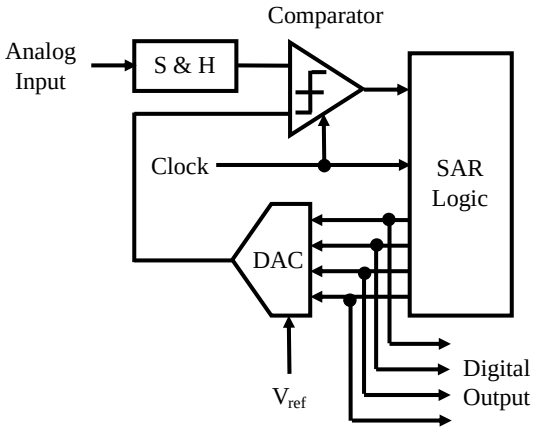

Fig. 3.1 Block diagram of typical SAR ADC

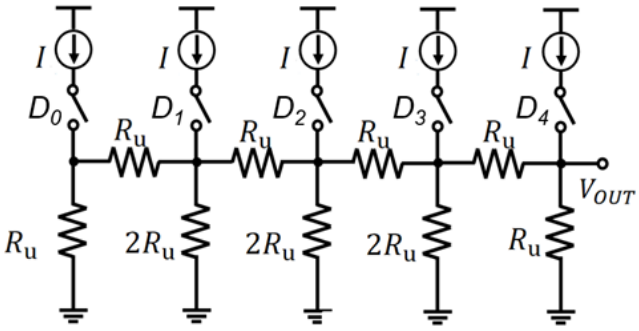

Fig. 3.2 R-2R ladder network DAC

3.2 Conventional Sine Histogram Method and Problem

Since accurate knowledge of the probability density function is key for the histogram method, a convenient test signal is a sine wave. Let us think about the sine wave histogram method. The input sine wave is sampled, as shown in Fig. 3.3, and the value of the histogram for the corresponding digital output code bin is increased by one. After that, the histogram or frequency of occurrence of each code can be displayed as shown in Fig. 3.4.

An accurate estimation of the probability density function that, including a possible offset ($V = A\sin(x) - V_{os}$) is

$$p(V) = \frac{1}{\pi\sqrt{A^2 - x^2}} : x = V - V_{os} \tag{3-1}$$

The integration of the density function from $P(V_i,\ V_{i+1})$ that voltage exists between V_i and V_{i+1} is given by

$$P(V_i, V_{i+1}) = \frac{1}{A\pi}\{\arcsin\left[\frac{V_{i+1} - V_{os}}{A}\right] - \arcsin\left[\frac{V_i - V_{os}}{A}\right]\} \tag{3-2}$$

The input signal's amplitude (vertical axis) in Fig. 3.3 is represented by the horizontal axis of Fig. 3.4. For example, in the case of a 12-bit ADC, the amplitude of the input signal is divided by 4096. Notice that while a highly linear saw signal is hard to produce, low distortion sine waves are relatively simple to achieve using analog filters [3-7].

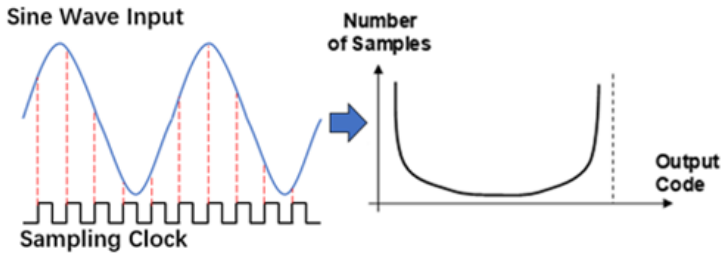

Fig. 3.3 Histogram generation for sine wave input

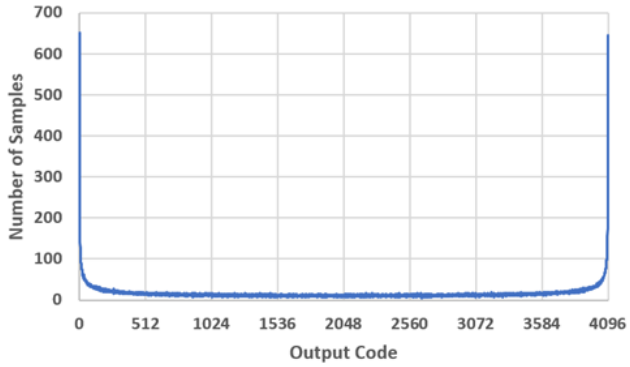

Fig. 3.4 Ideal 12-bit ADC output histogram for the sine wave input

The histogram is concentrated on both ends of the code, as shown in Fig. 3.4, which is a problem because the test time is longer near the center of the code.

In many cases, ADC linearity must often be assured around the center code. Histogram ADC testing with the sine wave input takes long time to measure the linearity accurately around the center of the ADC output range, because DNL measurement accuracy is proportional to the number of data samples in the bin. However, as shown in our previous study [8], focusing on specific codes can avoid this shortcoming.

3.3 DNL/INL Calculation Algorithm for Multi Tone Wave

Fig. 3.5 shows a waveform input to the ADC which is a periodic function $V = f(t)$ with two points (as shown in Fig. 3.5, the first point and the middle point) where $f'(t) = 0$ (slope is 0) in one cycle (T). Solving Eq. 3-3 over time t yields Eq. 3-4.

$$V = f(t) \tag{3-3}$$

$$t = f^{-1}(V) \tag{3-4}$$

The probability density $p[i]$ that voltage exists between i-th voltage V_i and $(i+1)$-th voltage V_{i+1} is given by

$$p[i] = \frac{2(t_{i+1} - t_i)}{T} = \frac{2\left(f^{-1}(V_{i+1}) - f^{-1}(V_i)\right)}{T} \tag{3-5}$$

Cumulative probability density is given as follows:

$$PI[i] = \sum_{k=0}^{i} p[k] = \frac{2f^{-1}(V_{i+1})}{T} \tag{3-6}$$

Then we obtain the following:

$$V_{i+1} = f\left(\frac{T}{2} PI[\mathrm{i}]\right) \tag{3-7}$$

Δ is the ideal step size or the average step size. About real output V_r, we use $\frac{V_{r,2^n-1} - V_{r,1}}{2^n - 2}$ to approximate Δ. DNL can be calculated as follows:

$$DNL[i] = \frac{V_{r,i+1} - V_{r,i}}{\Delta} - 1 = \frac{V_{r,i+1} - V_{r,i}}{\frac{V_{r,2^n-1} - V_{r,1}}{2^n - 2}} - 1$$

$$= (2^n - 2) \cdot \frac{f\left(\frac{T}{2} PI_r[i]\right) - f\left(\frac{T}{2} PI_r[i-1]\right)}{f(\frac{T}{2} PI_r[2^n - 2]) - f\left(\frac{T}{2} PI_r[0]\right)} - 1 \qquad (3\text{-}8)$$

$$i = 1,2, \dots, 2^n - 1$$

INL is also obtained as follows:

$$INL[i] = \sum_{k=1}^{i} DNL[k]$$

$$= (2^n - 2) \cdot \frac{f\left(\frac{T}{2} PI_r[i]\right) - f\left(\frac{T}{2} PI_r[0]\right)}{f(\frac{T}{2} PI_r[2^n - 2]) - f\left(\frac{T}{2} PI_r[0]\right)} - i \qquad (3\text{-}9)$$

$$i = 1,2, \dots, 2^n - 1$$

Here we set $DNL[0]$ and $INL[0]$ to 0. It is difficult to use inverse function of multi-tone wave for calculating probability density function $PI(V)$. But with this algorithm, we can obtain actual ADC DNLs and INLs using the histogram method with multi-tone signal, by using probability distribution $PI_r[i]$ obtained by measurement of the ADC under test substituting into $PI[i]$ in Eq. 3-8 and Eq. 3-9.

Comparing the algorithm with the approach using the ideal histogram, simulation using sine wave input has validated the algorithm's validity. In simulation, 10-bit SAR ADC is assumed and thus the ADC output ranges from 0 to 1023. The total number of samples is 2^{16} (65 536). To know the differential nonlinearity for a 10-bit converter to within 1LSB with 99.998 percent confidence, about 27 000 samples are needed from Eq. 2-32. And in a 10-bit converter to within 0.10LSB with 99 percent confidence case, about 1 070 700 samples are needed

Except for the results near the codes 0 and 1023, Fig. 3.6 shows that most always, the absolute difference between DNLs determined using the method in this section and the ideal histogram is 0.0002 LSB or less.

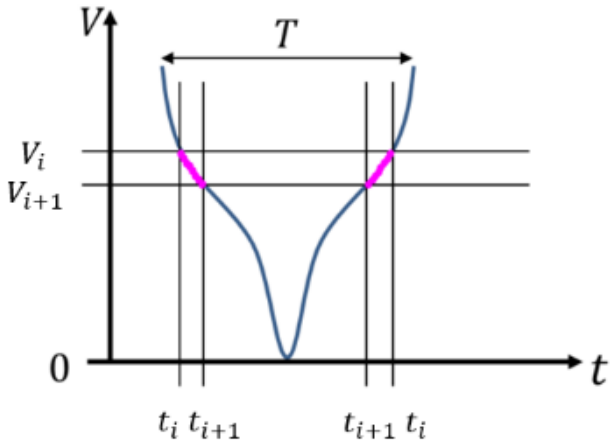

Fig. 3.5 Example of a periodic function $V = f(t)$.

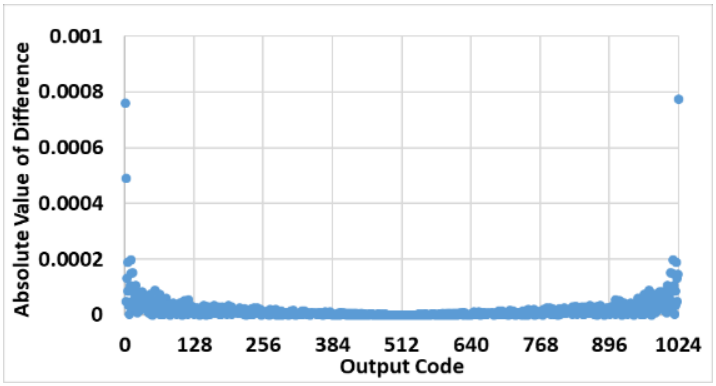

Fig. 3.6 Absolute value of the difference between DNLs calculated from the method in Section 3.3 and the ideal histogram.

3.4 Two-Tone Sine Wave Input

The amount of data in each histogram bin determines the accuracy of the nonlinearity evaluation for each code. Therefore, to improve the accuracy of the nonlinearity evaluation, the amount of data in the corresponding histogram bin should be increased.

The number of samples at the corresponding amplitude positions (codes) the obtained ADC output data increases with the gentler the slope of the input signal waveform. Therefore, we consider using a two-tone sine wave to make the slope softer at the corresponding amplitude locations [9]. And there are two reasons, the first is that the complexity of calculation and focus on code prone to nonlinearity are relatively simpler. And the second is that applicable input waveforms about proposed method that is a periodic function $V = f(t)$ with two points where $f'(\mathrm{t}) = 0$ (slope is 0) in one cycle (T). Multi-tone will more difficult to control.

The two-tone sine wave is generated by the arbitrary waveform generator (AWG) as shown in Fig. 3.7 [10, 11]. The arbitrary digital two-tone sine wave is generated from DSP. After the digital signal is converted to analog signal by DAC, it is applied to DUT through analog filter.

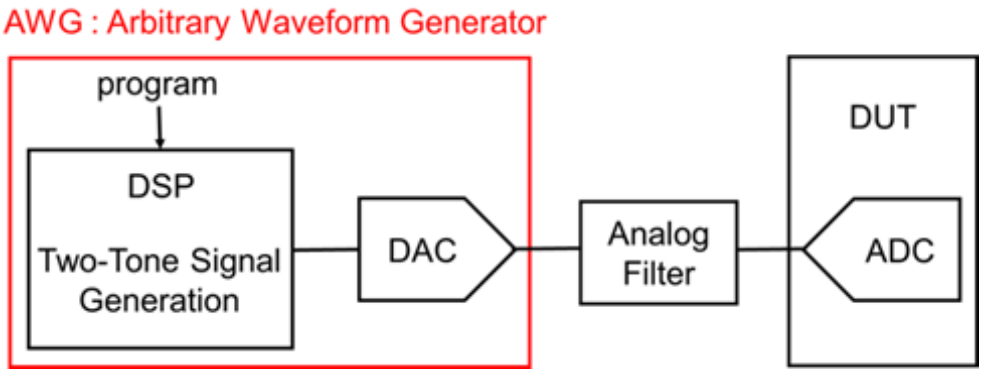

Fig. 3.7 Hardware components for generating proposed two-tone sine wave

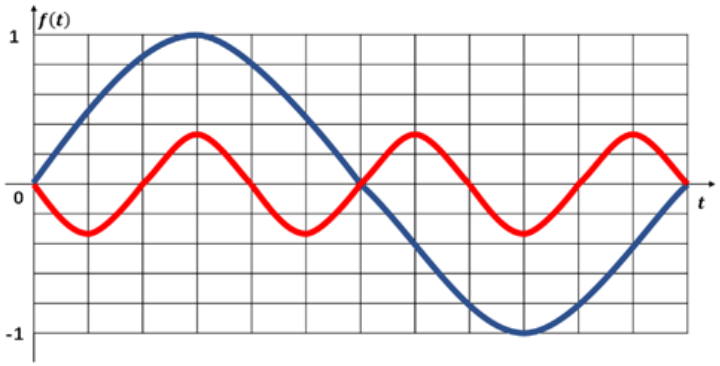

Fig. 3.8 Waveforms $f(t) = \sin(t)$ in blue and $f(t) = -\frac{\sin(3t)}{3}$ in red

First, we consider increasing the number of samples around the center 512. Fig. 3.8 plots the first term and second term of Eq. 3-11, respectively. Because the slope between half-cycles of sine wave are opposite, it needs to be staggered to match the slope by using odd number. The value of ω_2 is odd number 3. The slope of $f_3(t)$ at the center is reduced to zero ($t =$

$\arcsin 0 = \pi$) as shown in Fig. 3.9.

$$f_{\omega_2}(t) = \sin(\omega_1 t) - \frac{\sin(\omega_2 t)}{k} \tag{3-10}$$

$$f_3(t) = \sin(t) - \frac{\sin(3t)}{3} \tag{3-11}$$

Fig. 3.10 shows the histogram when the test stimulus of Eq. 3-11 is applied to the ideal 10-bit ADC. In all simulation in chapter 3, 10-bit SAR ADC is assumed and thus the ADC output ranges from 0 to 1023. The total number of samples is 2^{16} (65 536).

As a result, we see that the number of samples near the center (near the digital output 512) is increased, as shown in Fig. 3.10.

Fig. 3.11 and Fig. 3.12 show the obtained ideal 10-bit ADC DNL and INL measurements of the two-tone sine wave $f_3(t)$ and $\sin(t)$, respectively. Around the code 512, where the length of the bin of the histogram is greater, the distributions of the ideal 10-bit ADC DNL and INL of the two-tone sine wave become narrower.

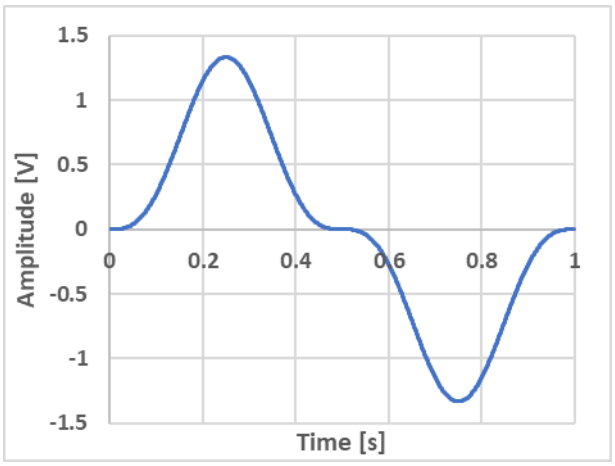

Fig. 3.9 Input wave $f_3(t) = \sin(t) - \frac{\sin(3t)}{3}$

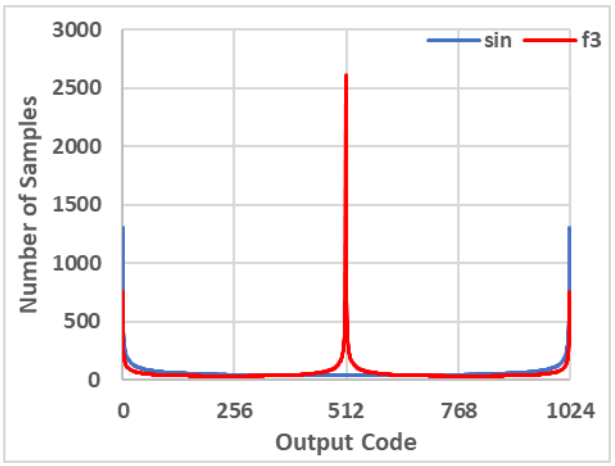

Fig. 3.10 Ideal 10-bit ADC output histogram for the input signal of $f_3(t) = \sin(t) - \frac{\sin(3t)}{3}$ in red and $f(t) = \sin(t)$ in blue

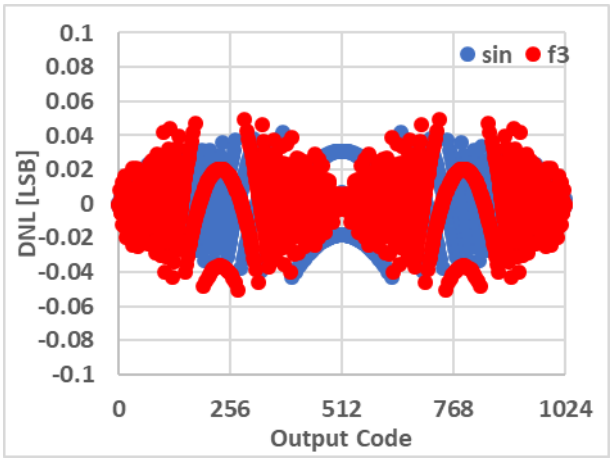

Fig. 3.11 Ideal 10-bit ADC DNL for the input signal of $f_3(t) = \sin(t) - \frac{\sin(3t)}{3}$ in red and $f(t) = \sin(t)$ in blue

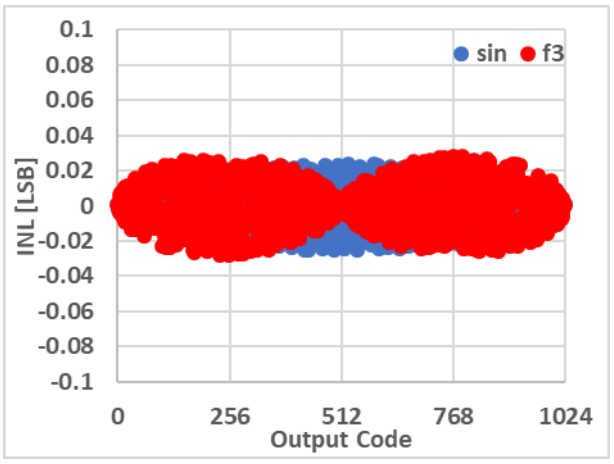

Fig. 3.12 Ideal 10-bit ADC INL for the input signal of $f_3(t) = \sin(t) - \frac{\sin(3t)}{3}$ in red and $f(t) = \sin(t)$ in blue

Next, we consider increasing the number of samples around 256 and 768. We change the amplitude positions to produce more occurrences of the gentle waveform slope, in other words, for example, $t = \arcsin\frac{1}{2} = \frac{\pi}{6}, \ldots$ Notice that $\frac{\pi}{6}$ is 1/12 of the period 2π, because the slope between half-

cycles of sine wave are opposite, it needs to be staggered to match the slope by using odd number. The value of ω_2 is adjacent odd number 11 is shown in Fig. 3.13. And each term of the two-tone sine wave of Eq. 3-12 is shown in Fig. 3.14.

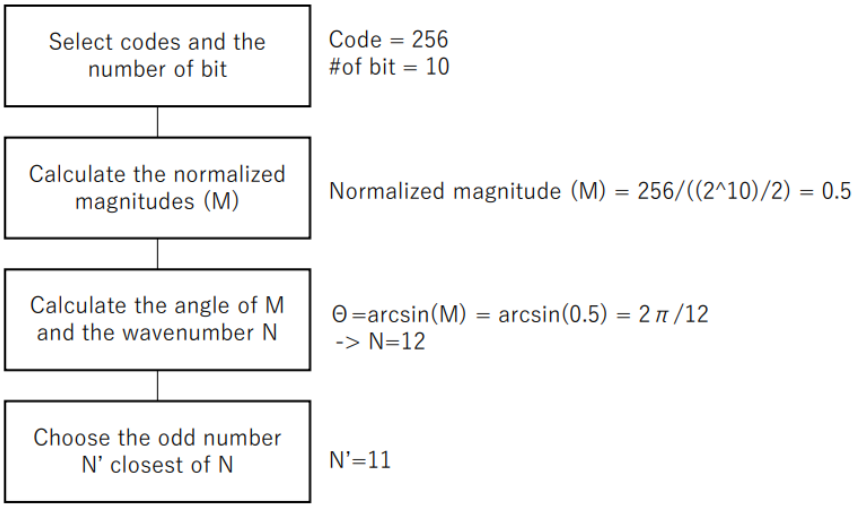

Fig. 3.13 Flowchart of ω_2 in $f_{11}(t)$

The value of k is 25 to make the waveform with two points where (slope is 0) in one cycle. The waveform of the two-tone sine wave is shown in Fig. 3.15.

$$f_{11}(t) = \sin(t) - \frac{\sin(11t)}{25} \tag{3-12}$$

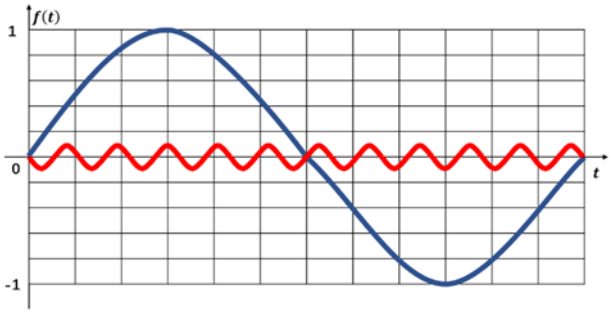

Fig. 3.14 $f(t) = \sin(t)$ in blue and $f(t) = -\frac{\sin(11t)}{25}$ in red

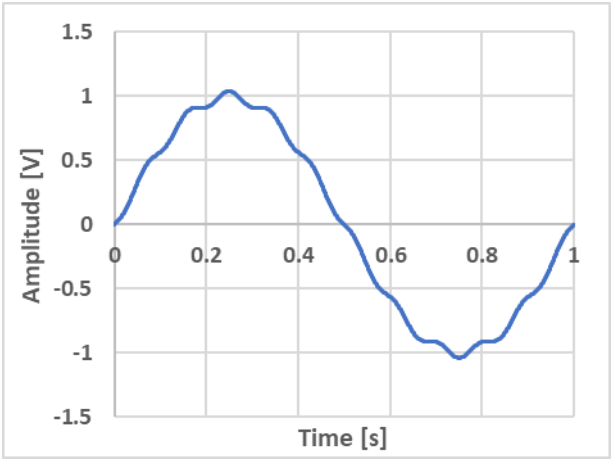

Fig. 3.15 Input wave $f_{11}(t) = \sin(t) - \frac{\sin(11t)}{25}$

Fig. 3.16 shows the histogram when the test stimulus of Eq. 3-12 is applied to the ideal 10-bit ADC. The total number of samples is 2^{16} (=65 536).

The number of samples near the targets (256, 768 as well as 512) has increased. The two extra sharp peaks surrounding the codes are visible in the histogram. Because the slope of the basic sine wave in some of these places is equal to or occasionally gentler than that of the second tone of the input two-tone sine wave, these extra peaks appear around the fundamental sine

wave's maximum and minimum values. It sometimes has a negative impact on DNL and INL calculations [12].

Fig. 3.17 and Fig. 3.18 show the obtained ideal 10-bit ADC DNL and INL measurements of the two-tone sine wave $f_{11}(t)$ and $\sin(t)$, respectively. The length of the bin in the histogram is larger, such as around the codes 256, 768, and 512, the distributions of both DNL and INL of the two-tone sine wave become narrower.

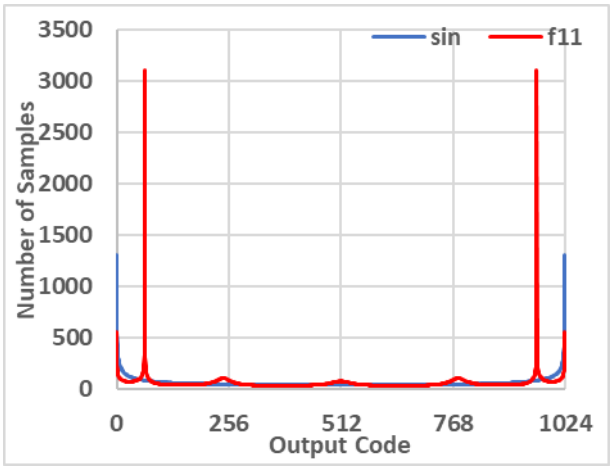

Fig. 3.16 Ideal 10-bit ADC output histogram for the input signal of $f_{11}(t) = \sin(t) - \frac{\sin(11t)}{25}$ in red and $f(t) = \sin(t)$ in blue

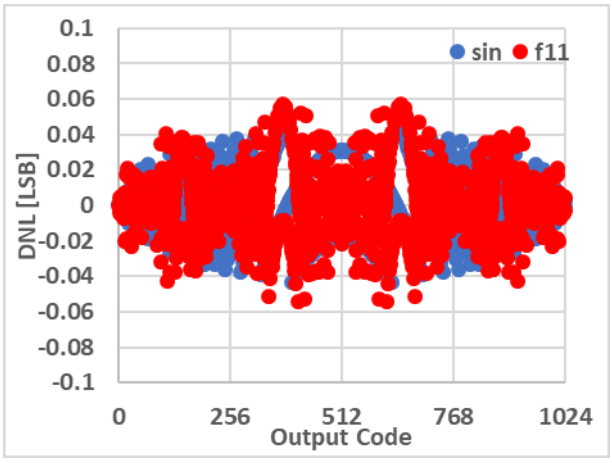

Fig. 3.17 Ideal 10-bit ADC DNL for the input signal of $f_{11}(t) = \sin(t) - \frac{\sin(11t)}{25}$ in red and $f(t) = \sin(t)$ in blue

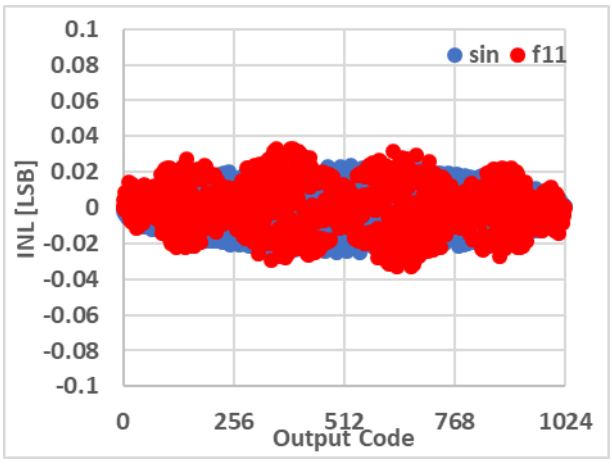

Fig. 3.18 Ideal 10-bit ADC INL for the input signal of $f_{11}(t) = \sin(t) - \frac{\sin(11t)}{25}$ in red and $f(t) = \sin(t)$ in blue

In the same way, we can use $\arcsin\frac{1}{4} \approx \frac{\pi}{12}$ ($\frac{1}{24}$ of period 2π) to consider increasing 384, 640 and $\arcsin\frac{1}{8} \approx \frac{\pi}{25}$ ($\frac{1}{50}$ of period 2π) to consider increasing 448, 576. The following Eq. 3-13 and Eq. 3-14 are corresponding two-tone sine waves. The values of *k* are 50, 100, respectively.

$$f_{23}(t) = \sin(t) - \frac{\sin(23t)}{50} \tag{3-13}$$

$$f_{51}(t) = \sin(t) - \frac{\sin(51t)}{100} \tag{3-14}$$

However, extra peaks of the histogram of $f_{23}(t)$and $f_{51}(t)$ make it difficult to calculate DNL and INL. The two-tone sine wave is amplified, and the amplitude positions are changed to avoid the extra peaks. (ω_2 is tuned). As a result, the following two equations Eq. 3-15 and Eq. 3-16 are used instead of Eq. 3-13 and Eq. 3-14, respectively.

$$f_{31}(t) = 1.2\left(\sin(t) - \frac{\sin(31t)}{50}\right) \tag{3-15}$$

$$f_{59}(t) = 1.2\left(\sin(t) - \frac{\sin(59t)}{100}\right) \tag{3-16}$$

Fig. 3.19 and Fig. 3.20 show each histogram. The total number of samples is 2^{16} (=65 536). The number of samples near target codes 128, 256, 384, 512, 640, 768, 896 of histogram of Fig. 3.19 should be increased. They are codes corresponding to the DAC output voltages. However, the peaks are not found on the codes 128, 256, 768, 896 in Fig. 3.19.

The number of samples near target codes 64, 128, 192, 256, 320, 384, 448, 512, 576, 640, 704, 768, 832, 896 of histogram of Fig. 3.20 should be increased. However, the peaks are not found on the codes 64, 128, 192, 832, 896 and 960 in Fig. 3.21. The heights of the peaks of the histograms of f_{31}

and f_{59} are around 100. The widths of the peaks get narrower as ω_2 increases.

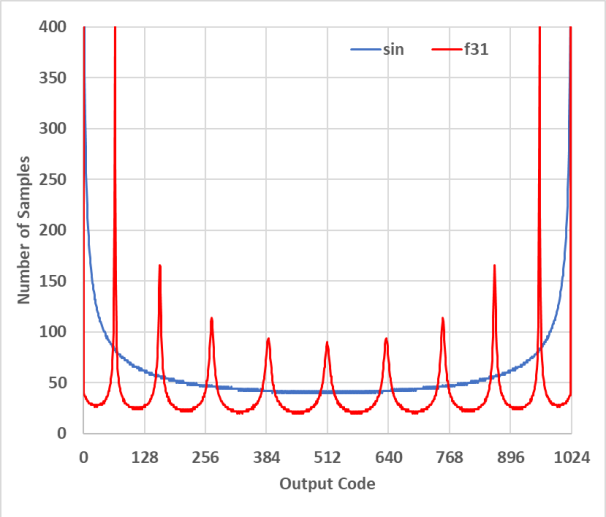

Fig. 3.19 Ideal 10-bit ADC output histogram for the input signal of $f_{31}(t) = 1.2\left(\sin(t) - \frac{\sin(31t)}{50}\right)$ in red and $f(t) = \sin(t)$ in blue

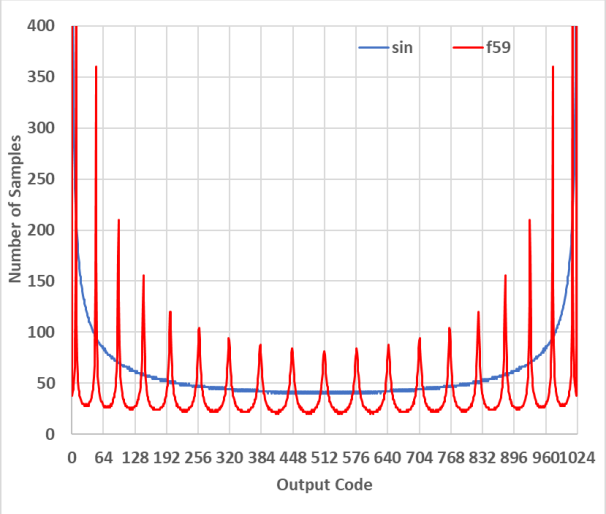

Fig. 3.20 Ideal 10-bit ADC output histogram for the input signal of $f_{59}(t) = 1.2\left(\sin(t) - \frac{\sin(59t)}{100}\right)$ in red and $f(t) = \sin(t)$ in blue

Fig. 3.21, Fig. 3.22, Fig. 3.23 and Fig. 3.24 show the obtained ideal 10-bit ADC DNL and INL measurements of the two-tone sine waves $f_{31}(t)$ and $f_{59}(t)$, comparing with those of $\sin(t)$, respectively. Compared to the distributions of DNL and INL $f_3(t)$ of $f_{11}(t)$, those of $f_{31}(t)$ and $f_{59}(t)$ spread relatively widely in the vertical direction.

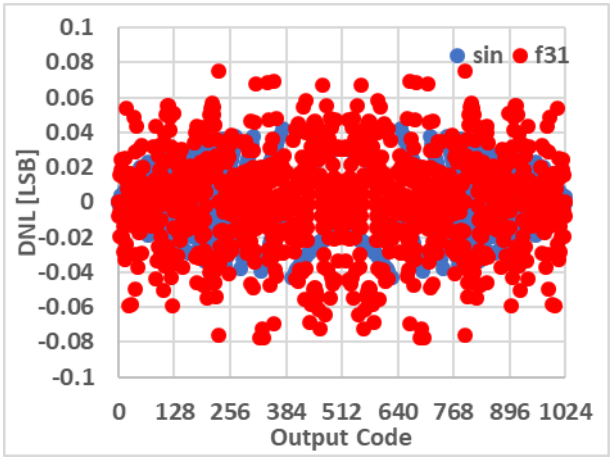

Fig. 3.21 Ideal 10-bit ADC DNL for the input signal of $f_{31}(t) = 1.2\left(\sin(t) - \frac{\sin(31t)}{50}\right)$ in red and $f(t) = \sin(t)$ in blue

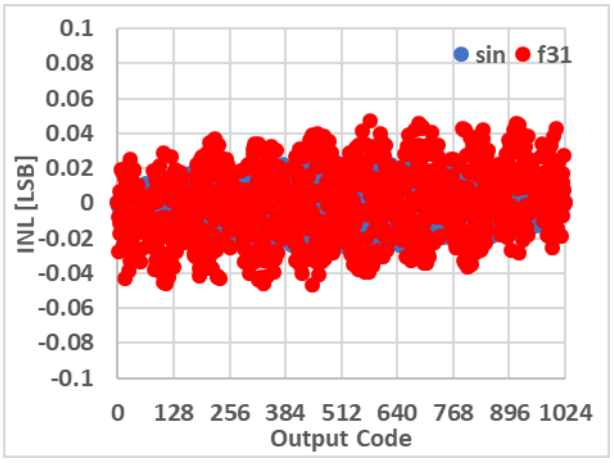

Fig. 3.22 Ideal 10-bit ADC INL for the input signal of $f_{31}(t) = 1.2\left(\sin(t) - \frac{\sin(31t)}{50}\right)$ in red and $f(t) = \sin(t)$ in blue

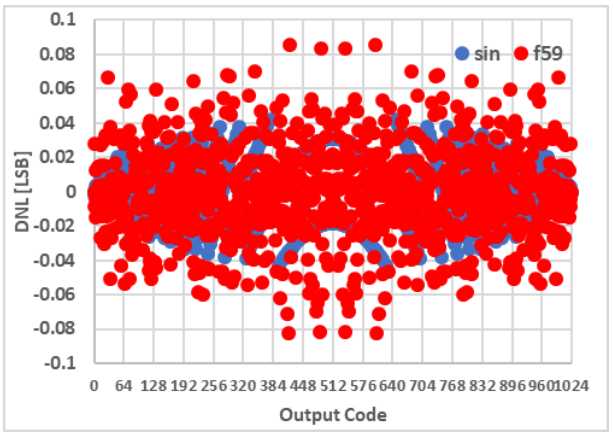

Fig. 3.23 Ideal 10-bit ADC DNL for the input signal of $f_{59}(t) = 1.2\left(\sin(t) - \frac{\sin(59t)}{100}\right)$ in red and $f(t) = \sin(t)$ in blue

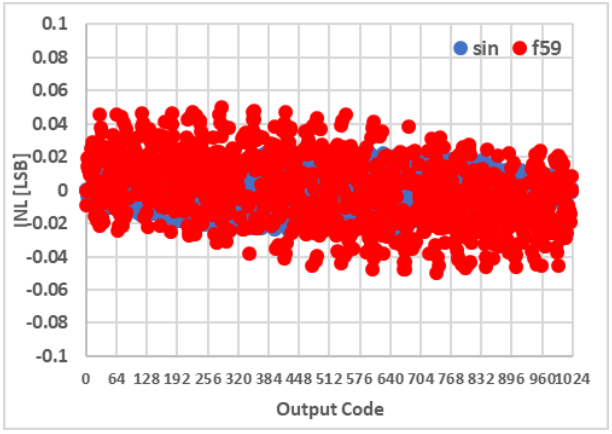

Fig. 3.24 Ideal 10-bit ADC INL for the input signal of $f_{59}(t) = 1.2\left(\sin(t) - \frac{\sin(59t)}{100}\right)$ in red and $f(t) = \sin(t)$ in blue

The INL and DNL around the codes with high peak seems to be larger as the number of peaks increases. Because we set DNL[0] and INL[0] to 0 and use it as a benchmark, so INL has a slope.

3.5 Evaluation Result of Undistorted ADC and Distorted ADC

Simulation results show the effectiveness of the code-selective histogram algorithm. ω_1 is 1.0, while ω_2 is 11.0. The code-selective histogram method is applied to a non-linear 10-bit ADC to calculate its DNL. In this evaluation, the two-tone sine wave Eq. 3-12 ($f_{11}(t) = \sin(t) - \frac{\sin(11t)}{25}$.) input is used to obtain more data at the bins of codes 511, 255, 767. The total number of samples is 2^{16} (=65 536).

The code-selective histogram method is applied to an ideal linear 10-bit ADC. Fig. 3.25 shows the result for two-tone $f_{11}(t)$ and sine wave $\sin(t)$ cases. Numbers of samples at codes of 511, 255, 767 have increased.

Measurement errors for two-tone at codes of 511, 255, 767 are smaller than those of the conventional sine wave method.

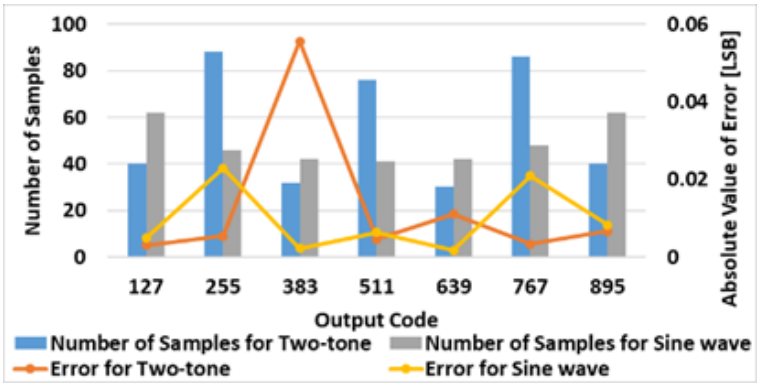

Fig. 3.25 Comparison of ideal ADC using sine wave and two-tone input ($f_{11}(t)$) histograms.

The code-selective histogram algorithm is applied to a distorted ADC to calculate its DNL. Here, relatively larger DNLs are added to the vulnerable codes of 511, 255, 767, 127, 383, 639, 895 for comparison and calculate their DNLs with the code-selective histogram method and the conventional sine wave method. In this evaluation, 0.5, -0.3, -0.3 LSB are added to codes of 511, 255, 767 as DNL, and 0.1 LSB are added to codes 127, 383, 639, 895 as DNL as shown in Table 3.1, respectively.

Table 3.1 DNL added of distorted ADC

Code	DNL(LSB)
127	0.1
255	-0.3
383	0.1
511	0.5
639	0.1
767	-0.3
895	0.1

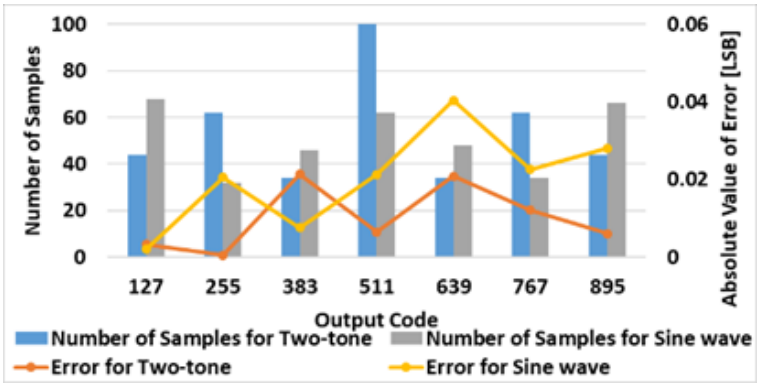

Fig. 3.26 Comparison of obtained DNL errors of non-ideal ADC using sine wave and two-tone input ($f_{11}(t)$) histograms.

Fig. 3.26 shows the result for two-tone $f_{11}(t)$ and sine wave $\sin(t)$ cases. Numbers of samples at codes of 255, 767, 511 have increased, whereas those at codes of 127, 383, 639, 895 have decreased. We see that errors for two-tone at codes of 255, 767, 511 are smaller than those of the conventional sine wave method. As shown in Table 3.2, Error compared to added DNL, the result of two-tone waveform is more accurate than sin waveform on specific codes. DNL accuracy of specific code is improved by about 2%~7%. At codes of 255, 767, 511, Numbers of samples for two-tone have almost twice as many samples as sine wave, and the total number of samples is 2^{16}

(=65 536). Therefore, by reducing the total number of samples, it is possible to shorten the time while maintaining the same accuracy.

Table 3.2 DNL Accuracy of Distorted ADC

Output code	255	511	767
Added DNL	-0.3	0.5	-0.3
Number of Samples for Two-tone	62	114	62
Error for Two-tone (LSB)	0.000475	0.006441	0.012022
Number of Samples for Sine wave	32	62	34
Error for Sine wave (LSB)	0.020511	0.021264	0.022598
$\frac{E_{Sin} - E_{Two}}{\lvert DNL_{Add} \rvert}$	6.67%	2.96%	3.52%

3.6 Sensitivity of DNL, INL to Inaccuracy of Input Tones

Here, we assess the impact of amplitude and phase error on the DNL and INL of the proposed method.

Following equation is used for the evaluation to consider the case that $\omega_2 = 3\omega_1, k = 3$ in Eq. 3-10. The total number of samples is 2^{16} (=65 536).

$$f(t) = \sin(t) - \frac{A\sin(3t + \theta)}{3} \tag{3-17}$$

Where A - 1 is amplitude error, θ is phase error. When no error exists, $A = 1$, $\theta = 0$. Here we consider the case that $A \neq 1, \theta = 0$, where amplitude error exists. We calculate DNL and INL with the equation when

$A = 1,\ \theta = 0$. The determined DNL and INL are used to calculate the root mean square (RMS) of the DNL and INL. In case that A =0.95, 0.96, 0.97, 0.98, 0.99, 1.0, 1.01, 1.02, 1.03, 1.04, 1.05, the RMS is calculated.

Similarly, we consider the case that $A = 1, \theta \neq 0$, where phase error exists. We calculate DNL and INL with the equation when $A = 1,\ \theta = 0$. From the calculated DNL and INL, the RMS of the DNL and INL is obtained. The RMS is calculated in case that θ = -5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5(degree).

Fig. 3.27 shows amplitude error characteristics of the RMS of the DNL and INL. The horizontal axis is A, the vertical axis is the RMS of the DNL and INL. The curve of DNL is almost constant compared with the curve of INL. It is unsensitive to the amplitude error. On the other hand, the curve of INL is downward convex. It takes the maximum INL value near 5.2 with A = 1.05.

Fig. 3.28 shows phase error characteristics of the RMS of the DNL and INL. The horizontal axis is θ, the vertical axis is the RMS of the DNL and INL. The curve of DNL is almost constant compared with the curve of INL, although both of shapes of the curves are downward convex with origin symmetry.

The amplitude error of INL is more sensitive than the others in view of these results.

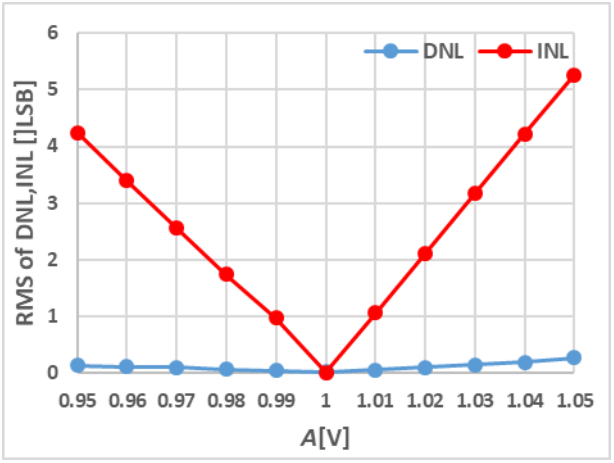

Fig. 3.27 Amplitude error characteristics of RMS of DNL, INL

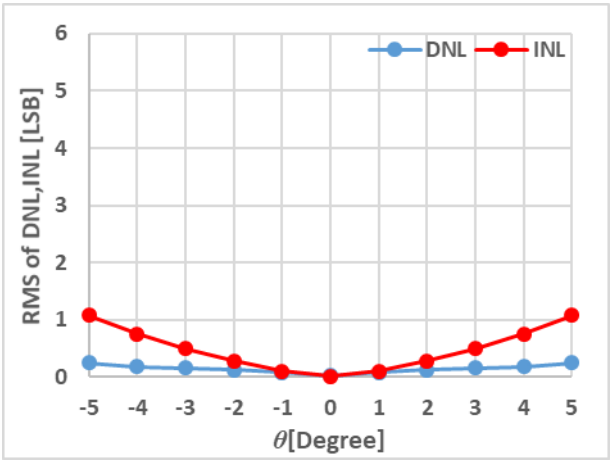

Fig. 3.28 Phase error characteristics of RMS of DNL, INL

Because the 3rd-order nonlinearity component of the DAC inside the AWG and that of the ADC under test would affect the $3\omega_1$ component at the ADC output, the condition $\omega_2 = 3\omega_1$ would not be appropriate in practical applications; sometimes, 3rd-order nonlinearity cannot be neglected.

However, the input waveforms yielded by equations Eq. 3-12, Eq. 3-15 and Eq. 3-16 are useful because the 11th, 31th, and 59th order nonlinearities are usually very small.

3.6 Summary

The two-tone sine wave input for the code selective histogram method for SAR ADC is the first introduced in this chapter. The proposed method increases frequency of appearance of the codes, then makes the length of the bins longer with two-tone sine wave input than method with sine wave. DNL accuracy of specific code is improved by about 2%~7%. And by reducing the total number of samples, it is possible to shorten the time while maintaining the same accuracy. Additionally, we created a program to test our algorithm in Section 3.3, and the outcomes of our simulations demonstrate the efficiency and performance of the code selected histogram method.

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Chapter 4 Decision of Optimal Sampling Frequencies Based on Classical Mathematics

4.1 Introduction

Chapter 3 mainly discusses the relationship between input signal waveform and histogram method, this section focuses on the relationship between input signal frequency and sampling frequency. In other words, this section outlines the decision-making process for the histogram method's the optimal sample frequency using classical mathematics [1].

The input signal frequency and sampling frequency for histogram method are defined as f_{sig}, f_{CLK}, respectively. With these parameters, the periods are also defined as $T_{sig} = 1/f_{sig}$, $T_{CLK} = 1/f_{CLK}$, respectively. Then the n-th sampling point of the sampling point's sequence p_n can be expressed as follows, by ignoring noise effect and initial phase difference between the frequencies.

$$p_n = nT_{CLK} mod\ T_{sig} \tag{4-1}$$

With a limited number of histogram data (in other words, with short test time), accurate test results can be obtained if the sequence distributes pseudo-randomly. If it cannot be pseudo-randomly distributed and concentrated in a certain place, the histogram will also be concentrated in the corresponding code, which is inconsistent with the actual. Accordingly, for accurate test,

the ratio between f_{CLK} and f_{sig} is important.

With the following two data sampling methods, we aim to find the optimal ratio between f_{CLK} and f_{sig}. These sample techniques are described in subsections 4.2 and 4.3, respectively. The characteristics of each sampling method with their comparison are provided in Subsection 4.4. Finally, the real number sampling method is then contrasted with some of the better samplings.

4.2 Metallic Ratio Sampling

In the first attempt, metallic ratio is introduced to the ratio between f_{CLK} and f_{sig}. Table 4.1 shows the definition of metallic ratio as $M_n = (n + \sqrt{n^2 + 4})/2$. The sampling frequency of the metallic ratio sampling is decided as $f_{CLK} = M_n \cdot f_{sig}$. With a small ratio of maximum to minimum distances between adjacent sampling points, metallic sampling can be performed. Also, the pseudo-randomness of the sampling points is improved approximately in proportional to the number of the data [2]. The authors investigated the relationship between f_{CLK} and f_{sig} and found that the "golden ratio" can effectively acquire the waveform in the time domain, and the proposed sampling condition ($f_{CLK} = \emptyset\, f_{sig}$, $\emptyset$: golden ratio) offers efficient waveform sampling, which we call golden ratio sampling [3, 4].

This paper uses the histogram method of ADC linearity test with the metallic ratio sampling and investigate the characteristics.

4.3 Prime Number Ratio Sampling

To apply the prime number ratio sampling is the second attempt. As ratios f_{CLK}/f_{sig}, two prime numbers are applied. (such as 23/13, 101/61, 199/127, 503/507).

4.4 Simulation Results

To investigate the optimal sampling method for code selective histogram method, Simulation is performed. RMS of DNL is the evaluation criterion. The resolution N is changed from 4-bit to 14-bit while the code selective histogram method is being used. In each resolution, RMS of DNL is calculated. The two-tone sine wave from Eq. 3-12 is used in this evaluation. The total number of samples M is 2^{20}(1 048 576). Then, the resolution characteristics of the root mean square (RMS) of the DNL are obtained with different resolution N. With each sample method, the characteristics are obtained. To know the differential nonlinearity for a 14-bit (16 384) converter to within 1-bit precision with 99.998 percent confidence, about 431 000 samples are needed from Eq. 2-32. And in a 14-bit converter to within 0.10LSB with 99 percent confidence case, about 17 130 862 samples are needed. At the same time needed samples in 9-bit, 10-bit, 11-bit, 12-bit, 13-bit are less than 14-bit case.

The metallic ration sampling is evaluated in Subsection 4.4.1, while the prime number ratio sampling is evaluated in Subsection 4.4.2.

4.4.1 Evaluation Results of Metallic Ratio

Table 4.1 Metallic ratios

N_n	The n-th metallic number	Decimal expansion	Nickname
0	1		
1	$\frac{1+\sqrt{5}}{2}$	1.6180339887⋯	Golden ratio ∅
2	$1+\sqrt{2}$	2.4142135623⋯	Silver ratio
3	$\frac{3+\sqrt{13}}{2}$	3.3027756377⋯	Bronze ratio
4	$2+\sqrt{5}$	4.2360679774⋯	
…		…	
N_n		$\frac{n+\sqrt{n^2+4}}{2}$	

In some cases of ADC testing, it is necessary to investigate several frequencies of f_{sig} for a fixed f_{CLK}, or several frequencies of f_{CLK} for a fixed f_{sig}. In such cases, golden ratio sampling is inadequate, therefore we used metallic ratios to investigate more relationships between f_{CLK} and f_{sig}, using metallic ratios (Table 4.1). Notice that the golden ratio is one of

the metallic ratios [5].

We obtain the resolution characteristics of the root mean square (RMS) of the DNL of the metallic ratio sampling with different resolution N. In this evaluation, $f_{CLK}/f_{sig} = M_n$. The resolution N characteristics are evaluated in the 8 cases while the value of n is changed from 1 to 8. Both the noise-free and noise-filled conditions are used to obtain the characteristics. In the case of the noisy condition, the sampling period and the fundamental sine wave of the two-tone test stimulus are both increased by the amount of Gaussian noise. In all the characteristics, RMS of DNL will increase as N increases. It is because M/N(the number of samples per bit divided equally) decreases as N increases.

The characteristics without noise, with 0.001% Gaussian noise, with 0.01% Gaussian noise, and with 0.1% Gaussian noise are shown in Figs. 4.1, 4.2, 4.3, and 4.4, respectively. The horizontal axis of each figure is division number N. The resolution of ADC is $log_2 N$(bits). The vertical axis is RMS of DNL.

The characteristics of M_2, namely Silver ratio, are shown in Fig. 4.1, are the worst. And all the characteristics, with the exception of M_2, are almost similar. The larger noise is, the worse characteristics are. As the added noise increases, the similarity of the characteristics becomes higher.

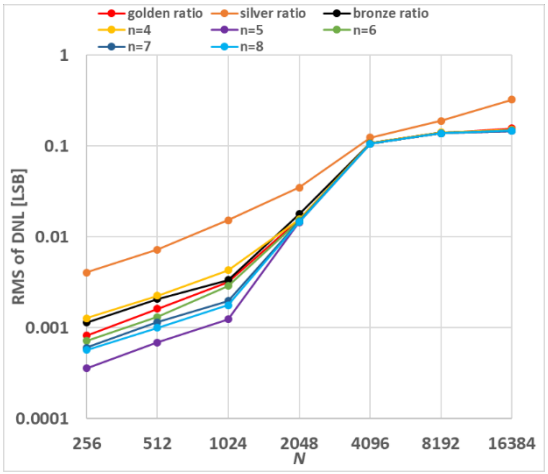

Fig. 4.1 Resolution characteristics of RMS of DNL of metallic ratio samplings (no noise)

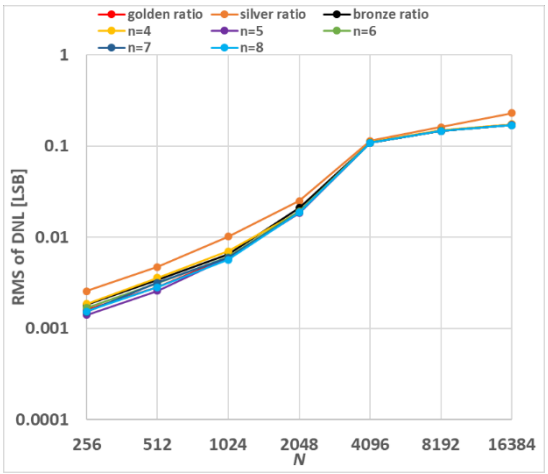

Fig. 4.2 Resolution characteristics of RMS of DNL of metallic ratio samplings (noise 0.001%)

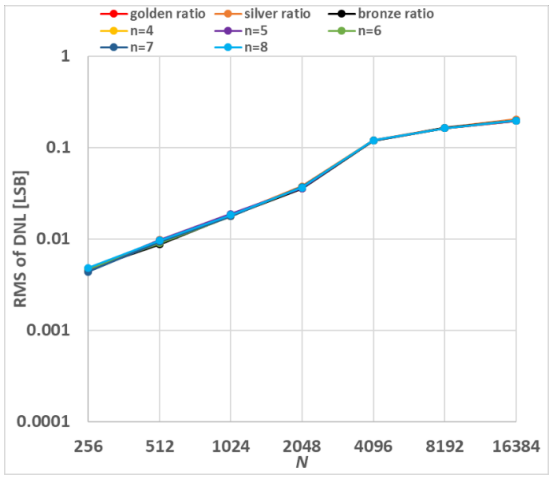

Fig. 4.3 Resolution characteristics of RMS of DNL of metallic ratio samplings (noise 0.01%)

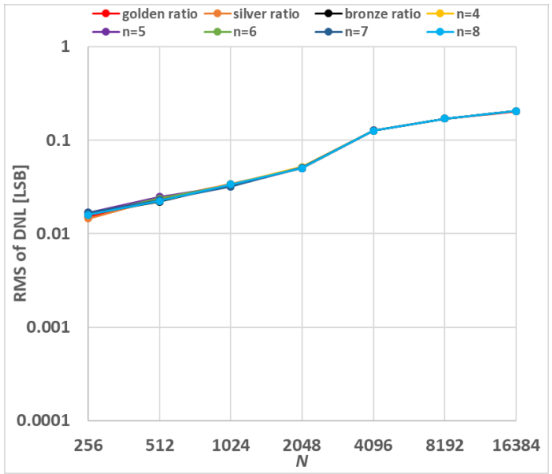

Fig. 4.4 Resolution characteristics of RMS of DNL of metallic ratio samplings (noise 0.1%)

4.4.2 Evaluation Results of Prime Number Ratio

We obtain the resolution characteristics of the RMS of the DNL of the prime number ratio sampling. In this way, we can know the performance of the prime number ratio and the comparison with the metallic ratio.

Prime number ratio sample by a pair of relatively small prime numbers and prime number ratio sampling by a pair of relatively large prime numbers are the two cases that are investigated in this evaluation.

In the evaluation of prime number ratio samplings by a pair of relatively small prime numbers, the characteristics of the prime number samplings when f_{CLK}/f_{sig}= 23/13, 101/61, 199/127, 503/307 are evaluated. On the other hand, in the evaluation of prime number ratio samplings by a pair of relatively large prime numbers, the characteristics of the prime number samplings when f_{CLK}/f_{sig}= 997/991, 997/953, 997/907, 997/853, 997/751, 997/599, 997/389 are evaluated. Figs. 31, 32, 33, 34 show the characteristics of the prime number ratio samplings by a pair of relatively small prime numbers without noise, with 0.001% Gaussian noise, with 0.01% Gaussian noise, with 0.1% Gaussian noise, respectively.

Overall, in comparison to those of Fig. 4.1 of the metallic ratio samplings, the results of Fig. 4.5 of the prime number samplings by a pair of relatively small prime numbers have poor characteristics. Especially, the RMS of DNL of 101/61 is more than 1.

The pair of prime number values has a significant impact on the property. In the direction of the vertical axis, the curves spread out relatively widely.

In order to compare the prime number ratio samplings with the case in which the ratio is 10,000 where $f_{CLK} \gg f_{sig}$. Compared to the other characteristics, the rate of rise for characteristics is higher. The minimum value taken at $N = 256$ is close to the value of 199/127. The maximum value taken at $N = 16384$ is closes to the value of 101/61.

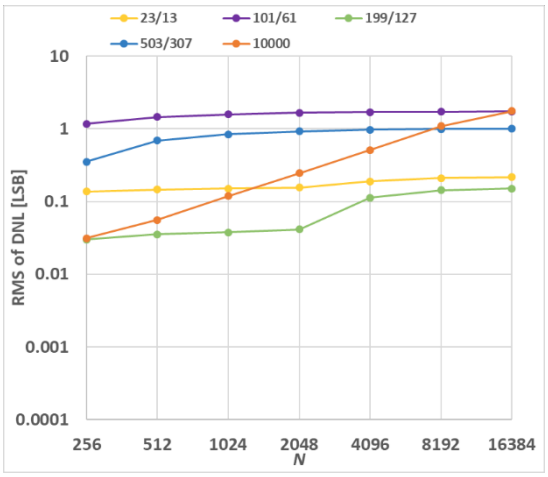

Fig. 4.5 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively smaller prime numbers (no noise)

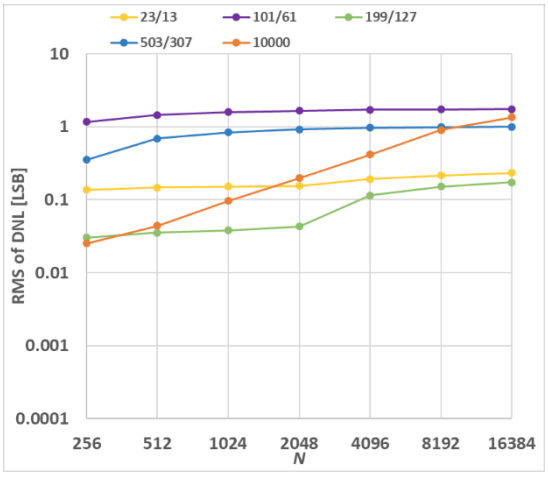

Fig. 4.6 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively smaller prime numbers (noise 0.001%)

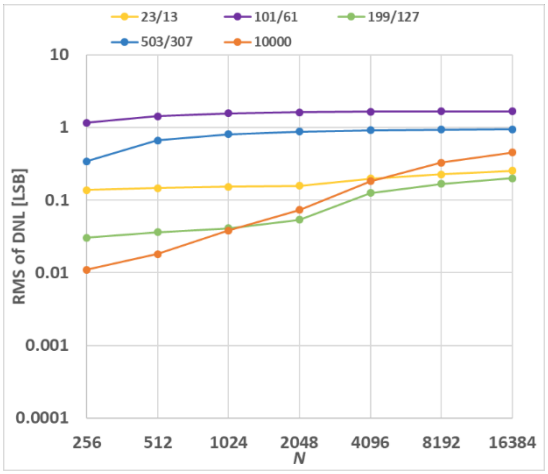

Fig. 4.7 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively smaller prime numbers (noise 0.01%)

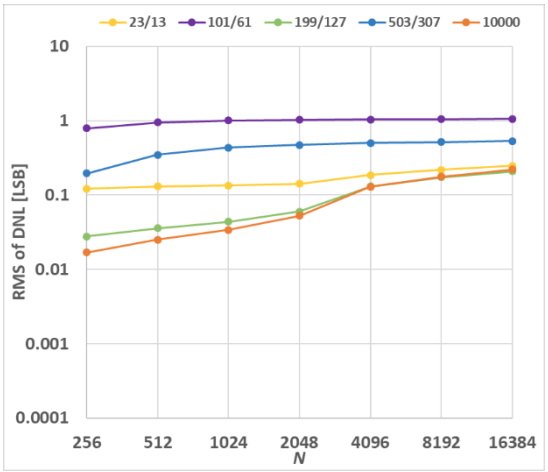

Fig. 4.8 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively smaller prime numbers (noise 0.1%)

The characteristics of prime number ratio samplings decrease as the noise level rises, and the vertical axis curves' vertical spread gradually narrows. On the other hand, as noise levels rise, the characteristics of 10000 progressively get better.

Figs. 4.9, 4.10, 4.11, 4.12 show the characteristics of the prime number ratio samplings by a pair of relatively large prime numbers without noise, with 0.001% Gaussian noise, with 0.01% Gaussian noise, with 0.1% Gaussian noise, respectively.

As shown in Fig. 4.9, the curves of the prime number ratio samplings by a pair of relatively larger prime numbers, as well as the curves on the lower domain when N is less than 4096, spread relatively widely in the vertical axis direction. However, The curves narrow on the higher domain, where N is more than 4096. The characteristics often decrease as the noise level rises, and the vertical axis curves' spread gradually narrows.

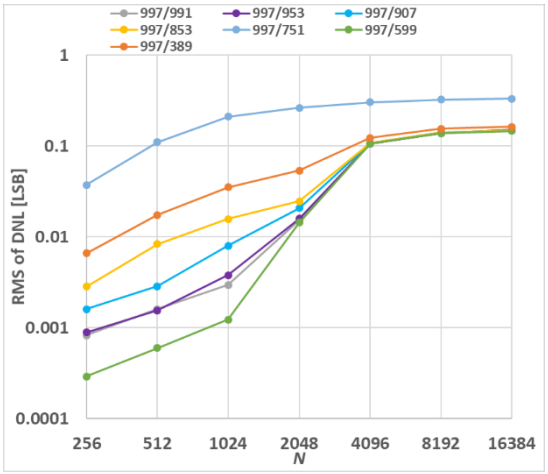

Fig. 4.9 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively larger prime numbers (no noise)

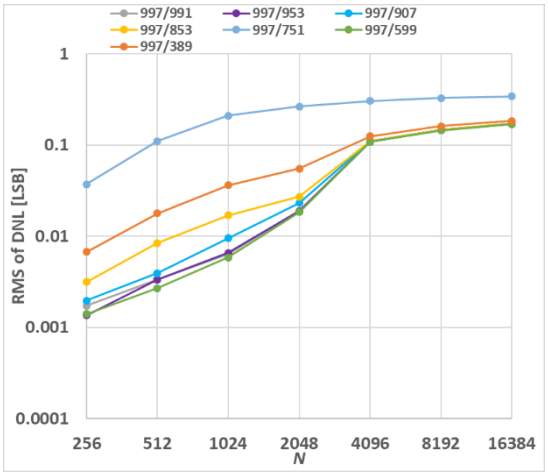

Fig. 4.10 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively larger prime numbers (noise 0.001%)

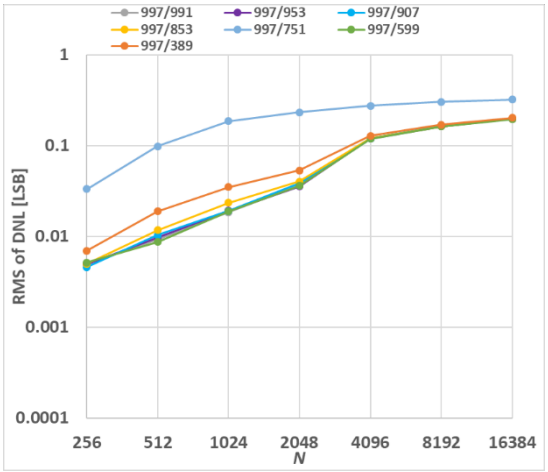

Fig. 4.11 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively larger prime numbers (noise 0.01%)

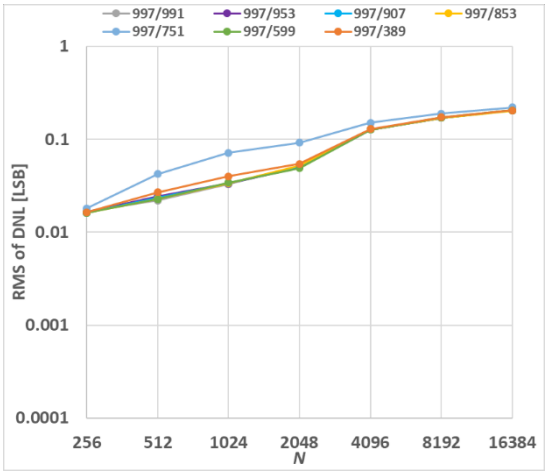

Fig. 4.12 Resolution characteristics of RMS of DNL of prime number ratio samplings by a pair of relatively larger prime numbers (noise 0.1%)

In the evaluation of the prime number ratio samplings, two metallic ratio samplings M_1 (golden ratio sampling) and M_8 with relatively good characteristics are compared with the prime number ratio sampling f_{CLK}/f_{sig}= 997/991 with the best characteristics. Figs. 4.13, 4.14, 4.15, 4.16 show the characteristics of these samplings, with 0.001% Gaussian noise, with 0.01% Gaussian noise, with 0.1% Gaussian noise, respectively.

These three samplings have nearly identical characteristics, as shown in Fig. 4.13. The worse the characteristics, the greater the noise. As more noise is added, the similarity of the characteristics grows.

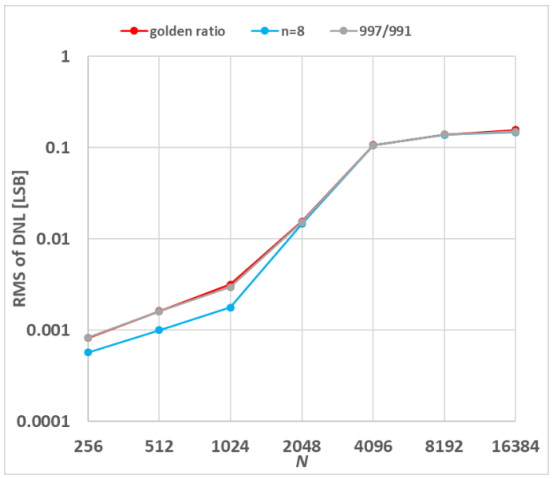

Fig. 4.13 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of prime number ratio sampling (no noise)

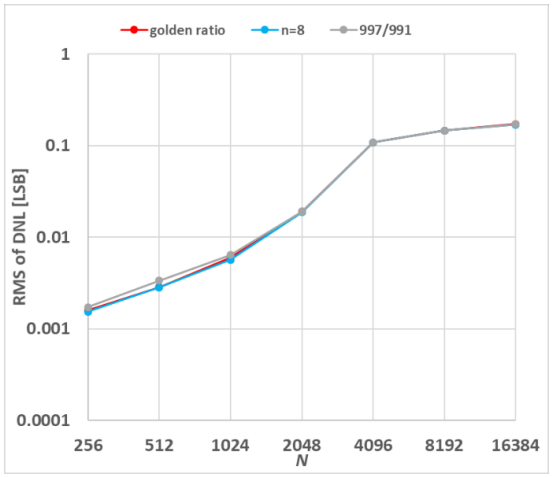

Fig. 4.14 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of prime number ratio sampling (noise 0.001%)

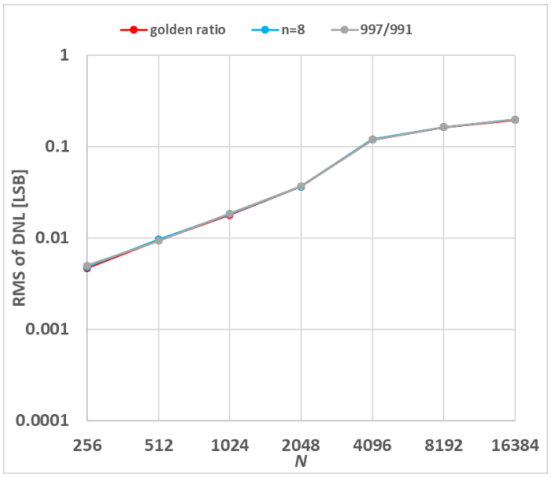

Fig. 4.15 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of prime number ratio sampling (noise 0.01%)

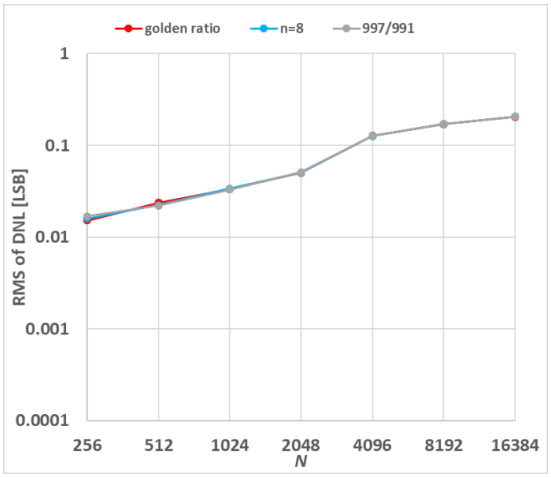

Fig. 4.16 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of prime number ratio sampling (noise 0.1%)

Here, let us call the sampling using the real number as the ratio f_{CLK}/f_{sig} the real number ratio sampling.

Finally, the real number ratio samplings are compared with two metallic ratio samplings M_1 (golden ratio sampling) and M_8, which have relatively

good characteristics. As the ratios for the real number ratio samplings in this evaluation, 8 real numbers in the range 1 to 10 where $M_n s(1 \leq n \leq 8)$ exist are generated randomly. Figs. 4.17, 4.18, 4.19, 4.20 show the characteristics of these samplings, with 0.001% Gaussian noise, with 0.01% Gaussian noise, with 0.1% Gaussian noise, respectively. The characteristics of the case when $f_{CLK}/f_{sig} = 10000$ are plotted on the same planes as the case where $f_{CLK} \gg f_{sig}$.

As shown in Fig. 4.17, the curves spread more widely in the direction of the vertical axis in the lower domain where N is less than 4096 compared to the higher domain where N is more than 4096. From all of the characteristics in Fig. 4.18, the characteristics of the two metallic ratio sampling are relatively better. It can be said that the characteristics of the real number ratio sampling are similar to the characteristics of the metallic ratio sampling. Compared to the characteristics of the case when $f_{CLK}/f_{sig} = 10000$, all the other characteristics are better. As more noise is increased, like the characteristics of the other sampling methods, the similarity of the characteristics becomes higher.

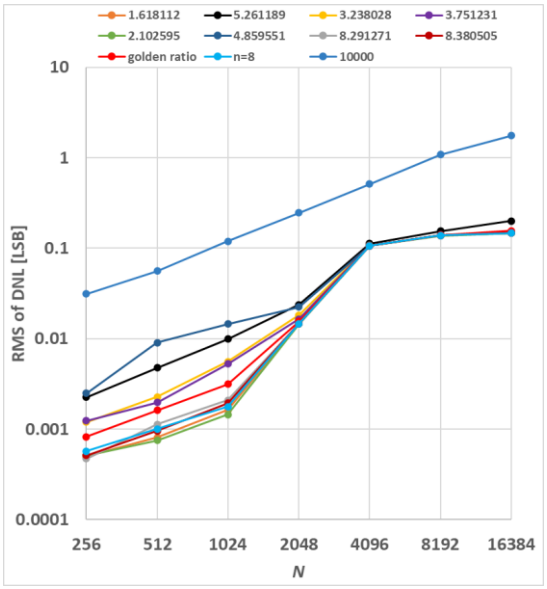

Fig. 4.17 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of real number ratio sampling (no noise)

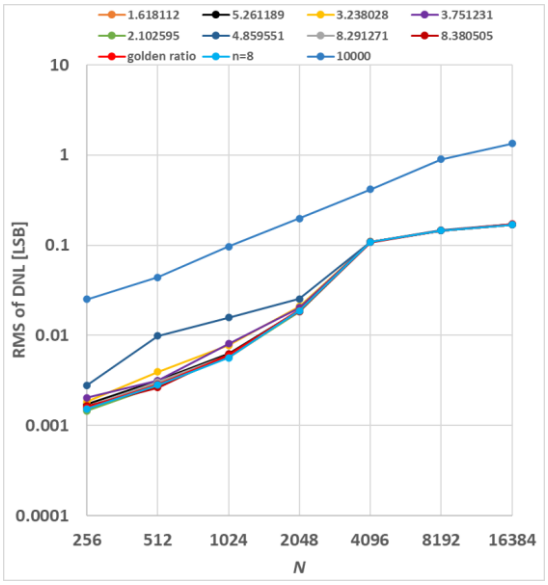

Fig. 4.18 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of real number ratio sampling (noise 0.001%)

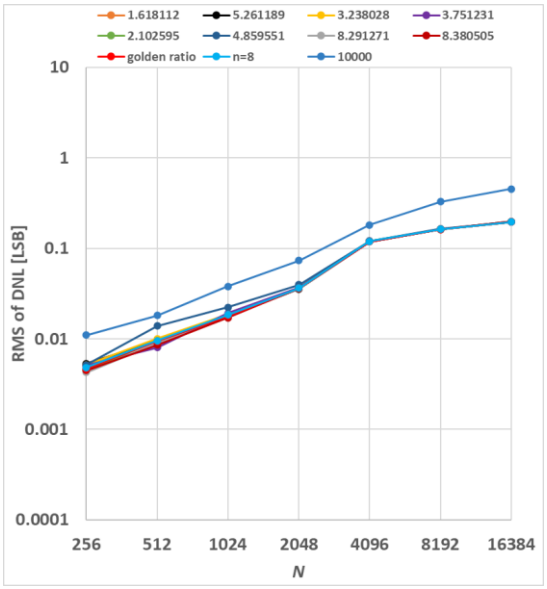

Fig. 4.19 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of real number ratio sampling (noise 0.01%)

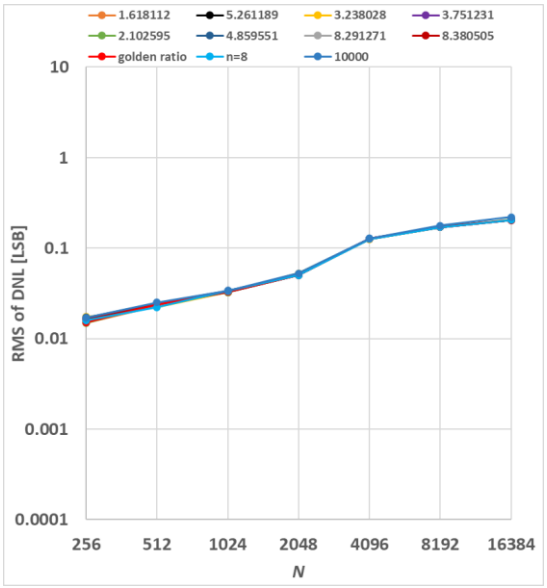

Fig. 4.20 Comparison of resolution characteristics of RMS of DNL of metallic ratio samplings with those of real number ratio sampling (noise 0.1%)

4.5 Summary

In this chapter, through the use of simulations, we have investigated numerous ratios between the input signal frequency and the sampling frequency, including metallic ratios and prime number ratios, and compared with the case of $f_{CLK} \gg f_{sig}$ ($f_{CLK}/f_{sig} = 10000$). In evaluation, with the same total number of samples (test time), each ratio has different sampling accuracy. Metallic ratio has better performance with better accuracy (RMS of DNL is small). This means that with the same accuracy, no more total number of samples is required, and no higher frequency is required to sample uniformly. So, it is possible to shorten the time by reducing the total number of samples while maintaining the same accuracy. And it has come across a number of intriguing results. In the event of small N, the metallic ratios perform similar in specific positions (32, 64, 128, 256, …).

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[5] M. Leonard Eugene Dickson: History of the Theory of Numbers, vol. 2, Diophantine Analysis, Dover, 2005.

Chapter 5 Conclusions and Future Work

5.1 Conclusions

This dissertation has introduced relatively simple methods of focusing histogram sampling on specific codes.

Chapter 3 proposes that the two-tone sine wave input for code selective histogram method, which is the first proposal. In order to perform a quick ADC linearity test, our proposal synthesizes a two-tone wave. Simulations confirmed the efficacy and performance of the proposed code selective histogram method. Additionally, we created a program to test our algorithm, and the outcomes of our simulations demonstrated the efficiency and performance of the code selective histogram approach. In the case of the same total number of samples, compared with the conventional sine wave method, the proposed method increases the sample number of the target code, while at the same time reducing the number of other samples, and also reducing its measurement accuracy. Taking f_{11} in Eq. 3-12 as an example, this method only corresponds to 255, 767 and 511 in 10-bit (1024). In this case, it may cause a test escape. So, well-balanced consideration would be needed as a future work.

Chapter 4 presents decision of the ratio between input and sampling frequencies based on classical number theory, which is the second proposal. Simulations with our developed programs were used to examine a variety of ratios, including metallic and prime number ratios, between the input signal

frequency and the sampling frequency. These simulations can be applied to increase test accuracy with fewer samples., Previous research has shown that golden ratio sampling has a high DNL measurement accuracy. In these simulations, metallic ratio sampling also has high DNL measurement accuracy, but prime number ratio sampling accuracy is lower. In many cases of analog device testing, sampling and/or input sine wave frequencies have to be changed. Set their ratio to one of metallic ratios (n=1, 2, 3, 4….). Then good measurement accuracy is obtained.

Code selective histogram method performs better at output code prone to nonlinearities in evaluation with the same total number of samples (test time), higher accuracy, and more samples. The metallic ratio performs better and is more accurate when compared to the other ratios' sampling accuracy (the RMS of DNL is small). This means that the proposed method does not need more total samples or a higher sampling frequency to obtain sample uniformly. Additionally, it is possible to decrease the total number of samples while keeping the accuracy same.

5.2 Future work

Even though we have obtained positive simulation results, there is still much work to be done before it can be effectively applied to actual ADC testing. There are still many obstacles to be overcome as well as numerous areas that need to be enhanced and considered. The next step we want to take is validation in more examples and application in actual circuits.

If the testing at the specific codes of ADC under test is very important, an alternative method is to use their corresponding DC signals as the input signal. The investigation of its testing system and comparison with the proposed code selective method would be left as future works.

We conclude this paper by noting that although the histogram method for the ADC linearity test is a mature technology and is widely used in industry, there can still be new algorithms and findings that are regarded as being favorable to industry.

List of Publications

Journal Paper

[1] **Yujie Zhao**, Kentaroh Katoh, Anna Kuwana, Shogo Katayama, Jianglin Wei, Haruo Kobayashi, Takayuki Nakatani, Kazumi Hatayama, Keno Sato, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa, “Revisit to Histogram Method for ADC Linearity Test: Examination of Input Signal and Ratio of Input and Sampling Frequencies”, Journal of Electronic Testing: Theory and Applications, Springer, (March 2022).

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Review Paper

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International Conference

[1] **Yujie Zhao**, Kentaroh Katoh, Anna Kuwana, Shogo Katayama, Daisuke Iimori, Yuki Ozawa, Takayuki Nakatani, Kazumi Hatayama, Haruo Kobayashi, Keno Sato, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa, "Evaluation of Code Selective Histogram Algorithm For ADC Linearity Test", The Seventh International Conference On Consumer Electronics (ICCE) Asia (ICCE-Asia), South Korea, hybrid mode (Both on-site and online), (Oct. 26-28, 2022).

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Domestic Conferences / Seminars

[1] **趙 宇杰**、桑名 杏奈、魏 江林、片山 翔吾、佐藤 賢央、石田 嵩、岡本 智之、市川 保、中谷 隆之、畠山 一実、小林 春夫、「コード選択ヒストグラム法: 2 トーン入力信号を用いた ADC 線形性テストの時間短縮」、第 35 回多値論理とその応用研究会、オンライン（2022 年 1 月 8 日）

[2] **趙 宇杰**、桑名 杏奈、山本 修平、佐々木 優斗、小林 春夫、ャン ミン チー、片山 翔吾、魏 江林、中谷 隆之、畠山 一実 (群馬大学)、佐藤 賢央、石田 嵩、岡本 智之、市川 保 （ローム (株)）、「ヒストグラム法による効率的 ADC 試験のための入力周波数とサンプリング周波数の関係の検討」、第 83 回 FTC 研究会、オンライン（2021 年 7 月 16 日）

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Award

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(BEST STUDENT PRESENTATION AWARD)