学 位 論 文 の 要 旨

ADC and DAC Design Based on Classical Mathematics
古典数学に基づく AD 変換器および DA 変換器の設計

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This dissertation describes analog-to-digital converter (ADC) design and digital-to-analog converter (DAC) design based on classical mathematics, and their simulation verifications. The designed ADC and DAC are very different from conventional ones and they can be useful for some applications.

The first part shows an asynchronous capacitive successive-approximation-register (SAR ADC) based on Hopfield network. The ADC is a key circuit for interface between analog and digital worlds. Much attention has been paid to the SAR ADC due to small chip area and low power as well as no need for operational amplifier, and its figure of merits has been improved. On the other hand, the Hopfield network has been investigated as an ADC architecture for several tens of years, but it has not been widely used in practice. Then we have investigated an N-bit asynchronous SAR ADC based on an asymmetric Hopfield network with only feedforward paths but without feedback paths to avoid the local minima problem. Conventional Hopfield network SAR ADC is composed of resistors whose values are required to be several tera ohms for easy drive; however, this makes its implementation on standard CMOS LSI to be difficult.

Then we have proposed and investigated switched capacitor type asynchronous SAR ADC instead of resistor type. This can be implemented with small chip area, which makes the proposed one to be practical in industry use. In N-bit resolution case, it uses N CMOS inverter-type comparators operating in parallel (with higher bits look-ahead for lower bits generation) and asynchronously without SAR logic or a high frequency internal clock, which leads to high-speed ADC operation.
Compared to the flash ADC which is the fastest, the circuit size and power consumption of the proposed ADC can be significantly reduced with comparable speed. Also, by designing the comparator with chopper type one, the proposed SAR ADC can be implemented with standard digital CMOS process without analog options, which leads to low supply voltage operation and low cost. The proposed ADC circuit configuration and operation are derived and circuit simulation verifications with standard CMOS SPICE parameters are shown,

The proposed ADC architecture has been derived from the Hopfield network which is one of classical neural networks. It has well-balanced performances, whose possible applications are wide such as consumer, industry, automotive and medical electronics. Also, the proposed ADC can be extended to a non-binary weighted structure. Since it has some redundancy, its reliability is improved which is suitable for automotive applications.

The second part shows derivation of two DAC architectures based on number theory. The first DAC is based on polygonal number theorem and the second DAC is based on the Goldbach conjecture about even numbers and prime numbers. Both DACs are composed of a resistor network, several current sources and corresponding switch arrays and decoder circuits. Their properties are placed between unary DAC ones and binary DAC ones. We have shown new DAC architecture derivation from number theory to validate our argument that classical mathematics can explore new analog and mixed-signal circuit design; this attempt leads to new DAC architecture derivation methodology.

We have proposed and investigated the DAC configurations based on the polygonal number theory: "Any natural number is composed of N or less than N N-polygonal numbers". The DAC consists of N current sources, N switch arrays, an N-polygonal number weighted resistor network, and decoder (N= 3, 4, 5, ...). We take the triangular number (N=3) as an example, and infer that this consideration is applicable to other polygonal numbers through theoretical analysis and simulation results of the triangular number. We have designed a N-polygonal resistor network and decoder circuits. The whole DAC circuit operation is verified with circuit simulations.

We have also proposed and investigated the DAC configuration based on the Goldbach conjecture: "All even numbers can be represented by the sum of two prime numbers." The DAC consists of 2 current sources, 2 switch arrays, a prime number weighted resistor network, and decoder circuits. We have designed a prime number resistor network and decoder circuits. The whole DAC circuit operation is verified with circuit simulations. Also, the possibility of dynamic element matching (DEM) technique usage to take care of the device mismatch effects is described.

There are several interesting classical neural networks, but they have not been used in actual applications. Here the Hopfield network together with switched capacitor circuits can be applied to practical ADC. Also, there are many interesting properties in natural numbers, but they have not been fully exploited for DAC design. Here new DAC architectures have been derived from the polygonal number theory and the Goldbach conjecture. Their operations have been confirmed with circuit simulations.