ADC and DAC Design Based on Classical Mathematics

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PhD Dissertation

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ADC and DAC Design Based on Classical Mathematics

DISSERTATION

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Declaration

I hereby undertake: This dissertation is my own research work.

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Part 1 Asynchronous Capacitive SAR ADC Based on Hopfield Network

Abstract

This part revisits a Hopfield network for an SAR ADC configuration, which enables fast operation, low supply voltage (as below as CMOS switches can work) and low power with small circuitry. The proposed SAR ADC employs an asymmetrical Hopfield network to avoid local minimum, and it uses capacitors and switches instead of very large resistors. Our N-bit SAR ADC uses N chopper-type comparators for asynchronous parallel operation with higher bits lookahead capability in lower bits generation circuits, which is different from the conventional asynchronous SAR ADC employing only one comparator with sequential operation from MSB to LSB. Our SAR ADC requires only the sampling clock for each input data sampling; no internal high frequency clock is required. Its AD conversion time is determined only by the comparator delays and the capacitor charge/discharge settling times; hence it is very fast, and the AD conversion latency is only one or two clock cycles. Its operation is verified with SPICE simulations.

Organization

In this part, the research background and motivation are introduced and dissertation organization in Chapter 1.

In Chapter 2, the A/D conversion principle, the evaluation criteria for ADCs, and the structure and application scenarios of different ADCs are introduced.

In Chapter 3, we compare this study with traditional ADC and synchronous ADC and explain what improvements have been made and what aspects have been optimized in this study compared with the previous asynchronous resistance ADC.

In Chapter 4, the results of this study are recorded.

Chapter 5 shows discussions and conclusions.

Part 2 Derivation of Digital-to-Analog Converter Architectures Based on Number Theory

Abstract

This part investigates possibilities of deriving new digital-to-analog converter (DAC) architectures based on polygonal and prime number theories. As the result, configurations of polygonal number DACs and prime number DACs are obtained; each consists of a few current sources, a resistor network, switch arrays and a decoder circuit. Whole circuits are designed, and their operations are confirmed with simulation; they work as DAC in principle, and most of their circuits consist of digital circuit, which is suitable for implementation with Nano-CMOS process. We demonstrate that it is feasible to derive different DAC architectures from conventional ones based on some interesting properties of integers. The proposed polygonal number and prime number DACs would be placed between binary and unary DACs in terms of circuit size and possibly performance.

Organization

Chapter 1 introduces the research motivation and background of this topic and summarizes the research results of applying classical mathematics to analog/mixed signal circuit design.

Chapter 2 introduces the basic composition and configuration of DAC and explains the common errors of DAC.

Chapter 3 introduces Polygonal Number Theory, Polygonal Number DAC and General Polygonal Number DAC, as well as composition, calculation method, simulation results, decoder verification results.

Chapter 4 introduces Prime Number Theory, Prime Number DAC as well as composition, calculation method, simulation results, decoder verification results.

Chapter 5 shows the conclusions.

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Part 1

Asynchronous Capacitive SAR ADC Based on Hopfield Network

Chapter 1

Introduction

Research Background and Motivation

An analog signal, which is a major part in the natural world, is only a noise when entering a digital integrated circuit. If you want to express your ideas overseas accurately, you must express them in the language of that country. In the same way, in digital integrated circuits such as DSP and CPU, it doesn't make sense unless it talks with the standard language used in the world. Analog signals converted into digital values through this conversion process are processed in DSP and CPU, then recorded on storage medium, and transmitted to remote places, such as radio.

ADC and DAC are key components indispensable for constructing various signal processing systems. This is because signal processing in the electronic system is carried out digitally by the advance of the recent integrated circuit technology. In the past, ADC and DAC have been sold as special expensive single parts and are used by system engineers to assemble the system, but in recent years the miniaturization of semiconductor integrated circuits has progressed and almost all systems have been realized on an integrated circuit. It is a problem of the continuance that the ADC and DAC are put on the integrated circuit at the time, and the high performance is put in the low chip power consumption in the small chip area, and it is always required in the electronics of the small and low power consumption.

There are five main types of ADC currently in use. Successive-approximation register (SAR) ADC, Sigma-delta, Flash ADC, Integrating ADC and Pipelined ADC.

ADC and DAC are essential components of various signal processing systems. This is because although the signals in nature are analog signals, due to the progress of integrated circuit technology in recent years, digital signal processing in electronic systems has various advantages. In the past, ADC and DAC were sold as single components with special high prices and used by system technicians to assemble systems. However, in recent years, with the miniaturization of semiconductor integrated circuits, almost all

systems are implemented on integrated circuits. At this time, how to carry ADC and DAC on integrated circuits with small chip area and low power consumption on high-performance circuits is an eternal topic often needed in electronics.

The SAR ADC as a goal of this study is often chosen as an architectural choice in medium to high resolution applications with sample rates less than 5 MSPs. The most commonly used 8-16 bit resolution SAR ADCs provide low power consumption and compact shape. The main advantages of SAR ADCs are low power consumption, high resolution, high precision, and small size. These advantages enable SAR ADCs to often be integrated with other larger functions. The combination of these features provides an ideal ADC for a wide range of applications, such as portable battery drives, pen digitizers, industrial controls, and data / signal collection.

In this paper, we show the performance of an asynchronous SAR ADC of faster operation, but comparable supply voltage (as below as CMOS switches can work), power consumption, circuit size to the conventional synchronous SAR ADC.

The ADC is a key circuit for interface between analog and digital worlds [1, 2, 3]. Much attention has been paid to the SAR ADC due to small chip area and low power as well as no need for operational amplifier [4-18], and its figure of merits (FOM) has been improved. The Hopfield network has been investigated as an ADC architecture for several tens of years [19-24], but it has not been widely used in practice. Then we have investigated an N-bit asynchronous SAR ADC based on an asymmetric Hopfield network with only feedforward paths but without feedback paths to avoid the local minima problem [25]. It uses N CMOS inverter-type comparators operating in parallel and asynchronously without SAR logic or an internal clock, which leads to high-speed operation. It can also realize a non-binary weighted ADC However, it uses many resistors with huge values (Giga or Tera Ohm order) for easy drive by the inverters and hence it consumes large chip area.

Based on these observations, we propose here an asynchronous SAR ADC with capacitors, switches and inverter-type comparators but without resistors; in other words, the resistors are replaced with capacitors and switches. It is expected to keep the above advantages of high-speed operation and simple configuration, and to overcome the disadvantage of large resistor usage. The

proposed ADC circuit configuration, operation and simulation results with some considerations are shown.

Chapter 2

ADC Performance Index [32]

Fig. 2.1 shows a basic system of the present electronic apparatus, where an analog signal is processed by a digital signal and returned to an analog signal again.

In general, the ADC can be equipped with a Variable-Gain Amplifier (AGC), in which a pre-filter is set to prevent frequency interruption due to sampling, and the amplitude of the signal can be appropriate. The output of the D/A converter is placed in the post filter to prevent frequency interruption.

The A/D conversion requires two processes: sampling and quantization, as shown in Fig. 2.2.

Sampling refers to sampling the value of the input analog signal at a certain period of time. Quantization refers to rolling the value of the input analog signal into a finite resolution value. Sampling refers to the discretization of the time direction, while quantization refers to the discretization of the signal size such as voltage and current. Two discretization are performed.

D/A transformation in this inverse process, the analog values (voltage, current, etc.) corresponding to the values with limited resolution are output at a fixed time in a specified period.

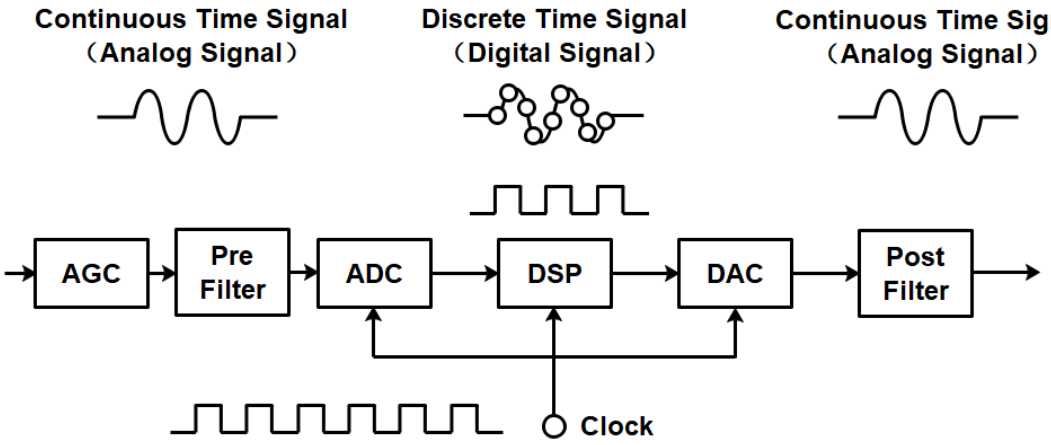
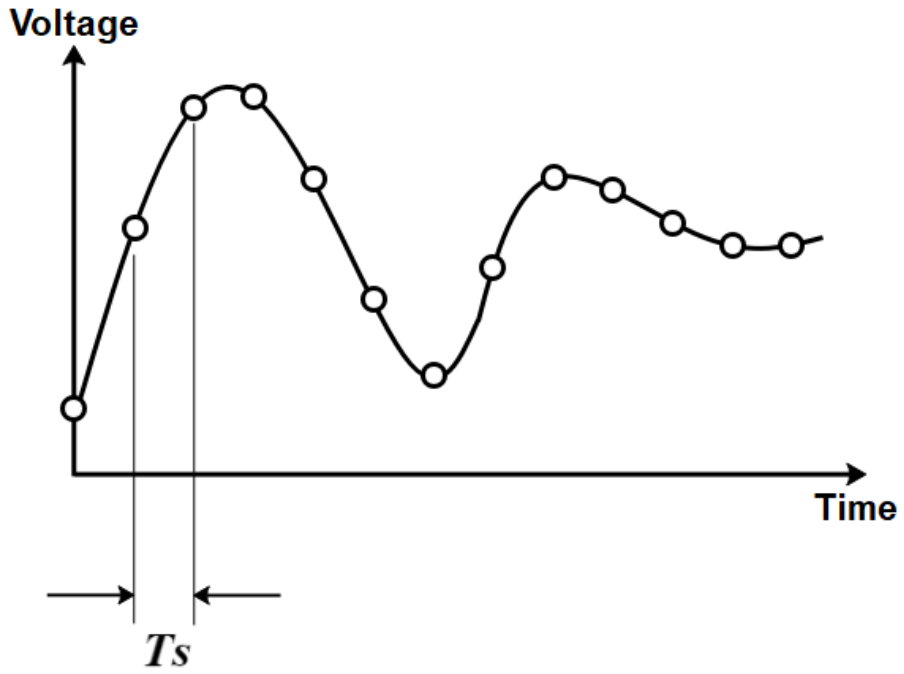
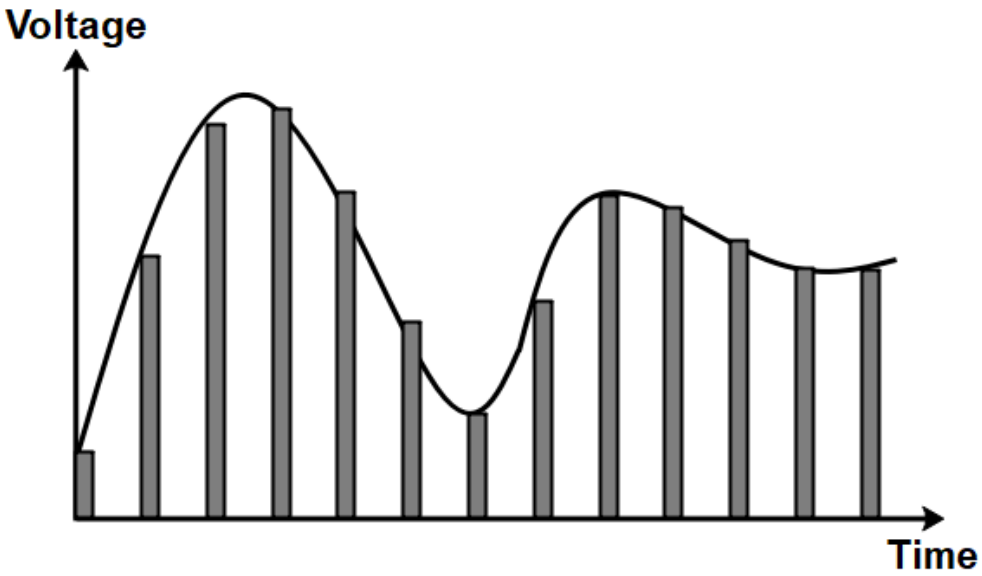


Figure 2.1 Composition of signal processing system using AD/DA converters and DSP



(a) Sampling



(b) Quantization

Figure 2.2 Sampling and quantization

2.1 Sampling

As shown in Fig. 2.3, when the analog signal $x(t)$ is sampled at a constant interval T_s, a sampling column $x(n)$ is obtained.

2.1.1 Performance in Time Domain

The reciprocal of T: $f_s = 1/T_s$ is called the sampling frequency, and $w_s = 2\pi/T_s$ is called the sampling angular frequency.

If the sampled signal $x_s(t)$ is represented by a pulse train, as shown below:

$$x_s(t) = \sum_{n=-\infty}^{\infty} x(t)\delta(t - nT_s) = \sum_{n=-\infty}^{\infty} x(n)\delta(t - nT_s) \qquad (2\text{-}1)$$

The properties of impulse function can also be shown as follows:

$$x_s(t) = x(t)\delta_T(t) \qquad (2\text{-}2)$$

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \qquad (2\text{-}3)$$

The sampling can be regarded as the multiplication of the analog signal $x(t)$ and the impulse string $\delta_T(t)$.

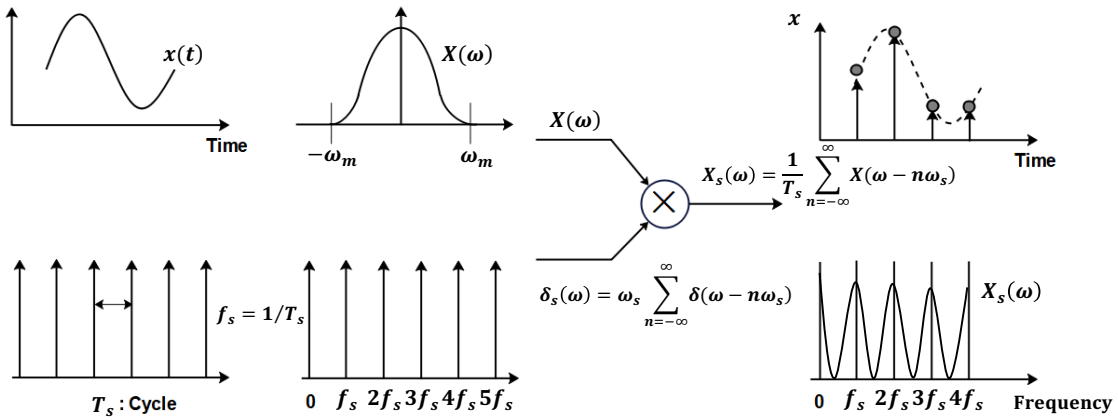


Figure 2.3 Role of sampling (time domain and frequency domain)

2.1.2 Performance in Frequency Domain

The relationship between the spectrum $X_s(\omega)$ and the spectrum $X(\omega)$ of the original signal $x(t)$ is obtained.

Since the impulse sequence $\delta_T(t)$ is a periodic function of the period T_s, it is developed into a Fourier series. The Fourier coefficient C_n is,

$$C_n = \frac{1}{T_s}\int_{-\frac{T_s}{2}}^{\frac{T_s}{2}} \delta_T(t) e^{-jn\omega_s t} dt = \frac{1}{T_s}\int_{-\frac{T_s}{2}}^{\frac{T_s}{2}} \delta(t) e^{-jn\omega_s t} dt = \frac{1}{T_s} \quad (2\text{-}4)$$

Thus, Fourier series expansion is

$$\delta_T(t) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} e^{jn\omega_s t} \quad (2\text{-}5)$$

Fourier transform is

$$\delta_s(\omega) = \int_{-\infty}^{\infty} \delta_T(t) e^{-i\omega t} dt$$

$$= \frac{1}{T_s}\int_{-\infty}^{\infty}\sum_{n=-\infty}^{\infty} e^{jn\omega_s t}\cdot e^{-i\omega t}dt = \frac{1}{T_s}\sum_{n=-\infty}^{\infty}\int_{-\infty}^{\infty} e^{i(n\omega_s-\omega)t}dt$$

$$= \frac{2\pi}{T_s}\sum_{n=-\infty}^{\infty}\delta(\omega - n\omega_s) = \omega_s\sum_{n=-\infty}^{\infty}\delta(\omega - n\omega_s) \quad (2\text{-}6)$$

On the other hand, since the signal $x_s(t)$ is the product of two signals $x(t)$ and $\delta_T(t)$, the vector $X_s(\omega)$ is used with the complex convolution integral.

$$X_s(\omega) = \frac{1}{2\pi}[\delta_s(\omega) * X(\omega)]$$

$$= \frac{1}{2\pi}\int_{-\infty}^{\infty}\left[\omega_s\sum_{n=-\infty}^{\infty}\delta(u - n\omega_s)\right]X(\omega - u)du \quad (2\text{-}7)$$

$$= \frac{1}{T_s}\sum_{n=-\infty}^{\infty}X(\omega - n\omega_s)$$

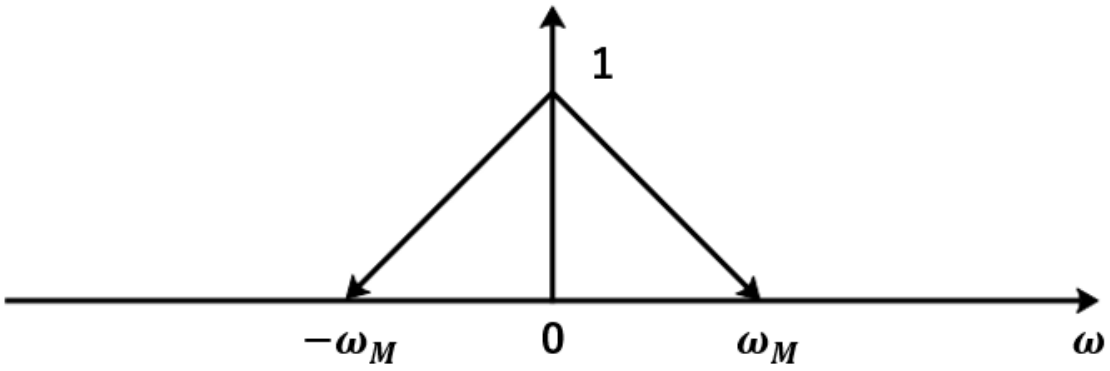
Thus the spectrum $X_s(\omega)$ of signal $X_s(t)$ is, as shown in Fig. 2.3, the spectrum $X(\omega)$ of the analog signal $x(t)$ before sampling was placed on the frequency axis at intervals ω_s. It becomes a periodic function of the periodic ω_s.

2.1.3 Sampling Theorems and Folding

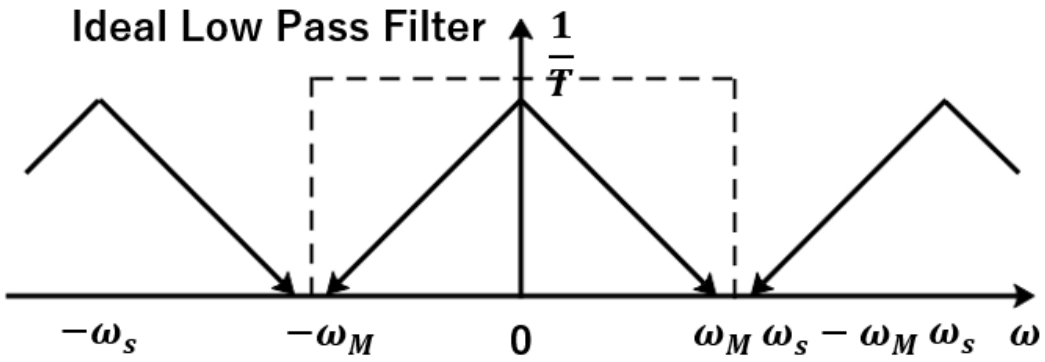
The Fourier transform $X_s(\omega)$ of the signal $x(t)$ corresponds to a certain angular frequency ω_M. When the following conditions are met, the signal $x(t)$ is limited by the frequency band.

$$X(\omega) = 0, |\omega| \geq \omega_M \quad (2\text{-}8)$$

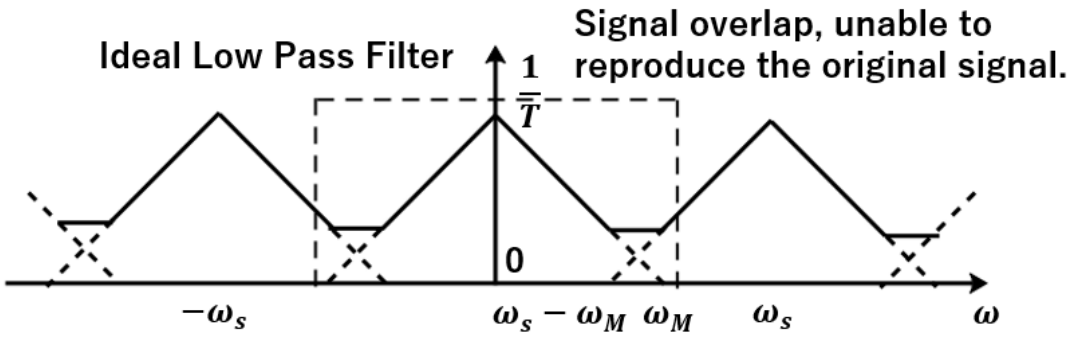
The frequency spectrum $X_s(\omega)$ of the sampled signal obtained by sampling the analog signal $x(t)$ with the angular frequency $\omega_s = \frac{2\pi}{T_s}$ is given by Eq (2-7). Now, as shown in Fig. 2.4, if $x(t)$ is a band limiting signal, if $\omega_s > 2\omega_M$, it is re configured on the frequency axis without overlapping. However, if $\omega_s < 2\omega_M$, spectral overlap will occur as shown in Fig. 2.4 (c). In this state, the signals overlap and the original signals cannot be reproduced.



(a)



(b)



(c)

Figure 2.4 Spectrum of original signal and sampled signal

Sampling Theorems:

Suppose that signal $x(t)$ is a band limited signal. That is, when the following conditions are met, $x(t)$ uses the sampling value $x(n)$ in $t = \frac{n\pi}{\omega_M} = nT_s$ (n is an integer), we obtain the followings:

$$x(t) = \sum_{n=-\infty}^{\infty} x(n) \frac{sin\{\omega_M(t-nT_s)\}}{\omega_M(t-nT_s)} = \sum_{n=-\infty}^{\infty} x(n) S_a\{\omega_M(t-nT_s)\} \quad (2\text{-}9)$$

Here, $S_a(x) = \frac{\sin x}{x}$.

When the signal band of the original signal is smaller than 1/2 of the sampling frequency due to the sampling, the original signal can be reproduced by using the ideal low pass filter as shown in Fig. 2.4 (b). This is called folding. Therefore, if the ADC is used, it is necessary to suppress the frequency component which causes the folding by the filter.

Fig. 2.5 shows the state of the folded back when the signal of 3 MHz including the harmonic is converted at 8 MHz. Although the frequency of the signal of 3 MHz is unchanged, the signal of 6 MHz of the second harmonic is 2 MHz, the signal of 9 MHz of the third harmonic is 1 MHz, and the signal of 12 MHz of the fourth harmonic is folded back to 4 MHz. If the frequency of the converted signal is f_a and the conversion frequency is f_s, the converted frequency f_b is as follows:

$$\begin{gathered} f_b = f_a - nf_s : nf_s \le f_a < (n+\frac{1}{2})f_s \\ f_b = (n+1)f_s - f_a : (n+\frac{1}{2})f_s \le f_a < (n+1)f_s \\ n = 0, 1, 2, \ldots \end{gathered} \quad (2\text{-}10)$$

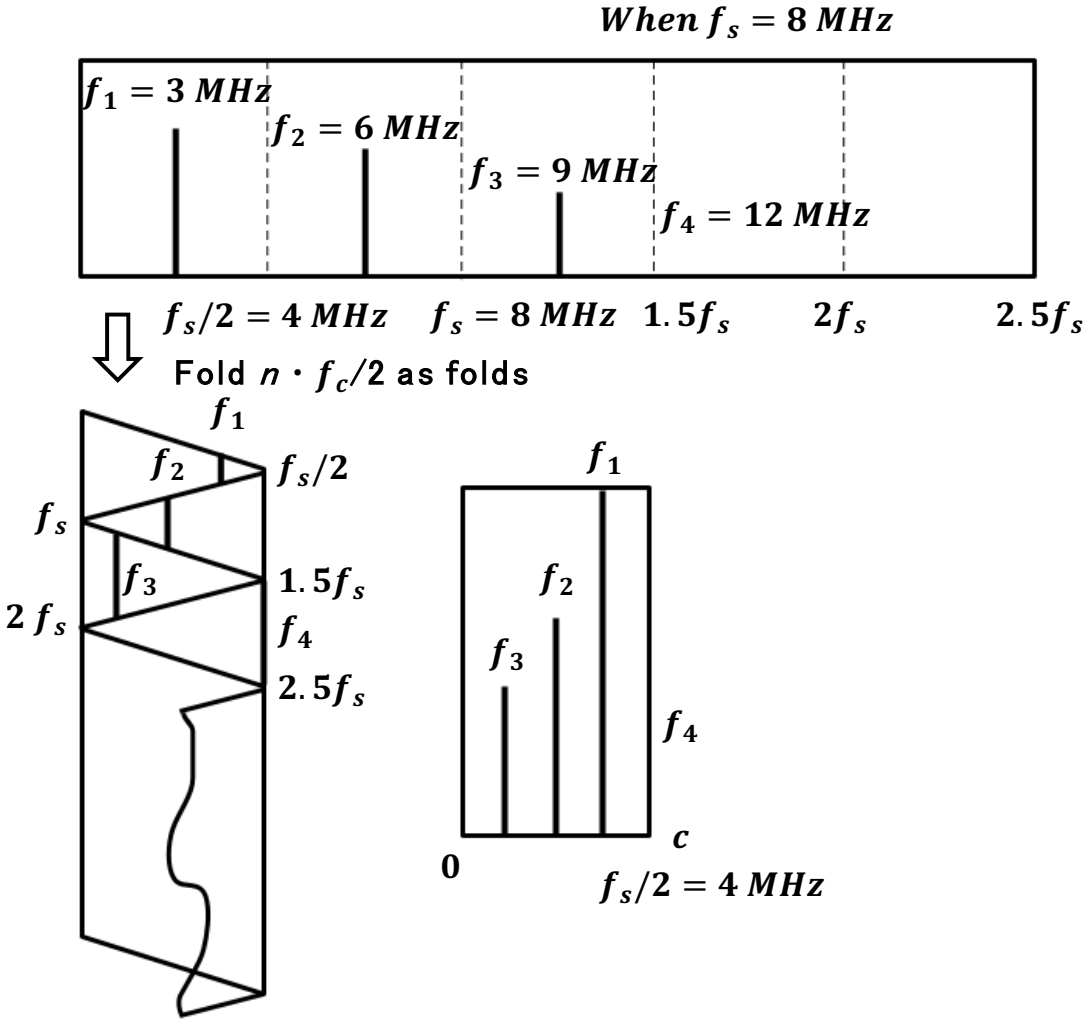


Figure 2.5 Turn-back when converting 3MHz signal containing high-order harmonics to 8MHz

2.1.4 Over Sampling

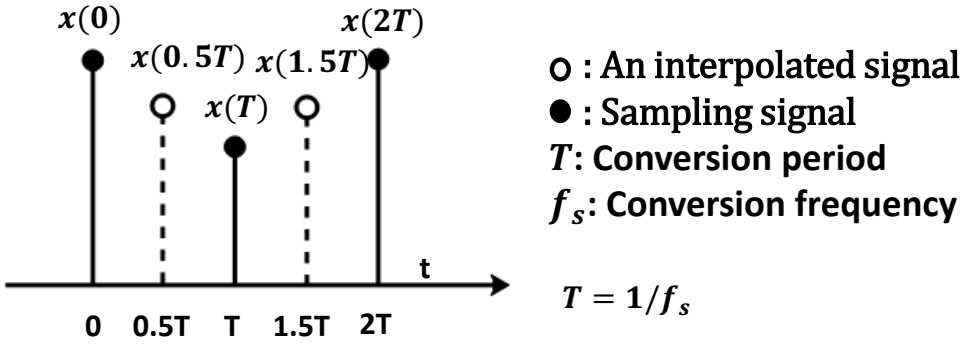
It is called oversampling if the conversion frequency is more than twice of the signal frequency band.

In A/D conversion, in order to avoid folding, a low-frequency filter is required to fully reduce signals with frequencies above $\frac{f_s}{2}$. However, if the conversion frequency is about twice as low as the signal frequency band, the implementation of the filter becomes difficult (an ideal filter cannot be done

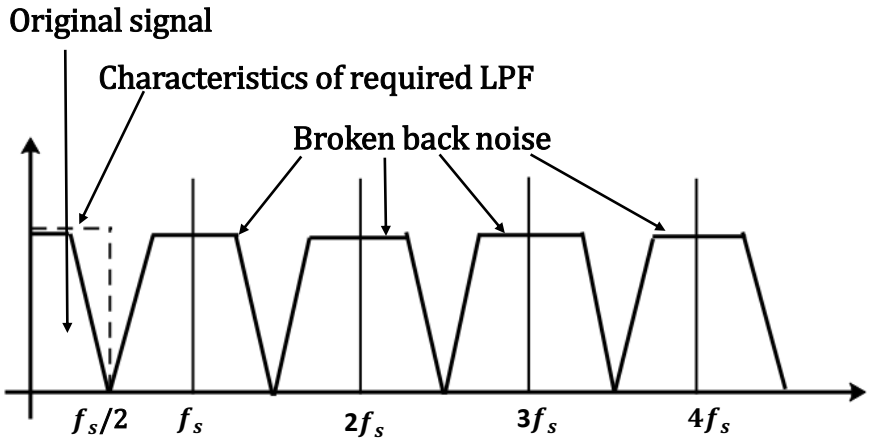
in reality). Therefore, in fact, the conversion frequency is more than 3 times of the signal frequency band.

In addition, in the D/A transformation, due to the folding of the frequency spectrum of the regenerated signal, as shown in Fig.2.6 (b), a sideband based on the original signal is generated around the frequency nf_s which is n times the sampling frequency. Therefore, a filter is required to attenuate these turn-back components. However, because the separated signal frequency is too close, it is difficult to simply use a filter to attenuate. Therefore, a digital filter is used to process the sampled signal and synthesize the interpolated signal represented by a white circle.

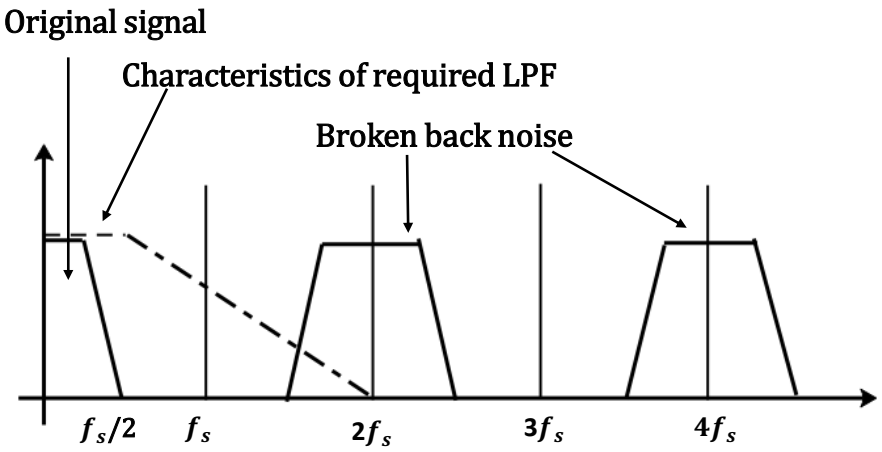
Through this processing, the sample size is 2 times from the appearance, so as shown in Fig. 2.6 (c), the repetition frequency of the turn back signal is 2 times. Because the turn-back signal is separated, even low-order low-frequency filters can fully attenuate the turn-back signal.



(a) Reproduced signal and interpolation



(b) Characteristics of spectrum modulated LPF



(c) Spectrum of oversampled signals

Figure 2.6 Reproduction signal and signal spectrum during oversampling

2.2 Quantization

During A/D conversion, as shown in Fig. 2.7, the continuous value is converted to the quantized value. Therefore, the triangle part in the figure will produce errors. This is called quantization error.

This quantization error needs to be treated as distortion when the input signal and the sampling signal have some correlation, but most of it can be treated as noise when it can be regarded as a random signal. Therefore, the size of the noise accompanying the quantization and its ratio to the signal, Signal-to-Noise Ratio (SNR) is calculated.

If the quantization error is uniformly distributed between $-\frac{q}{2}$ and $\frac{q}{2}$ as shown in Fig. 2.8, then its probability density function $p(x)$ is given by

$$p(x) = \begin{cases} \frac{1}{q}, & |x| \le \frac{q}{2} \\ 0, & |x| > \frac{q}{2} \end{cases} \tag{2-11}$$

Probability average power, quantization noise N_q is,

$$N_q = \int_{-\frac{q}{2}}^{\frac{q}{2}} x^2 p(x) dx = \frac{1}{3}(\frac{q}{2})^2 = \frac{q^2}{12} \tag{2-12}$$

On the other hand, when the full-scale sinusoidal signal input is added to the ADC, the signal power S has N as the resolution of the ADC.

$$S = \frac{1}{2}(\frac{2^N q}{2})^2 = 2^{(2N-3)} q^2 \tag{2-13}$$

Therefore,

$$\frac{S}{N_q} = 1.5 \cdot 2^{2N} \quad (2\text{-}14)$$

It is expressed in dB, as follows:

$$SNR = 10\,log\left(\frac{S}{N_q}\right) = 20Nlog^{2N} + 10log1.5 = 6.02N + 1.76(dB) \quad (2\text{-}15)$$

That is, with the resolution N increasing by 1 bit, the SNR increases by about 6dB. One of the reasons for requiring a high-resolution ADC is to obtain this high SNR.

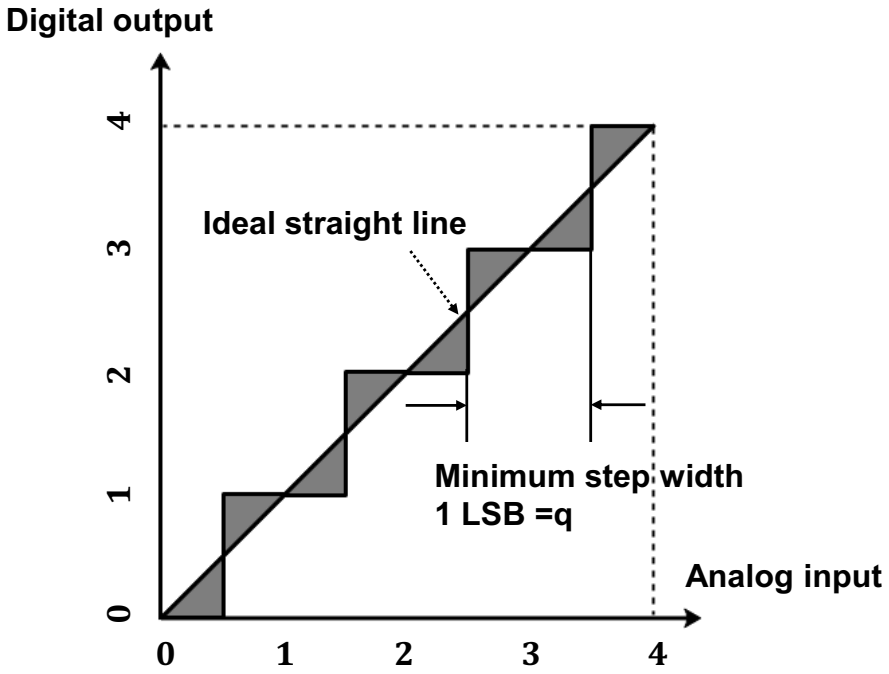


Figure 2.7 Input / output characteristics of AD conversion.

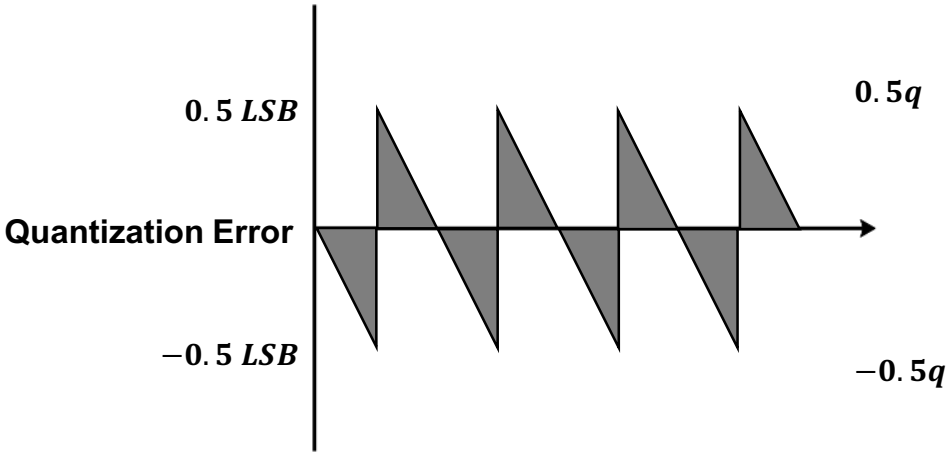


Figure 2.8 Quantization error.

2.3 Conversion Characteristic Specification

2.3.1 INL and DNL

In ADC, the correspondence between input and output digital values is shown.

When the A/D conversion characteristics shown in Fig. 2.9 are used for illustration, the ideal conversion characteristics are shown as wavy lines, but the actual conversion characteristics are shown as solid lines. Therefore, when the transformation value is transferred, the deviation between the actual input signal value and the ideal characteristic is called the Integral Non-linear characteristic, and the maximum value is called the Integral Non-Linearity (INL). However, the so-called best fitting method has a method to set a certain offset in the input/output transformation characteristics so as to minimize the nonlinear error of integration, most use this definition.

In addition, the ideal quantization voltage V of the input signal voltage range V with a certain transformation value is taken. The deviation is called quantized voltage V, and the normalized value is called Differential Non-linearity.

The Integral Non-Linearity is mainly related to distortion, and the Differential Non-linearity (DNL) is related to noise.

In image processing, human vision is pure to distortion and sensitive to change and noise, so more attention is paid to Differential Non-linearity.

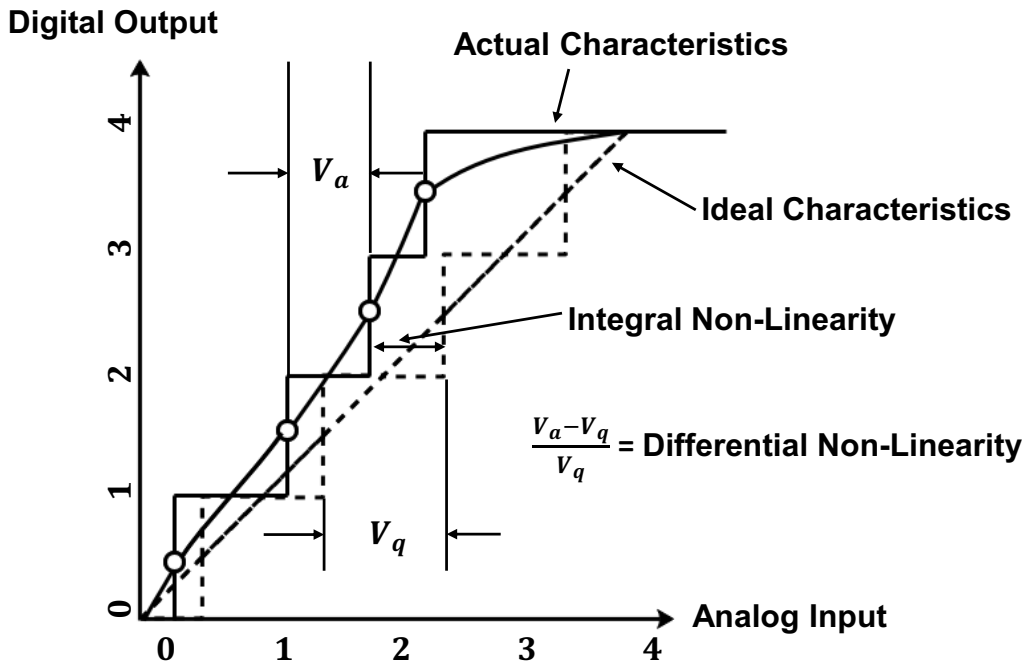
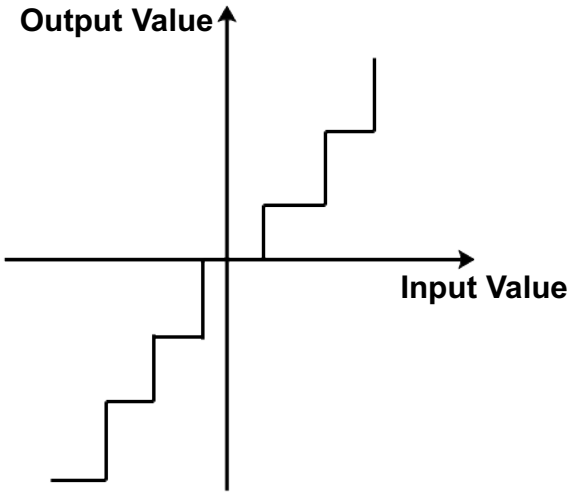


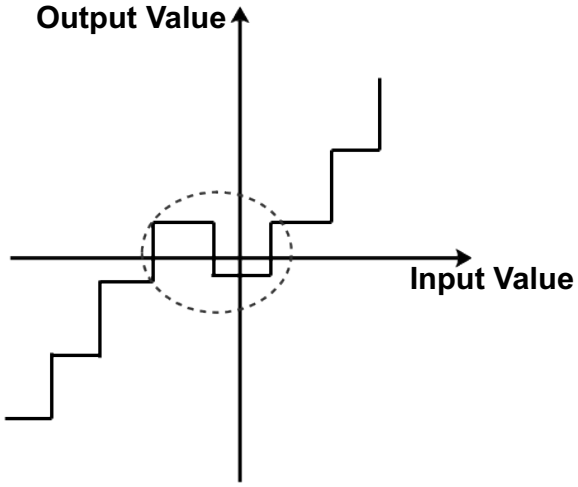
Figure 2.9 Conversion characteristic of ADC

2.3.2 Monotonicity of ADC

The so-called monotonicity degradation is shown in Fig.2.10. In the input and output characteristics of the ADC/DAC, monotonic increase or monotonic decrease collapse, becoming the characteristics of rise, fall, and rise again. In this case, even if the deterioration of straightness is not big, it will become a big problem in certain applications. In particular, systems involving negative feedback will cause problems such as oscillation and local traps. This monotonicity degradation easily occurs in binary ADC/DAC.



(a) Ensuring monotonicity



(b) Degradation of monotonicity

Figure 2.10 Monotonicity of ADC

2.3.3 Dynamic Characteristics of ADC

The dynamic characteristics of an ADC are generally obtained by Fast Fourier Transform (FFT) analysis, which is related to the input frequency, input signal amplitude, and sampling frequency, and they are measured by Signal-to-Noise Ratio (SNR), Signal-to-Noise and Distortion Ratio (SNDR), Effective Number of Bits (ENOB), Spurious-Free Dynamic Range (SFDR), and Total Harmonic Distortion (THD), etc.

(1) SNR: Signal-to-Noise Ratio

$$SNR = Signal\ power\ /\ Noise\ power \tag{2-16}$$

(2) SNDR: Signal-to-Noise and Distortion Ration

The signal distortion ratio refers to the ratio of the output signal power to the sum of all noise and harmonic power in the band, which is simply the ratio of the output signal power to the output non-signal power. It can be expressed as follows:

$$SNDR = \frac{Signal\ power}{Noise\ power + Full - height\ modulation\ electric\ power} \tag{2-17}$$

(3) ENOB: Effective Number of Bits

The number of valid bits refers to the effective number of bits corresponding to the SNDR obtained by the ADC output at full scale input signal, with the following conversion relationship:

$$ENOB = \frac{SNDR[dB] - 1.76}{6.02} \tag{2-18}$$

(4) SFDR: Spurious-Free Dynamic Range

The Spurious-Free Dynamic Range (SFDR) is defined as the ratio of the energy of the fundamental component to the maximum spurious component in the output signal of the ADC, which reflects the maximum interference to the output signal of the ADC in a certain frequency band. For a certain input frequency, the input amplitude and the sampling frequency, the SFDR can be expressed as:

$$SFDR = Signal\ power/Maximum\ high\ modulation\ power \tag{2-19}$$

(5) THD: Total Harmonic Distortion

Total Harmonic Distortion (THD) is defined as the ratio of the harmonic component of the ADC output signal to the energy of the fundamental signal and it can be expressed as:

$$THD = Full\ height\ modulation\ power/Signal\ power \tag{2-20}$$

2.4 Types of ADC

Nowadays, ADCs have been widely used in various types of System-on-Chips (SoCs), and the requirements of ADCs vary from application system to application system. In order to adopt to the application requirements of different SoCs, various structure types of ADCs have emerged during their continuous development, mainly flash ADCs, pipeline ADCs and SAR ADCs. This section focuses on the operating principles of the above types of ADCs and clarifies their application scope as well as their advantages and disadvantages.

2.4.1 Flash ADC

ADC as the core part of analog signal circuit, in many applications, high conversion speed is required, however, flash ADC (fully parallel ADC) has the simplest structure and the fastest conversion rate is often also used.

For an N-bit flash ADC can be represented as Fig. 2.11, which mainly consists of 2^N matching resistors, $(2^N - 1)$ comparators and an encoder. Among them, 2^N matching resistors divide the reference voltage V_{ref} into 2^N equal-step comparison references, and the comparator compares the input signal with these reference voltages, the voltage difference between each adjacent voltage is $V_{ref}/2^N$ (that is, LSB). The other input of the comparator is connected to the analog input signal. This gives a 2^N bit thermometer code by comparing it with each reference voltage, and the final binary code output is completed by a decoder. The flash ADC is a simple structure that requires only one comparison cycle to complete the conversion of the entire ADC, and if the speed of the comparator is guaranteed, the structure can achieve a high conversion rate. However, as the accuracy N increases, the input capacitance increases exponentially, resulting in the smaller input bandwidth. The numbers of comparators and resistors also increase exponentially with N, resulting in this type of ADC requiring a larger chip area, larger power consumption, and even larger input capacitance. Therefore, flash ADCs are often used in low-resolution systems,

such as satellite communications, high-speed instrumentation, radar, and video [5-9].

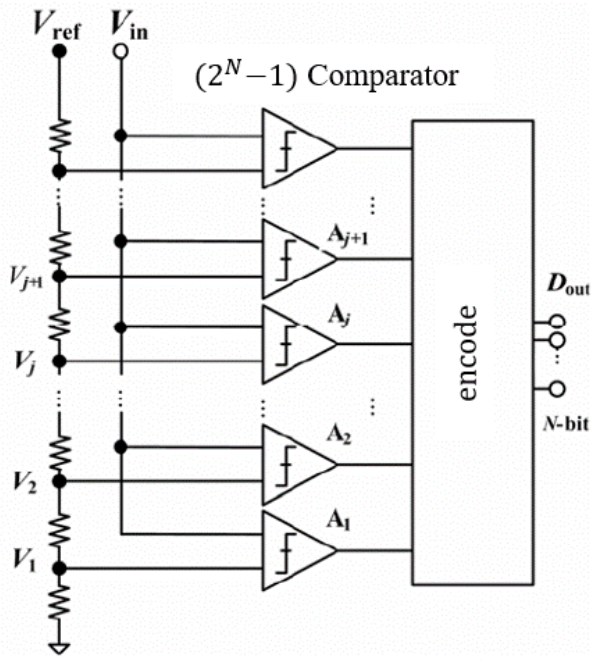


Figure 2.11 Flash ADC structure.

2.4.2 Two-step ADC

The two-step ADC separates the quantization process of higher and lower bits and consists of two ADCs, as shown in Fig. 2.12. It consists of a sample/hold (S/H) circuit, a first-stage ADC, a DAC, a subtractor, and a second-stage ADC. The resolution of the first ADC stage is M-bit, the second stage is L-bit, and the total resolution is (M+L)-bit. The sampled signal is converted to digital by the first stage ADC with high bit (MSBs), and then to analog by the DAC with VB, and the subtractor generates the difference between VA and VB (called the residual). This residual signal is processed by the second ADC stage to obtain a digital output of lower bits (LSBs). However, since S/H, quantization, A/D conversion, D/A conversion, subtraction operations and other operations are performed sequentially, the sampling rate is somewhat limited.

By separating the quantization process of MSBs and LSBs, the two-step structure reduces the number of comparators from $(2^N - 1)$ in the original Flash structure to $(2^M + 2^N - 2)$ and the number of resistors from 2^N to $(2^M + 2^N)$. Compared with the flash ADC, the two-step ADC has a reduced operating speed, but has reduced power consumption and chip area, and is often used in video signal acquisition, mobile communication, high-speed portable systems, and so on [10-12].

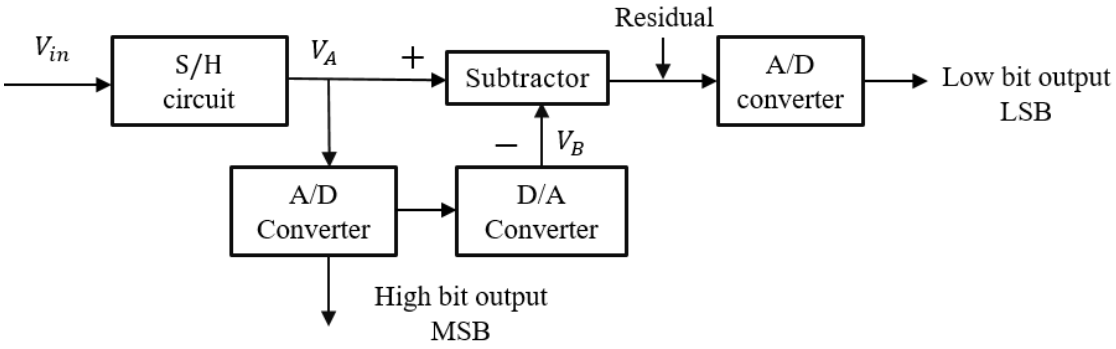


Figure 2.12 Two-step ADC structure block diagram.

2.4.3 Pipeline ADC

The pipeline ADC is based on the two-step ADC principle and consists of several stages cascaded with sub-circuits of similar structure and function. To avoid sampling rate limitation, a sample-hold circuit is added to each stage. Fig. 2.13 shows a block diagram of a K-stage pipeline ADC structure, where each stage 1 to (K-1) contains an S/H, m-bit ADC, m-bit DAC converter, subtractor and amplifier, and the last stage usually uses a flash ADC.

First, the sampled signal from the analog input is converted into an m-bit digital quantity by the first ADC stage, and then this digital quantity is converted into an analog quantity by the DAC, and the residual is obtained using a subtractor, which is amplified and passed to the next stage for processing.

Since each stage can implement S/H, all stages can work simultaneously. The speed of the pipeline ADC is limited by the conversion speed of each

stage and the setup time of the sampling circuit of the next stage. Pipeline ADCs offer conversion rates comparable to flash ADCs with less power and chip area. The main applications are high-speed digital instrumentation, video signal processing, medical imaging, and wireless LAN systems.

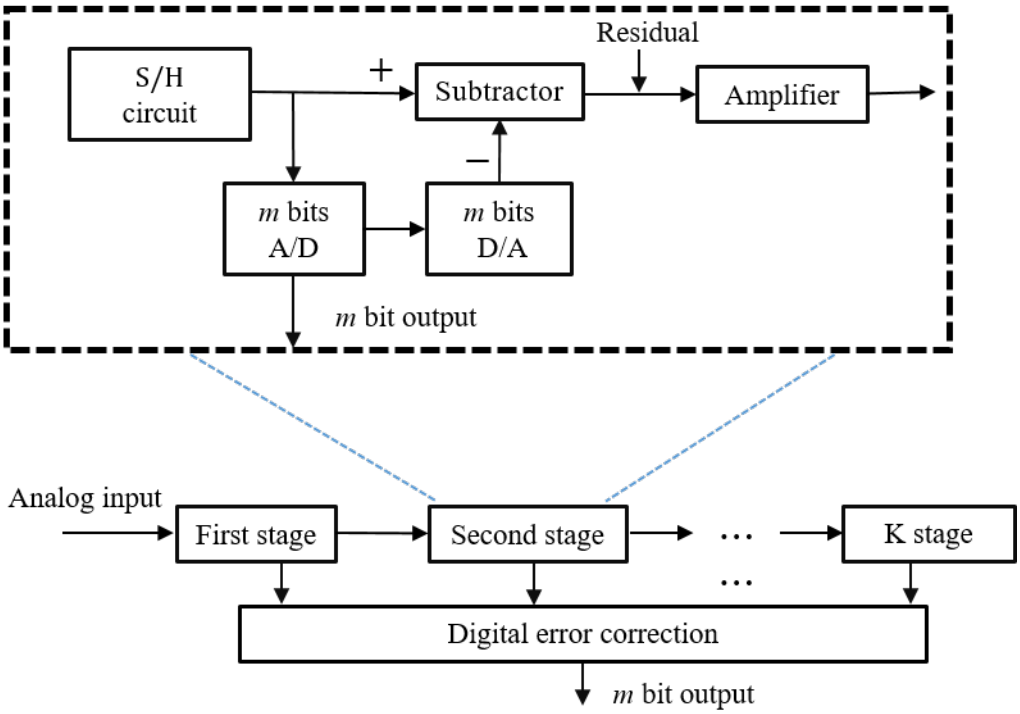


Figure 2.13 Pipeline ADC structure block diagram.

2.4.4 SAR ADC

The Successive Approximation Register (SAR) ADC is a common ADC structure with a sampling rate below 5MS/s with medium to high accuracy, and also it belongs to the Nyquist ADC type. Fig. 2.14 shows the block diagram of the SAR ADC structure [15,16], which mainly includes a S/H circuit, a comparator, a DAC and logic control circuit. The SAR ADC works based on the binary search method by comparing the sampled value $V_{S/H}$ of the input signal with the reference voltage value generated by the D/A

conversion network, the logic output from the high bit to the low bit is successively generated.

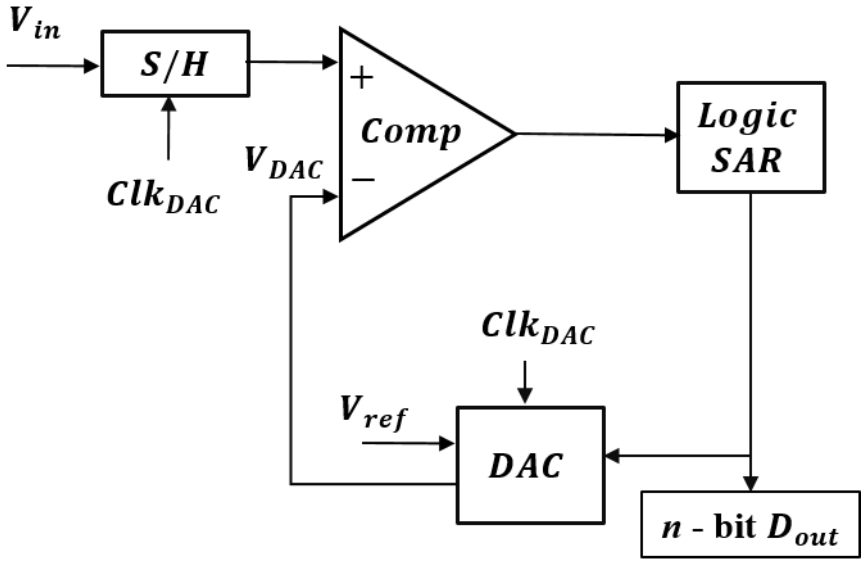


Figure 2.14 SAR ADC structure block diagram.

Fig. 2.15 shows the workflow diagram of SAR ADC. The SAR ADC first samples and holds the analog signal, compares the magnitude of the input signal V_{in} and the output reference voltage V_{dac} of the capacitor array, and then uses the comparison result to control the switch flip connected to the capacitor array of the DAC to increase or decrease the corresponding voltage value, repeats this operation until the DAC completes the N-bit conversion, and the N-bit digital code stored in the successive approximation register is the final output code, which is complete for the A/D conversion.

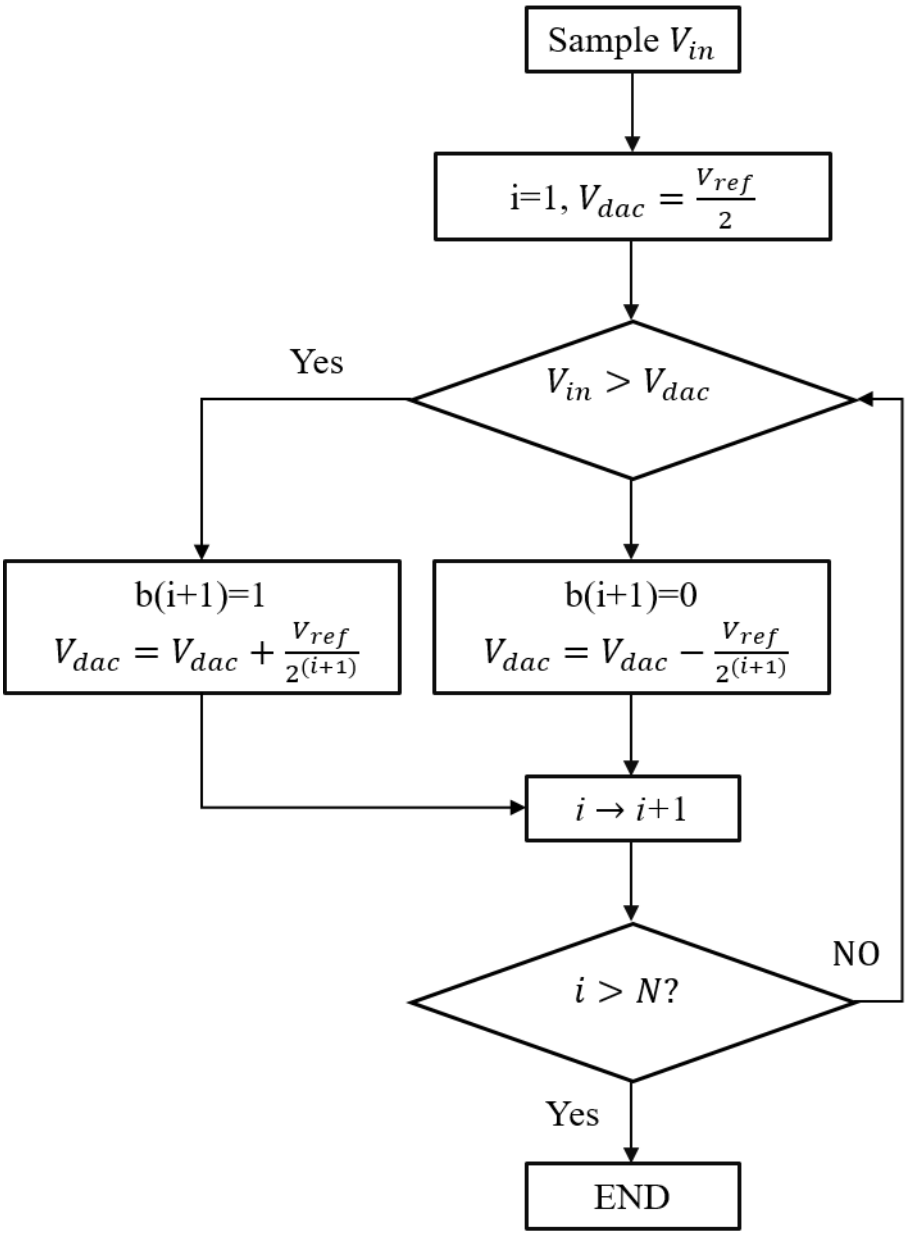


Figure 2.15 SAR ADC working process diagram.

2.4.5 ΔΣ ADC

A sigma-delta ADC (also known as a delta-sigma ADC) oversamples the incoming signal by a large factor using a smaller number of bits than required are converted using a flash ADC and filters the desired signal band. The resulting signal, along with the error generated by the discrete levels of the

flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the quantization error that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output.

Figure 2.16 shows the basic structure of the ΔΣADC.

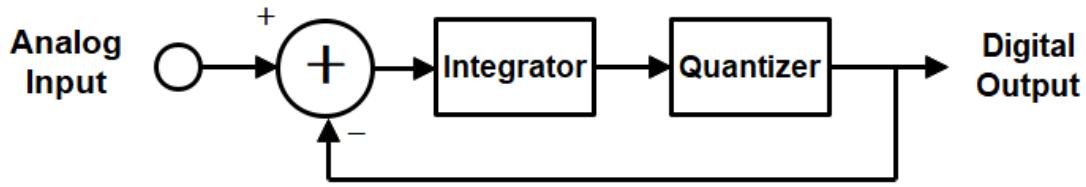


Figure 2.16 ΔΣ ADC (modulator part).

Table 1 Typical Architecture ADC Performance Summary

ADC structure type	Sampling rate	Resolution (accuracy)	Supply voltage	Power	Application
Flash	GS/s	6-8 bit	Low	Large	High-speed system
Two-step	MS/s	8-12 bit	Low	Medium	Wireless communication, medical imaging
Pipeline	MS/s	10-14 bit	High	Medium	High-speed video equipment
SAR	KS/s	8-16 bit	Low	Low	Industrial equipment, loT system
ΔΣ	KS/s	16-24 bit	High	Medium	Audio, precision measurement

Chapter 3

Conventional SAR ADCs

3.1 Synchronous SAR ADC

The conventional synchronous SAR ADC consists of a track/hold circuit, a DAC, a comparator, an SAR logic circuit and a clock generator (Fig. 3.1). Assume that the SAR ADC has 8-bit resolution, and its sampling speed is 10MHz; it requires 8 cycles to obtain 8-bit and also, say, 2 cycles for the input signal sampling with the track/hold circuit. Then the SAR ADC operates with 100MHz clock internally. This restricts the speed and resolution of the SAR ADC.

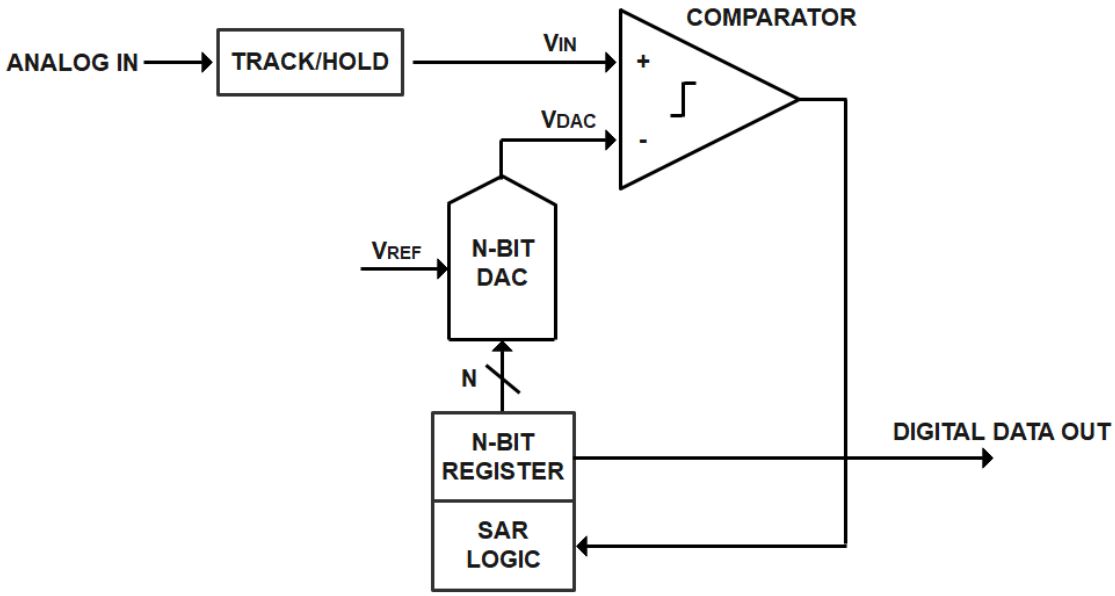


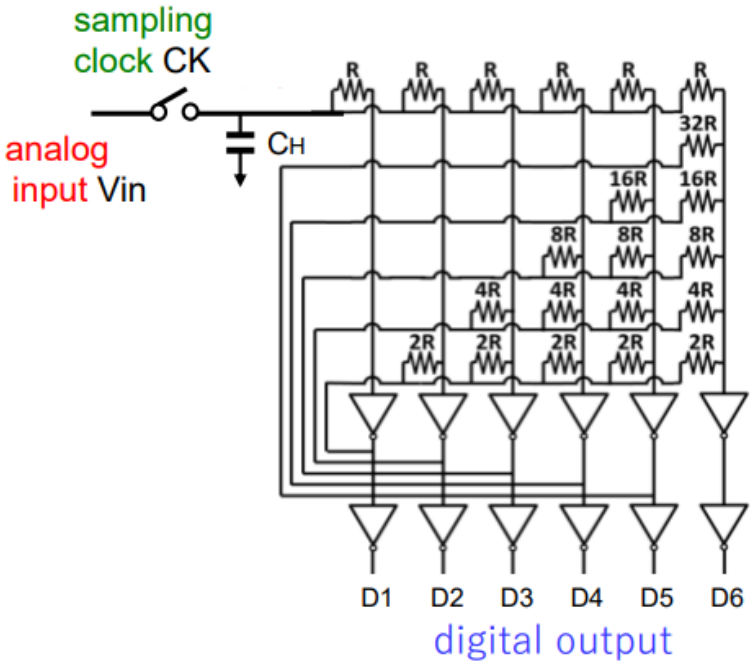
Figure 3.1 An N-bit synchronous SAR ADC.

3.2 Resistor-type Asynchronous SAR ADC Based on Asymmetric Hopfield Network.

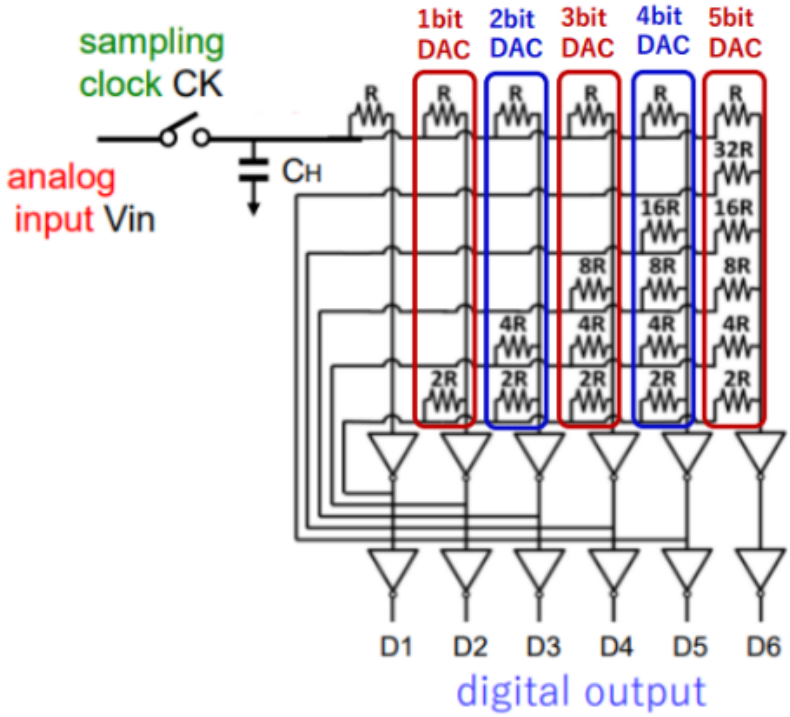
We have investigated an asynchronous SAR ADC based on an asymmetric Hopfield network as shown in Fig. 3.2 (a) [2, 3]. It has N comparators for N-bit resolution, which operate asynchronously and in parallel without a fast internal clock; then its sampling speed becomes much faster. However, the resistor value R needs to be very large (GΩ or TΩ order) to be driven with the inverters.

We also observe in Fig. 3.2 (b) that there are internal DACs corresponding to each bit, and this observation has inspired us to come up with the ADC architecture presented here.

Notice that in this dissertation, we denote D1 as MSB and D6 as LSB for the 6-bit ADC as shown in Fig. 3.2.



(a) Circuit



(b) Internal DACs

Figure 3.2 6-bit asynchronous SAR ADC based on an asymmetric Hopfield network.

3.3 Difference of Synchronous and Asynchronous SAR ADC

Figure 3.3 is an example of synchronous and (conventional) asynchronous SAR ADCs to explain their difference. I compare the working process of synchronous ADC with asynchronous ADC. The performance of asynchronous SAR ADC is no internal high-speed clock, no decoder circuit. So, the advantages are high speed, low power, small chip area.

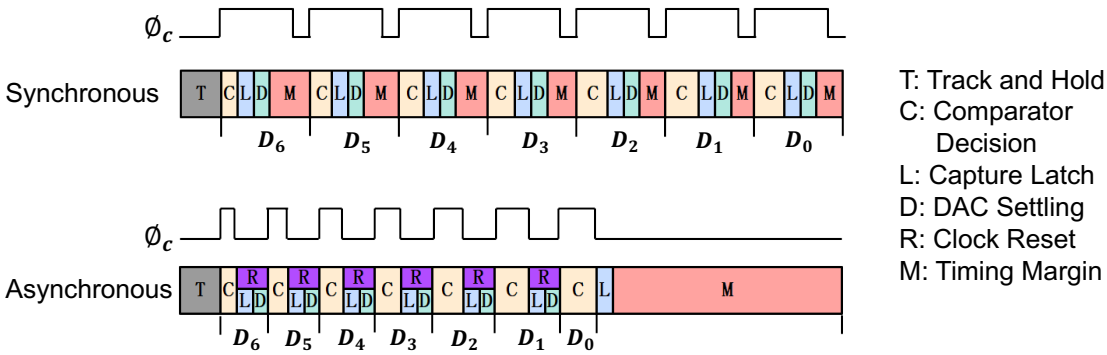


Figure 3.3 4 -Time chart of synchronous and (conventional) asynchronous SAR ADCs

3.4 Conventional and Proposed Asynchronous SAR ADCs

The differences are mainly reflected in the number of comparators and the generation of MSB to LSB. The specific difference is that the conventional asynchronous SAR ADC has only one comparator, and the sequential bit generation from MSB to LSB. The proposed asynchronous SAR ADC has N comparators, lower bits generation with higher bits look-ahead.

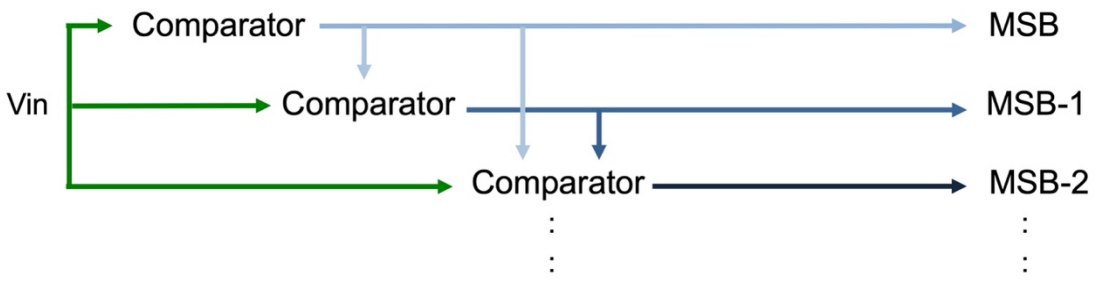


Figure 3.4 Principal block diagram of proposed asynchronous SAR ADC

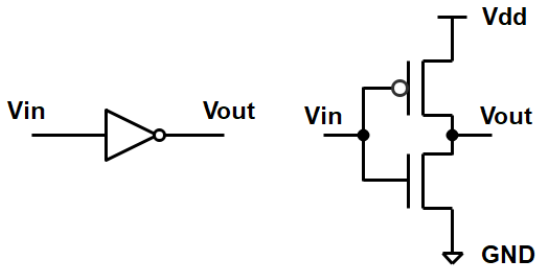
The proposed asynchronous SAR ADC can operate faster than the conventional one, because the proposed SAR ADC can start to generate lower bits before higher bit generation circuits are completely settled with look ahead of higher bits information.

Chapter 4

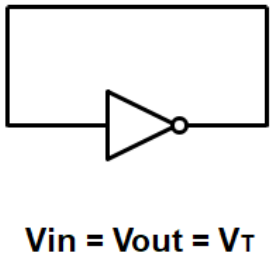
Proposed ADC Circuit and Operation

We here show a 6-bit case of our proposed ADC architecture. Its direct extension to 7-bit, 8-bit or other resolution cases is straightforward.

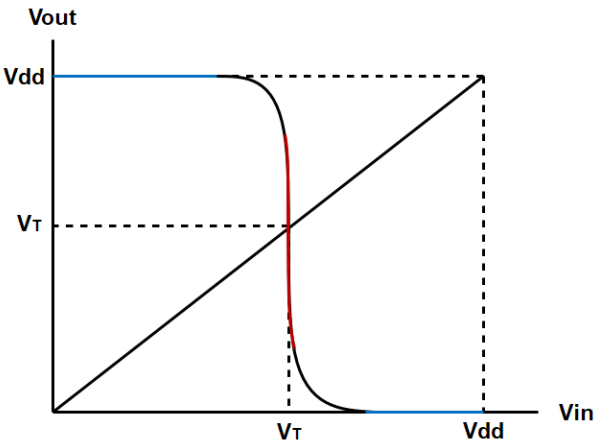
Before discussion on the proposed SAR ADC circuit configuration, the CMOS inverter circuit is shown in Fig. 4.1.



(a) Circuit



(b) CMOS inverter with the input and output connection to bias at the CMOS inverter threshold voltage V_T



(c)Explanation of the circuit operation in Fig. 4.1 (b).

Figure 4.1 CMOS inverter circuit

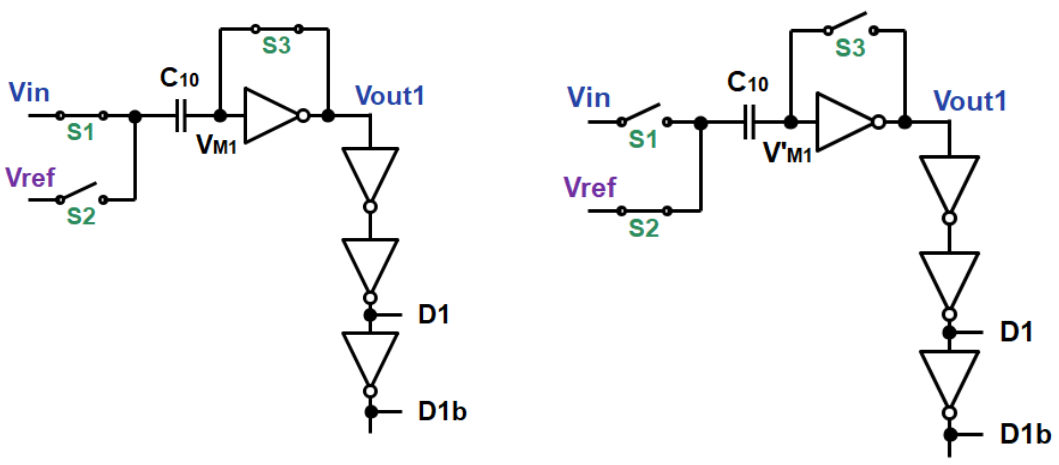
4.1 MSB (D1) Generation Circuit

Fig. 4.2 shows the MSB generation circuit (chopper-type comparator) and its operation. Vin is the analog input signal and V_{ref} is a positive reference voltage, and D1 is the MSB output at logic level.

In phase 1 (Fig. 4.2(a)), the CMOS inverter is biased at its threshold voltage V_T by closing S3; $V_{M1} = V_T$. By opening S2 and closing S1, the capacitor C_{10} is charged with $Q = C_{10}(V_{in} - V_T)$.
In phase 2 (Fig. 4.2(b)), the inverter is biased at high gain region and works as a comparator by opening S1, S3 and closing S2. Since the charge Q in C is conserved, we have the node voltage $V'_{M1} = V_{ref} - V_{in} + V_T$. Then we have the following:

When $V_{in} < V_{ref}$, $V_{out1} = 0$, (D1=0).

When $V_{in} > V_{ref}$, $V_{out1} = V_{dd}$, (D1=1).



(a) Phase 1 (b) Phase 2

Figure 4.2 MSB (D1) generation circuit

4.2 MSB-1 (D2) Generation Circuit

Let us consider the MSB-1 generation circuit (Fig. 4.3). V_{in} is the analog input signal and V_{ref} is a positive reference voltage, $-V_{ref}$ is a negative reference voltage, V_{out1} is the MSB output and D2 is the MSB-1 output. Also, we set $C_{21} = (1/2)C_{20}$.

In phase 1 (Fig. 4.3(a)), the CMOS inverter is biased at its threshold voltage V_T by closing S9; $V_{M2} = V_T$. By opening S5 and closing S4 and S6, the capacitor C_{20} is charged with $Q_1 = C_{20}(V_{in} - V_T)$. Also, by opening S7 and S8, and closing S9, the capacitor C_{21} is charged with $Q_2 = C_{21}(-V_T)$.

In phase 2 (Fig. 4.3(b)), the CMOS inverter is biased at high gain region and works as a comparator by opening S4 and S6 and closing S5. After the phase 2 starts, some inverter delays pass and D1, D1b are determined to 0 or 1.

Suppose $V_{in} < (1/2)V_{ref}$, then D1 becomes 0. Otherwise D1 becomes 1.

In case D1=0 (i.e., $V_{out1} = 0$):
Close S8 and keep S7 open (Fig. 5(b)). Then due to the charge conservation law, we have the following:

$$C_1(V_{in} - V_T) + C_2(-V_T)$$
$$= C_1\left(V_{ref} - V'_{M2}\right) + C_2(-V_{ref} - V'_{M2})$$

Then

$$V'_{M2} = V_{ref} - [C_1/(C_1 - C_2)]\, V_{in} + V_T$$

And we obtain the following:

When $V_{in} < (1/2)V_{ref}$, $V_{out2} = 0$ (D2=0).

When $(1/2)V_{ref} < V_{in}$, $V_{out2} = V_{dd}$ (D2=1).

In case D1=1 (i.e., $V_{out1} = V_{dd}$):
Close S7 and keep S8 open (Fig. 4.3(c)). Then due to the charge conservation law, we have the following:

$$C_1(V_{in} - V_T) + C_2(-V_T) = (C_1 + C_2)(V_{ref} - V'_{M2})$$

Then

$$V'_{M2} = V_{ref} - [C_1/(C_1 + C_2)]V_{in} + V_T$$

And we obtain the following:

When $V_{in} < (3/2)V_{ref}$, $V_{out2} = 0$ (D2=0).

When $(3/2)V_{ref} < V_{in}$, $V_{out2} = V_{dd}$ (D2=1).

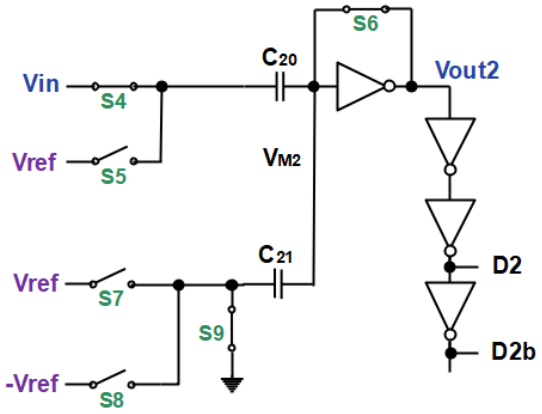
Then we have the following:

When $V_{in} < (1/2)V_{ref}$, D2=0.

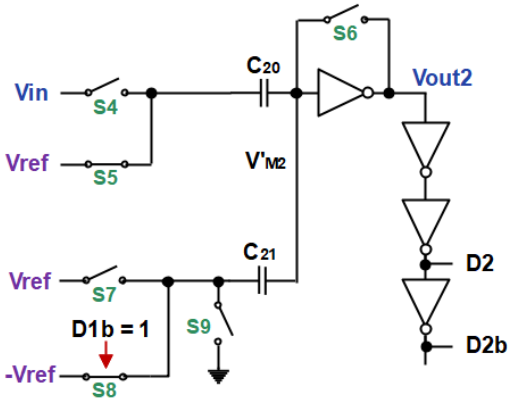
When $(1/2)V_{ref} < V_{in} < V_{ref}$, D2=1.

When $V_{ref} < V_{in} < (3/2)V_{ref}$, D2=0.

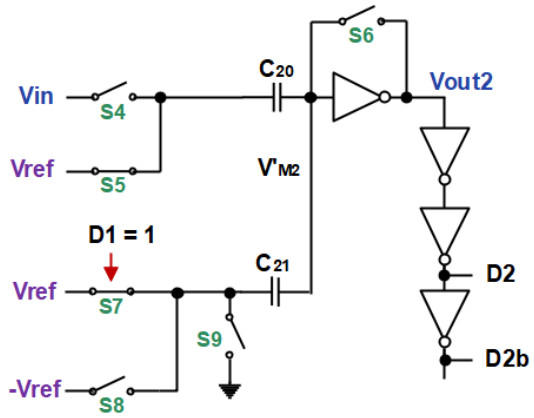
When $(3/2)V_{ref} < V_{in}$, D2=1.



(a) Phase 1



(b) Phase 2 in case D1=0



(c) Phase 2 in case D1=1

Figure 4.3 MSB-1 (D2) generation circuit

4.3 MSB-2 (D3) Generation Circuit

Fig. 4.4 shows MSB-2 generation circuit and its operation. Here $C_{32} = (1/2)C_{31} = (1/4)C_{30}$.

In phase 1 (Fig. 4.4(a)), S11, S13, S14, S16, S17 are open, and S10, S12, S15, S18 are closed.

In phase 2 (Fig. 4.4(b)), S10, S12, S15, S18 are open, and S11 is closed. In case that D1=0, D1b=1, then S13 is kept open and S14 is closed, while in case that D1=1, D1b=0, then S14 is kept open and S13 is closed. In other words, right after D1, D1b, D2 and D2b are determined to 0 or 1, the operation of MSB-2 (D3) generation circuit starts to operate.

We have the following:

When $V_{in} < (1/4)V_{ref}$, D3=0.

When $(1/4)V_{ref} < V_{in} < (1/2)V_{ref}$, D3=1.

When $(1/2)V_{ref} < V_{in} < (3/4)V_{ref}$, D3=0.

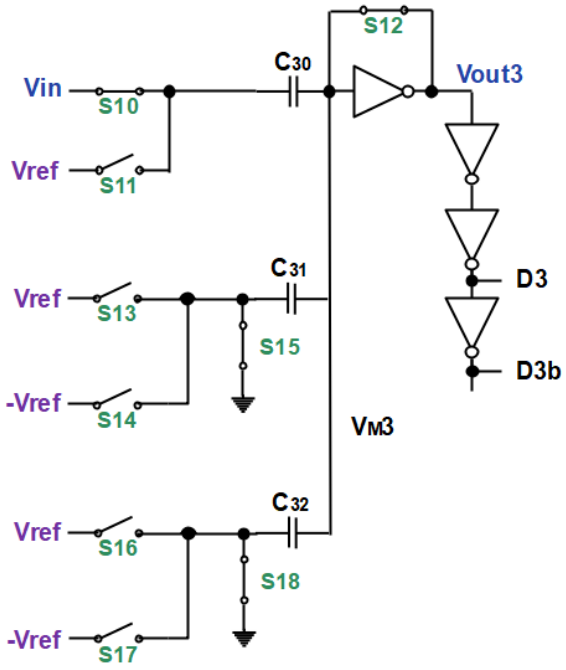
When $(3/4)V_{ref} < V_{in} < V_{ref}$, D3=1.

When $V_{ref} < V_{in} < (5/4)V_{ref}$, D3=0.

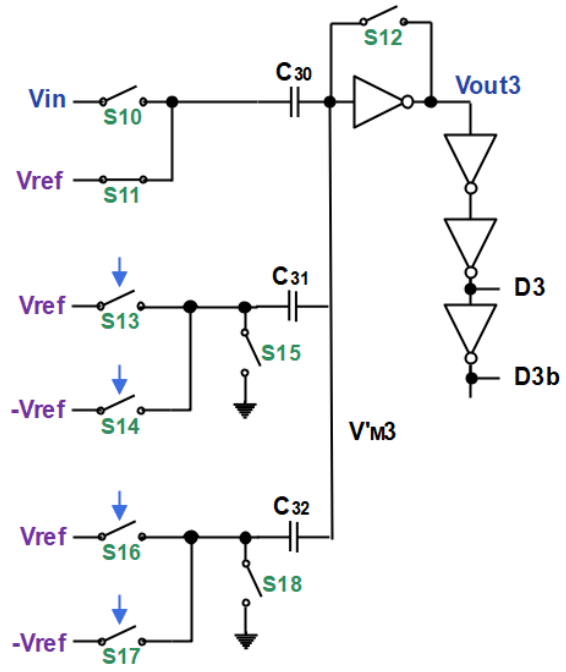
When $(5/4)V_{ref} < V_{in} < (3/2)V_{ref}$, D3=1.

When $(3/2)V_{ref} < V_{in} < (7/4)V_{ref}$, D3=0.

When $(7/4)V_{ref} < V_{in}$, D3=1.



(a) Phase 1



(b) Phase 2

Figure 4.4 MSB-2 (D3) generation circuit

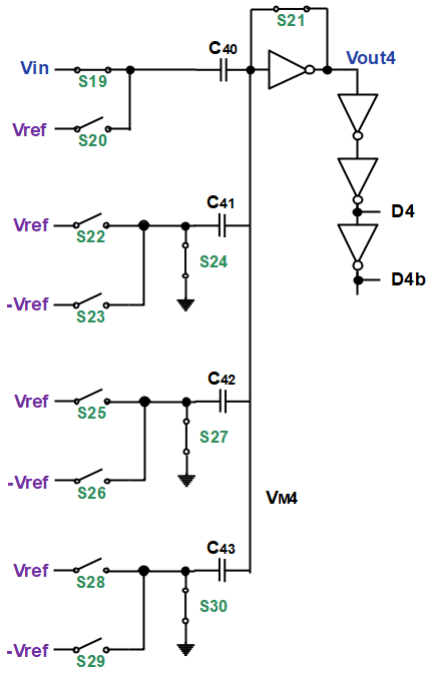
4.4 MSB-3 (D4) Generation Circuit

Fig. 4.5 shows MSB-3 generation circuit and its operation. Here $C_{43} = (1/2)C_{42} = (1/4)C_{41} = (1/8)C_{40}$.

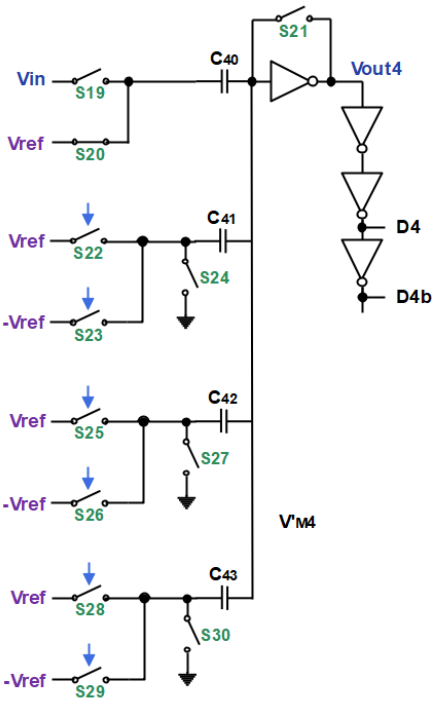
In phase 1 (Fig. 4.5(a)), S20, S22, S23, S25, S26, S28, S29 are open, and S19, S21, S24, S27. S30 are closed.

In phase 2 (Fig. 4.5(b)), S19, S21, S24, S27, S30 are open, and S20 is closed. In case that D1=0, D1b=1, then S22 is kept open and S23 is closed, while in case that D1=1, D1b=0, then S23 is kept open and S22 is closed. In case that D2=0, D2b=1, then S25 is kept open and S26 is closed, while in case that D2=1, D2b=0, then S25 is kept open and S26 is closed. In case that D3=0, D3b=1, then S28 is kept open and S29 is closed, while in case that D3=1, D3b=0, then S28 is kept open and S29 is closed.

Right after D1, D1b, D2, D2b, D3 and D3b are determined to 0 or 1, the operation of MSB-3 (D4) generation circuit starts to operate in comparator delay propagation manner. Hence its operation can be very fast.



(a) Phase 1

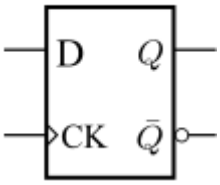


(b) Phase 2

Figure 4.5 MSB-3 (D4) generation circuit

4.5 Simulation Results

A D flip-flop is the most commonly used logic circuit for storing the value of a signal.
Before giving the simulation results, I will explain the principle of D flip flop used in the simulation. Fig. 4.6 shows the truth table of the D-type flip-flop. Fig. 4.7 shows the configuration of internal circuit of D-type flip-flop. Fig. 4.8 shows the principle of D-type flip-flop.



CK	D	Q	$\overline{Q}$
0	X	Q_{PREV}	$\overline{Q_{PREV}}$
↑	0	0	1
↑	1	1	0

Figure 4.6 D-type flip-flop and the truth table.

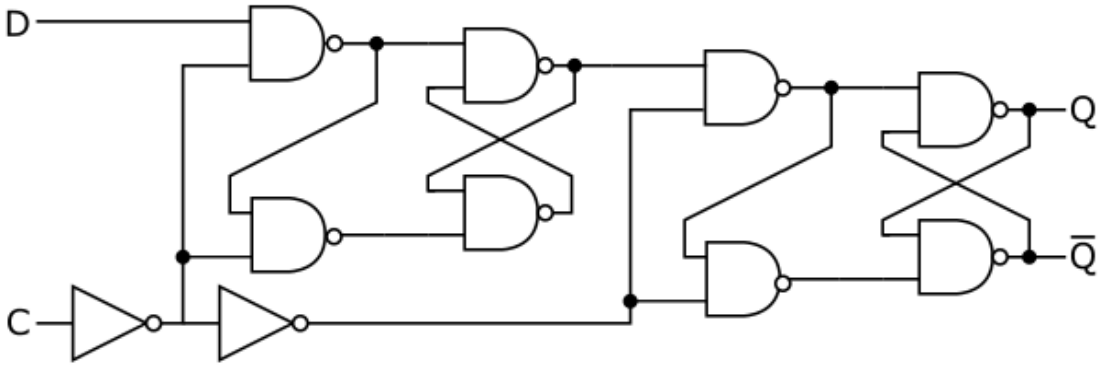


Figure 4.7 Configuration of internal circuit of D-type flip-flop

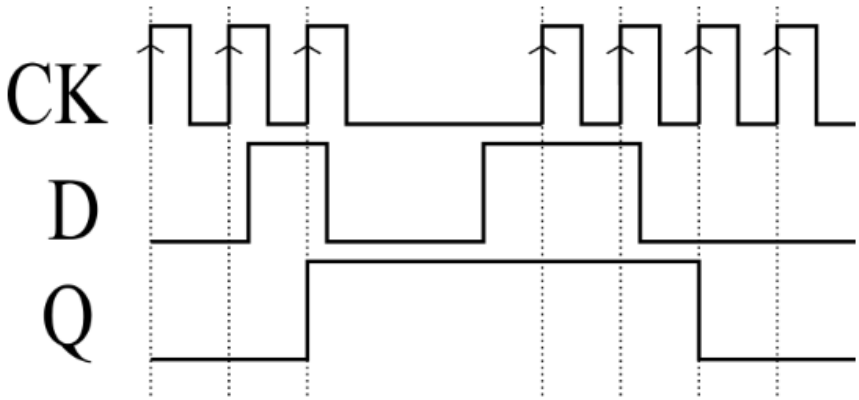


Figure 4.8 principle of D-type flip-flop

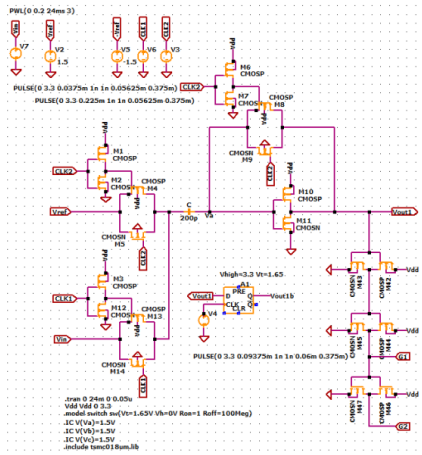
We prove the theoretical results by SPICE simulation. We can find that the theoretical results are consistent with the simulation results. As shown in Figure 4.9-4.11, it is the theoretical and simulation results of 1-3bit.

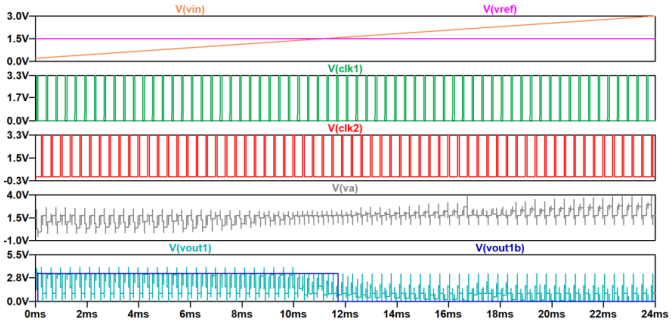
In the simulation of this study, we also use the D-type flip-flop, as shown in Fig. 4.9. We connect the output Vout1 to the D-type flip-flop, and the output of the result Vout1b through the D-type flip-flop.

In this simulation, Driving the input and output switches of capacitors and inverters. Generates pulse for latch by delaying pulses. Delay utilizes inverter delay. Therefore, the delay is adjusted by the size and number of the inverter.

The timing setting and the realization method in the actual circuit design are future problems.

Simulation Results





Theoretical results:

Vin	⇒	$Vout$
0 ~ Vref	⇒	Vdd
Vref ~ 2 Vref	⇒	0

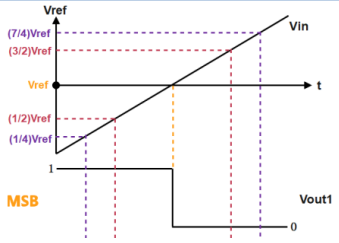
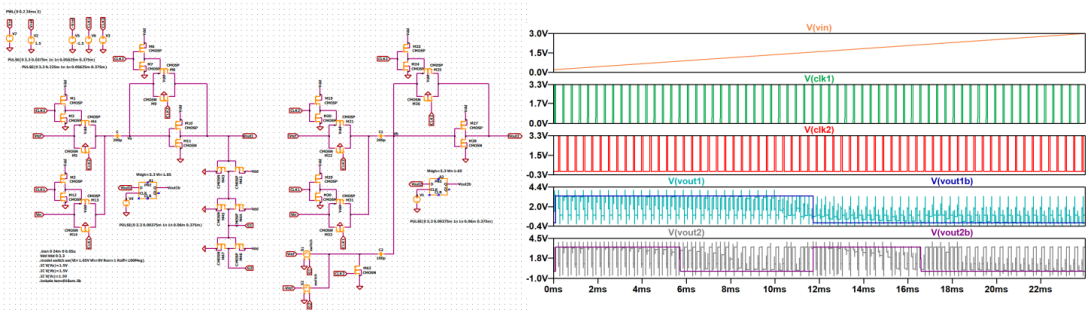


Figure 4.9 Simulation results of the proposed ADC for the ramp input signal (In 1-bit resolution case).

Simulation Results



Theoretical results:

MSB

Vin	⇒	$Vout$
0 ~ Vref	⇒	Vdd
Vref ~ 2 Vref	⇒	0

MSB-1

Vin	⇒	$Vout$
0 ~ (1/2) Vref	⇒	Vdd
(1/2)Vref ~ Vref	⇒	0
Vref ~ (3/2)Vref	⇒	Vdd
(3/2)Vref ~2Vref	⇒	0

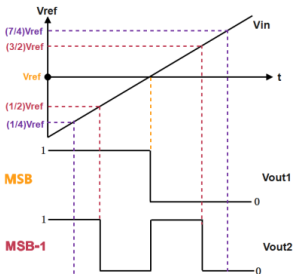
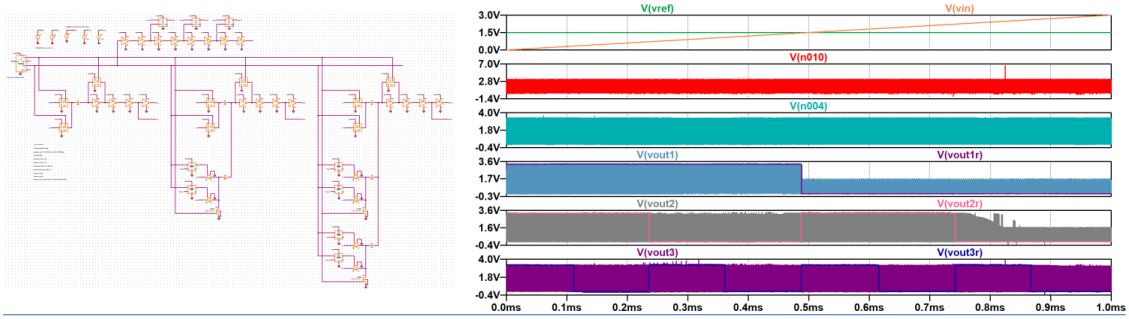


Figure 4.10 Simulation results of the proposed ADC for the ramp input signal (In 2-bit resolution case).

Simulation Results



Theoretical results:

MSB

Vin	⇒	$Vout$
0 ~ Vref	⇒	Vdd
Vref ~ 2 Vref	⇒	0

MSB-1

Vin	⇒	$Vout$
0 ~ (1/2) Vref	⇒	Vdd
(1/2)Vref ~ Vref	⇒	0
Vref ~ (3/2)Vref	⇒	Vdd
(3/2)Vref ~2Vref	⇒	0

MSB-2

Vin	⇒	$Vout$
0 ~ (1/4)Vref	⇒	Vdd
(1/4)Vref ~ (1/2)Vref	⇒	0
(1/2)Vref ~ (3/4)Vref	⇒	Vdd
(3/4)Vref ~ Vref	⇒	0
Vref ~ (5/4)Vref	⇒	Vdd
(5/4)Vref ~ (3/2)Vref	⇒	0
(3/2)Vref ~ (7/4)Vref	⇒	Vdd
(7/4)Vref ~ 2Vref	⇒	0

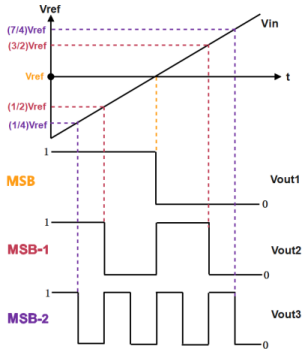


Figure 4.11 Simulation results of the proposed ADC for the ramp input signal (In 3-bit resolution case).

We have designed also MSB-4 (D5) and MSB-5 (D6) generation circuits, and then whole 6-bit ADC with TSMC 0.18μm CMOS process parameters. Fig. 4.12 shows its LT-spice simulation results for the ramp input and we see that the proposed ADC works properly.

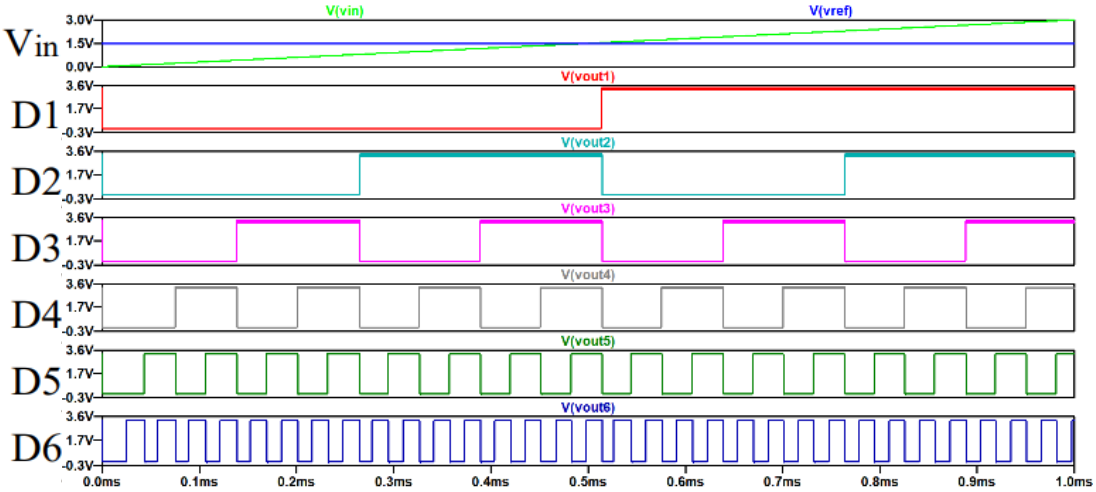


Figure 4.12 Simulation results of the proposed ADC for the ramp input signal (In 6-bit resolution case).

Chapter 5

Discussions and Conclusions

5.1 Discussions

The proposed ADC uses switches, capacitors and CMOS chopper-type comparators without operational amplifiers. Hence it can operate with low supply voltage (as below as CMOS switches can work) and low power and is suitable for fine CMOS implementation.

The proposed ADC employs open-loop configuration and hence it can be fast, but its linearity may not be good if care is not taken. It can be used inside a multi-bit ΔΣ AD modulator (Fig. 5.1) [26, 27] where the ADC nonlinearity is noise shaped. Also, it is suitable as a sub-ADC inside a pipelined ADC (Fig. 5.2) [1], where the sub-ADC errors can be compensated by the redundancy of the pipelined ADC circuits. In these applications, kT/C noise and capacitor mismatch effects inside the proposed ADC are compensated and hence its capacitor sizes can be minimized.

The circuits use a minus reference voltage of $-V_{ref}$, but with some circuit design, the usage of $-V_{ref}$ can be avoided (Fig. 5.3).

The proposed ADC is similar to an asynchronous SAR ADC [6-12], a pipelined ADC [1], a sub-ranging ADC [1], or a binary-search ADC [28-31] in some respects but has several different points (Table 2).

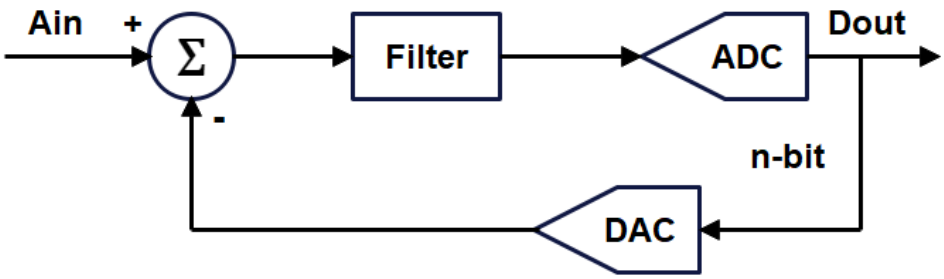


Figure 5.1 Multi-bit ΔΣ AD modulator

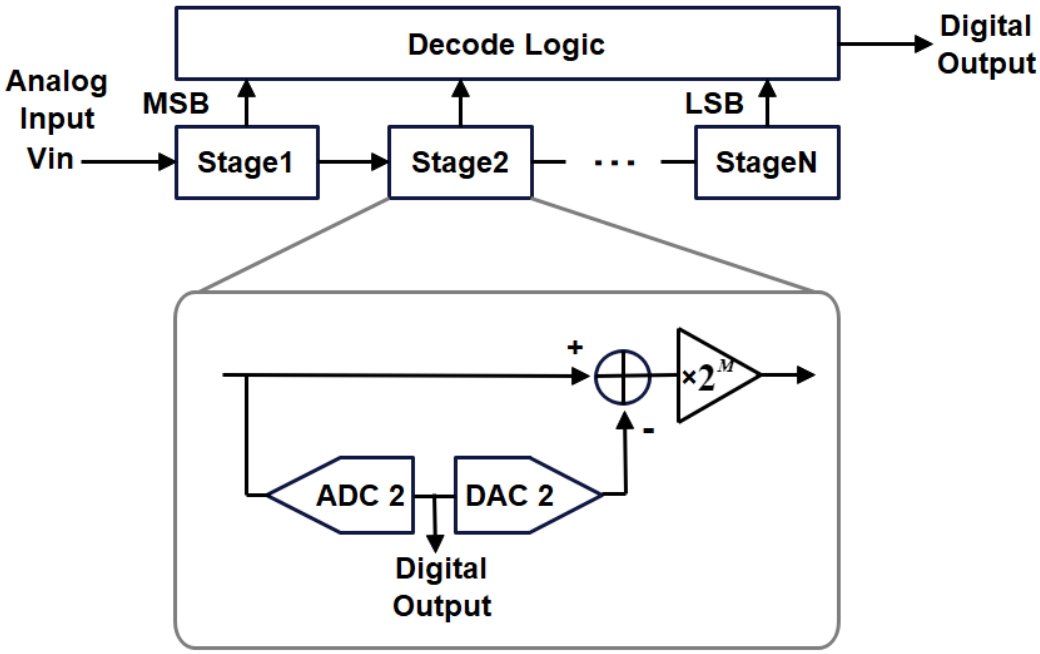
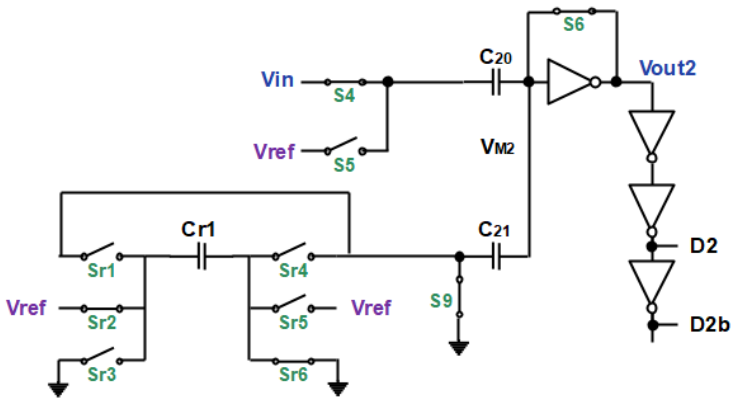
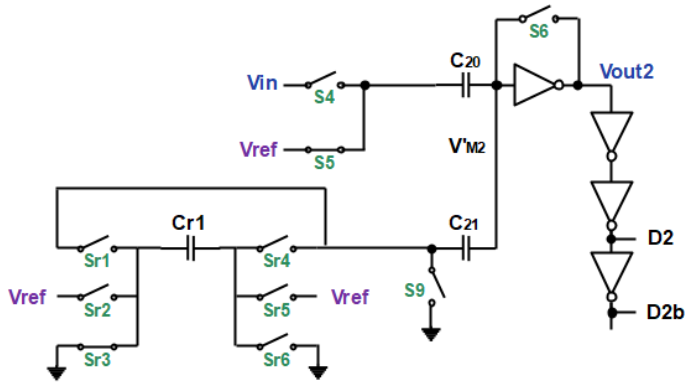


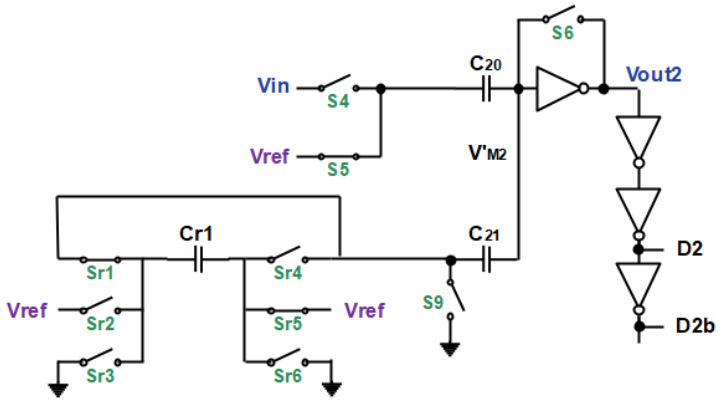
Figure 5.2 Pipelined ADC configuration.



(a) Phase 1



(b) Phase 2 in case of D1=1



(c) Phase 2 in case of D1=0

Figure 5.3 Equivalent circuit replacing minus reference voltage in MSB-1 (D2) generation circuit

Table 2 N-bit ADC Comparison

	# of comparators	High Freq. Internal Clock	Power	Operation	Speed	Chip area
Synchronous SAR ADC	1	Needed	Medium	Sequential	Slow	Small
Conventional Asynchronous SAR ADC	1	NOT needed	Very small	Sequential	Fast	Small
Proposed Asynchronous SAR ADC (Resistor-type)	N	NOT needed	Small	Sequential with look ahead	Very fast	Large (huge resistors)
Proposed Asynchronous SAR ADC (Capacitor-type)	N	NOT needed	Small	Sequential with look ahead	Very fast	Small

5.2 Conclusions

This paper has proposed a new ADC architecture with the following features:

1. It uses switches, capacitors and N CMOS chopper-type comparators without operational amplifiers for N-bit resolution. Hence it can operate with low supply voltage (as below as CMOS switches can work) and low power.
2. In each bit generation circuit, each corresponding DAC is embedded.
3. All N comparators as well as the above DACs operate in parallel and the total AD conversion time is the sum of comparator propagation delays and capacitor charge/discharge settling time.

4. Its possible applications are for a sub-ADC inside a multi-bit ΔΣ AD modulator and a pipelined ADC.

The basic circuits of the proposed ADC are shown and its operation is confirmed with LTspice simulation with TSMC 0.18um CMOS process parameters.

We close this part by remarking that the proposed ADC can be extended to a non-binary weighted structure [13-18]; since it can have some redundancy, the decision mistakes of the upper bits can be digitally corrected if the lower bits are obtained correctly, the upper bit generation circuits can be designed with minimum size and power. This would be the next project.

Finally, we discussed the application of this ADC.

The proposed SAR ADC can be used in Sub-ADC inside multi-bit ΔΣ AD modulator, and pipeline ADC. (Fig. 5.4) It can be required to achieve high-speed, small circuit, low power. But no need for accuracy by noise-shaping and digital error correction.

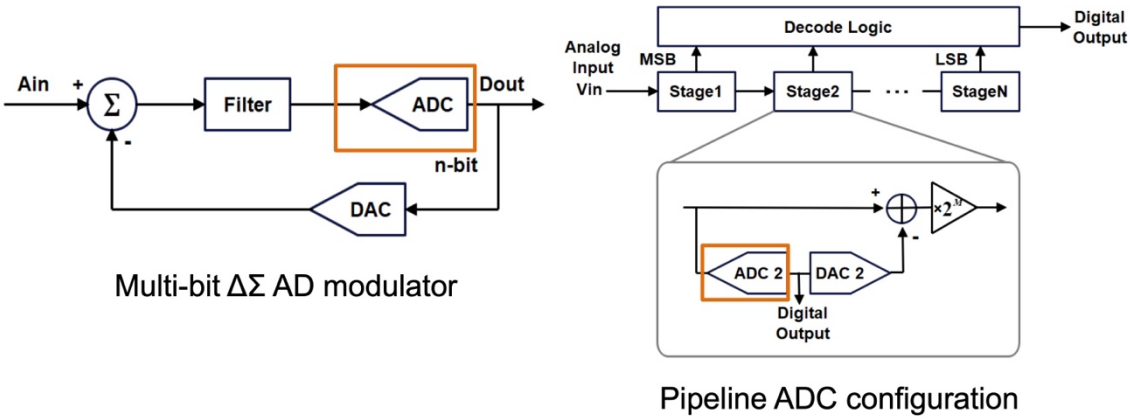


Figure 5.4 Application of the proposed SAR ADC

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Part 2

Derivation of Digital-to-Analog Converter Architectures Based on Number Theory

Chapter 1

Introduction

Analog/mixed-signal circuit design is art rather than technology, with which industry can differentiate their electronic products. There is analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are especially important [1-4]. Their design often relies on intuitions and experiences of mature designers, rather than mathematical theory; only one exception is analog filter synthesis and analysis [5]. On the contrary, the authors have been involved in the research for applications of classical mathematics - such as number theory [6] - to their design; in this viewpoint, our research results have been reviewed and summarized in [7-13]. This paper introduces new DAC architecture derivation from number theory to validate our argument that classical mathematics can explore new analog and mixed-signal circuit design. The derived DAC architectures may not well incorporate circuit non-ideality effects such as device mismatches. However, this attempt may lead to new DAC architecture derivation methodology, and this paper shows its first step.

Our previous research results for applications of classical mathematics to analog/mixed-signal circuit designs are summarized as follows.

Fibonacci sequence weight SAR ADC:

We have investigated SAR ADC design using a redundant SAR search algorithm with Fibonacci sequence weight. We showed that this method can realize high speed SAR AD conversion when the internal DAC incomplete settling is considered [14].

Metallic Ratio Sampling:

We have investigated efficient waveform acquisition conditions between the measured waveform repetitive frequency (f_{sig}) and the sampling clock frequency (f_{CLK}) in an equivalent-time sampling system, when the measured waveform is periodic. We have obtained that in case that $f_{\mathrm{CLK}}/f_{\mathrm{sig}}$ is a metallic ratio, waveform missing phenomena for the equivalent-time sampling can be avoided and highly efficient waveform acquisition sampling

can be realized [15-17]. This technique can be used for analog/mixed-signal IC testing where the input signal is controllable.

Residue Sampling:

We have investigated the residue sampling circuit which provides high-frequency signal estimation using multiple low-frequency sampling circuits following an analog Hilbert filter and ADCs; the sampling frequencies are relatively prime. It is based on aliasing phenomena in the frequency domain for waveform sampling and the residue number theory [18, 19].

Efficient ADC Histogram Testing Condition:

We have studied the ADC testing efficiency improvement of the histogram method by investigating the ratio between the input frequency and the sampling frequency to shorten ADC test time, and we have found that the metallic ratio is effective [20].

Non-uniform Current Division Resistive DAC:

We have studied design and analysis of DACs based on the non-uniform current division resistive ladder, and proposed a new configuration DAC with segmentation of binary, quaternary and unary resistive-ladders, which enables two times gain with equivalent chip area and current sources to the conventional one [21-23].

Gray Code Input DAC:

We have also investigated three types of Gray-code input DAC architectures (current-steering, charge-mode and voltage-mode DACs) for glitch reduction and hence clean signal can be generated [24, 25].

2D Layout of Unit Cells with Pseudo Random Selection Order for Unary DAC:

We have investigated pseudo random selection order algorithms for the segmented DAC linearity improvement, by cancelling systematic mismatch effects among unit cells [26-29]. We consider their 2D array layout with systematic errors. If they are laid out and selected in a regular manner, the systematic errors are accumulated at the DAC output, which causes large non-linearity. If they are selected pseudo-randomly, they can be cancelled to some extent. The investigated pseudo-random selection algorithms are based on Magic Square, Latin Square as well as Euler's Knight Tour.

Polygonal Number DAC and Prime Number DAC:

We have proposed the preliminary ideas of the following DAC configurations based on number theory [30-32]: (i) The DAC consists of N

current sources, N switch arrays, an N-polygonal number weighted resistor network, and a decoder (N= 3, 4, 5, ...); this is based on the polygonal number theory. (ii) The DAC consists of 2 current sources, 2 switch arrays, a prime number weighted resistor network, and a decoder (N= 3, 4, 5, ...); this is based on the Goldbach conjecture. This paper discusses the derivation of these DACs from the number theory in details. This paper shows that the derivation of very new DAC configurations from the number theory is possible and demonstrates their operations in principle as the first step. Also, the possibility of dynamic element matching (DEM) technique usage [3, 12] to take care of the device mismatch effects is described.

The outline of this paper is as follows: Section 2 shows the derivation of the polygonal number DAC from the polygonal number theorem and its configuration as well as operation verification with simulation. Section 3 shows the derivation of the prime number DAC from Goldbach conjecture and its configuration as well as operation with simulation. Section 4 provides conclusion.

Chapter 2

D/A Converter and Basic Configuration

2.1 D/A Converters

D/A converter is a circuit that converts digital signals into analog signals. In addition to being used alone, it can also be used as the internal circuit of the ADC.

There are several DAC architectures; the suitability of a DAC for a particular application is determined by figures of merit including: resolution, maximum sampling frequency and others. Digital-to-analog conversion can degrade a signal, so a DAC should be specified that has insignificant errors in terms of the application.

DACs are commonly used in music players to convert digital data streams into analog audio signals. They are also used in televisions and mobile phones to convert digital video data into analog video signals. These two applications use DACs at opposite ends of the frequency/resolution trade-off. The audio DAC is a low-frequency, high-resolution type while the video DAC is a high-frequency low- to medium-resolution type.

Due to the complexity and the need for precisely matched components, all but the most specialized DACs are implemented as integrated circuits (ICs). These typically take the form of metal–oxide–semiconductor (MOS) mixed-signal integrated circuit chips that integrate both analog and digital circuits.

Discrete DACs (circuits constructed from multiple discrete electronic components instead of a packaged IC) would typically be extremely high-speed low-resolution power-hungry types, as used in military radar systems. Very high-speed test equipment, especially sampling oscilloscopes, may also use discrete DACs.

DACs and ADCs are part of an enabling technology that has contributed greatly to the digital revolution. To illustrate, consider a typical long-distance telephone call. The caller's voice is converted into an analog electrical signal by a microphone, then the analog signal is converted to a digital stream by an ADC. The digital stream is then divided into network packets where it may be sent along with other digital data, not necessarily audio. The packets

are then received at the destination, but each packet may take a completely different route and may not even arrive at the destination in the correct time order. The digital voice data is then extracted from the packets and assembled into a digital data stream. A DAC converts this back into an analog electrical signal, which drives an audio amplifier, which in turn drives a loudspeaker, which finally produces sound.

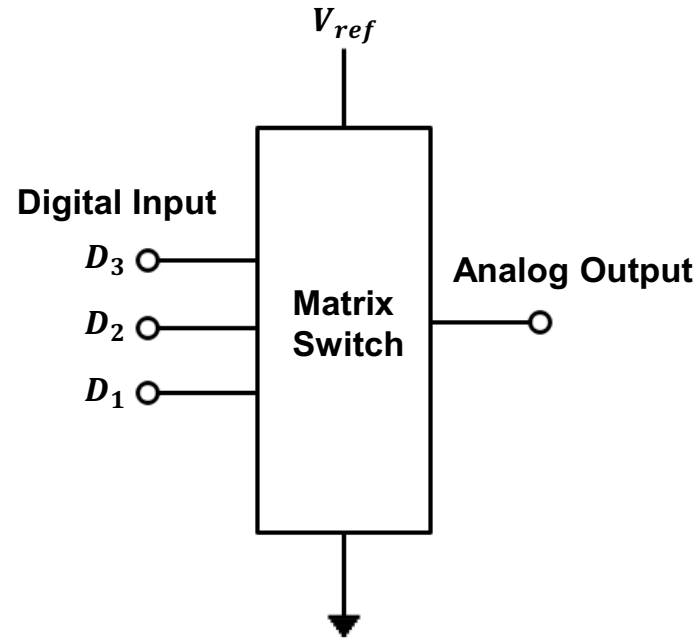
In the DAC, when the bits of the N-bit digital input card are set from the highest MSB (Most Significant Bit) to D1, D2, DN, the output voltage V_O can be expressed by the following formula.

$$V_O = V_{FS}\left(\frac{D_1}{2} + \frac{D_2}{2^2} + \cdots + \frac{D_N}{2^N}\right) + V_{OS} \quad D_i \in \{1, 0\} \qquad (2\text{-}1)$$

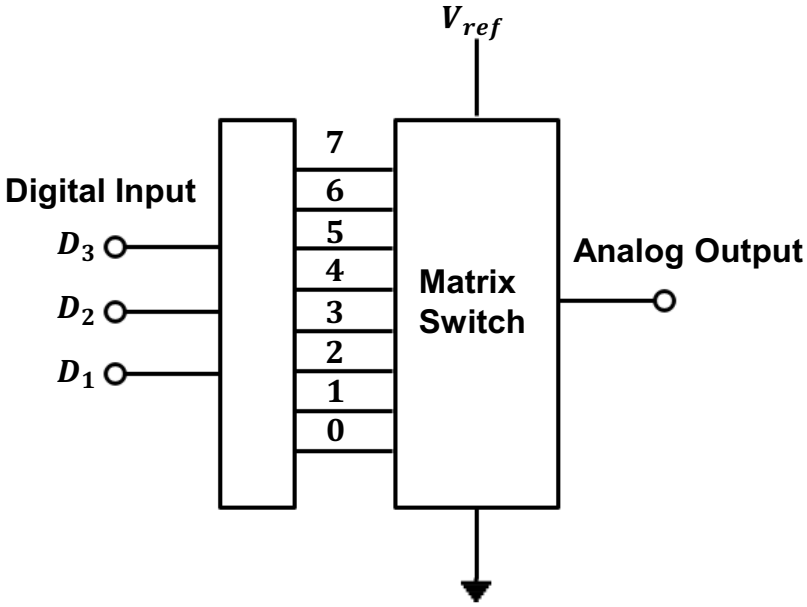
Here, V_{OS} is the offset voltage. When the output is current, the output current can be expressed as the following equation.

$$I_O = I_{FS}\left(\frac{D_1}{2} + \frac{D_2}{2^2} + \cdots + \frac{D_N}{2^N}\right) + I_{OS} \quad D_i \in \{1, 0\} \qquad (2\text{-}2)$$

As a method to realize this DAC, there are roughly two methods. As shown in Fig. 2.1, one is the binary type that adds the elements of the binary number, and the other is the decoding type that temporarily decodes the input binary data into numerical values and adds the unit elements according to their numbers.



(a) Binary method



(b) Decoding method

Figure 2.1 Basic structure of DAC

2.2 Basic Configuration of D/A Converters

2.2.1 Binary DAC

The binary DAC can be directly expressed as Eq. (2-1) or Eq. (2-2),

A weighted current source or charge of magnitude is prepared as shown following:

$$\frac{1}{2^i} \quad (i \in \{0, 1, 2, \dots, N\})$$

The weighted current source or charge is added by each bit of the input digital signal. Since the voltage source is difficult to add, it is not used for a binary type DAC. The simplest binary DAC is shown in Fig. 2.2, using a weighted resistor and an operational amplifier. When the reference voltage V_{ref} is applied to the resistance $2^i R_S$, the flowing current I_i can be expressed as the following formula,

$$I_i = \frac{V_{ref}}{2^i R_S} \tag{2-3}$$

Therefore, the voltage V_O appearing in the output can be expressed as,

$$V_O = V_{ref} \frac{R_F}{R_S} \sum_{1}^{N} \frac{D_i}{2^i} \quad (i \in \{1, 2, \dots, N\}) \tag{2-4}$$

However, the ratio of resistance in this method is too large to be practical. For example, when it is decomposed into 10 bits, it becomes 2^9, i.e., 512 times.

Generally, the practical method of using resistance to realize binary DAC is to use R-2R ladder resistor network as shown in Fig. 2.3.

In the R-2R ladder resistance network as shown in the figure, the resistance from point a to the right is the parallel resistance of 2R and 2R, so it is R. Therefore, the current flowing in from the left side of point a is evenly divided, and half of the current flows respectively. The resistance from point b to the right is the series resistance of R and R, so it is 2R. Since the

resistance inserted into point B and the grounding terminal is 2R, the current flowing from the left side of point *b* is equally divided into half on the grounding side and half in the direction of point *a*. Because there is such a property, the current I_i flowing through the nth resistance is,

$$I_i = \frac{V_{ref}}{R} \cdot \frac{1}{2^i} \quad (i \in \{1, 2, \dots, N\}) \tag{2-5}$$

With the structure shown in Fig. 2.4, a binary DAC can be realized. As the resistance ratio is only 2 times, it can be easily realized through parallel connection or series connection of the same resistance. The above DACs use the additivity of current but can also use the additivity of charge.

Fig. 2.5 shows a binary DAC using capacitance. First, set all the switches to the grounding side, so that the charge of the capacitor is zero. There, the charge at point A is zero.

Then, according to the input data, when the data value is 1, the reference voltage $-V_{ref}$ is applied to each capacitor. When the data value is 0, the capacitors are grounded,

$$CV_{ref} \sum_{i=1}^{N} \frac{D_i}{2^i} - CV_{out} = 0 \tag{2-6}$$

Therefore, the output voltage V_{out} is,

$$V_{out} = V_{ref} \sum_{i=1}^{N} \frac{D_i}{2^i} \tag{2-7}$$

D/A conversion can be realized.

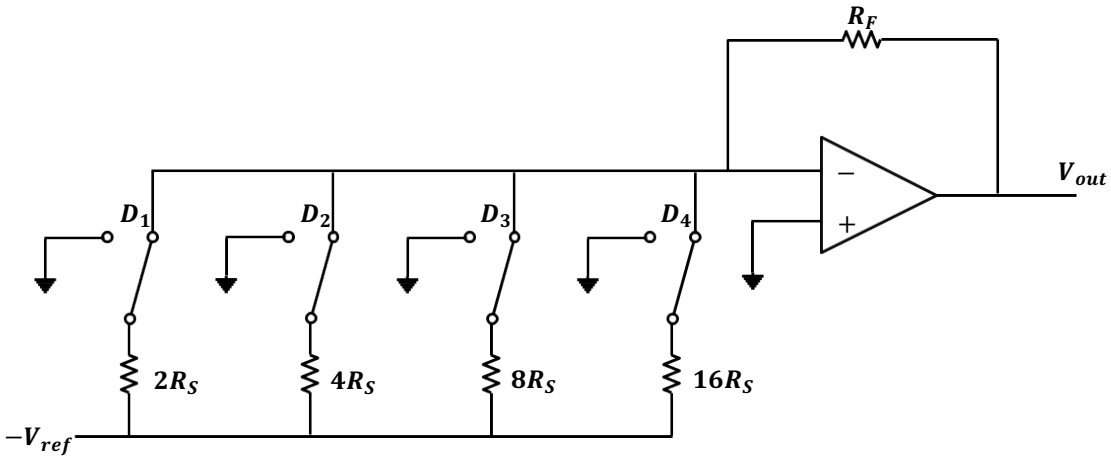


Figure 2.2 DAC using weighted resistance

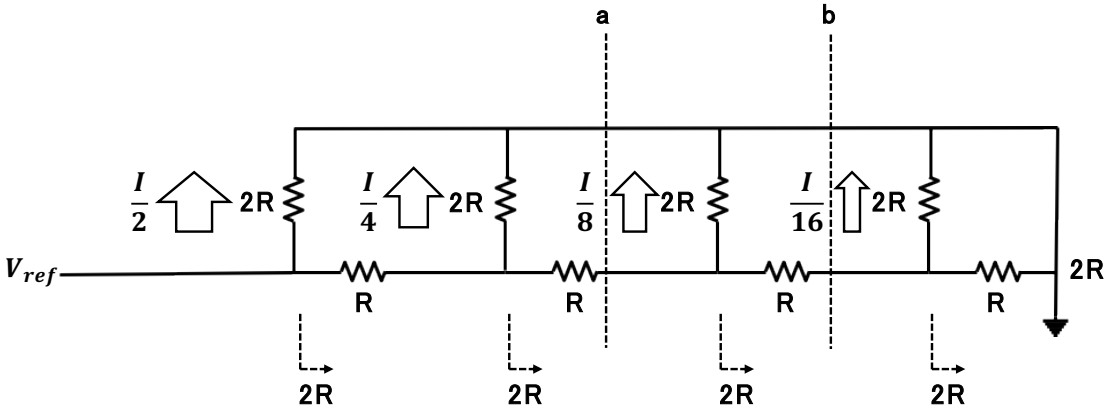


Figure 2.3 R-2R ladder resistance network.

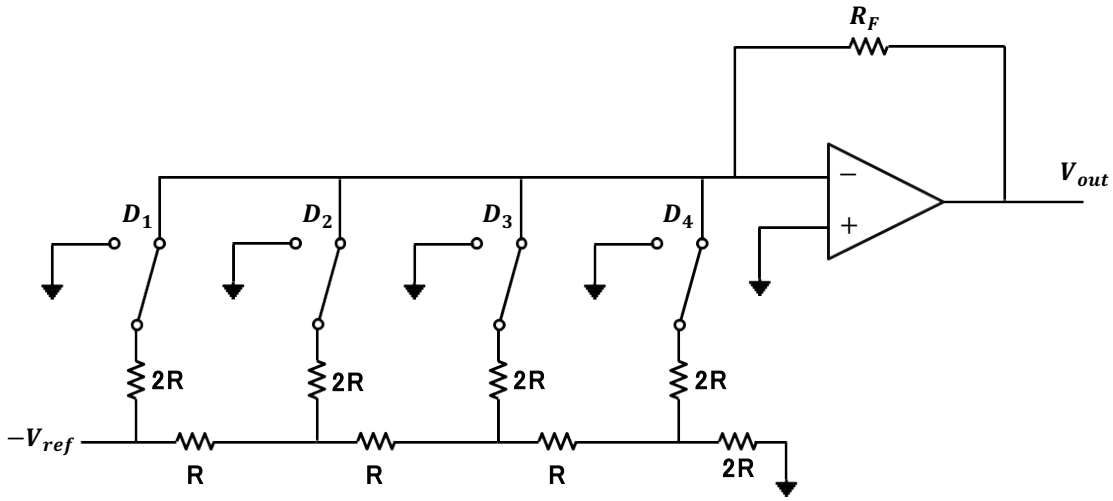


Figure 2.4 Binary type DAC using R-2R ladder resistance network.

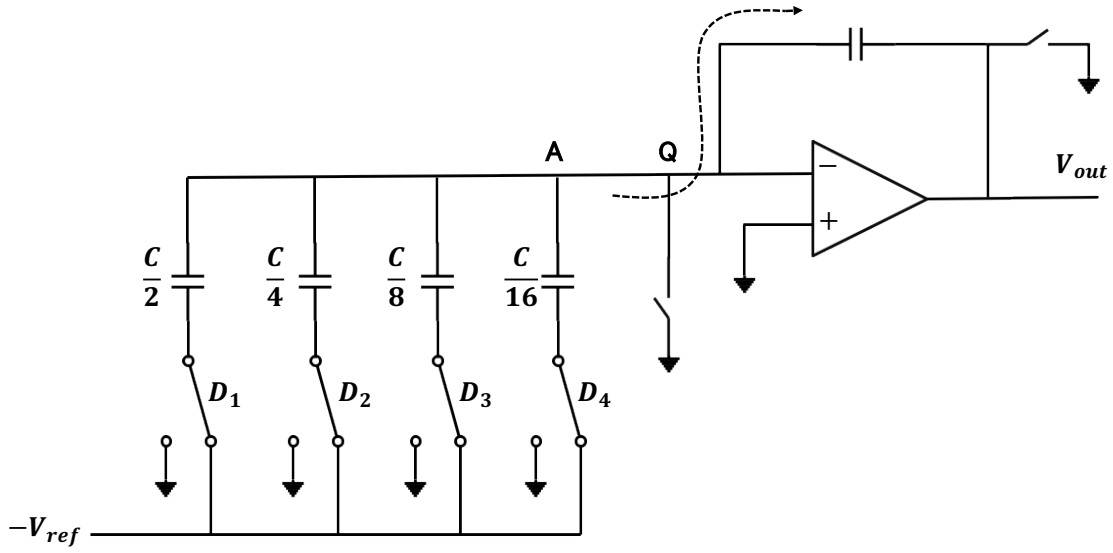


Figure 2.5 DAC using weighted capacitance.

2.2.2 Decoding DAC

Decoding D/A converter uses $2^N - 1$ minimum units of voltage or current to add according to the digital value, so as to perform D/A conversion.

In the case of voltage type, as shown in Fig. 2.6, the resistance equivalent to 1LSB is connected in series. If the reference voltage is applied, the voltage will be generated at each connection point. Therefore, it is realized by

making the switch corresponding to the digital value turn on and taking out the required voltage.

In the current mode, as shown in Fig.2.7, prepare $2^N - 1$ unit current source equivalent to 1LSB, D/A conversion is performed by adding according to the digital value.

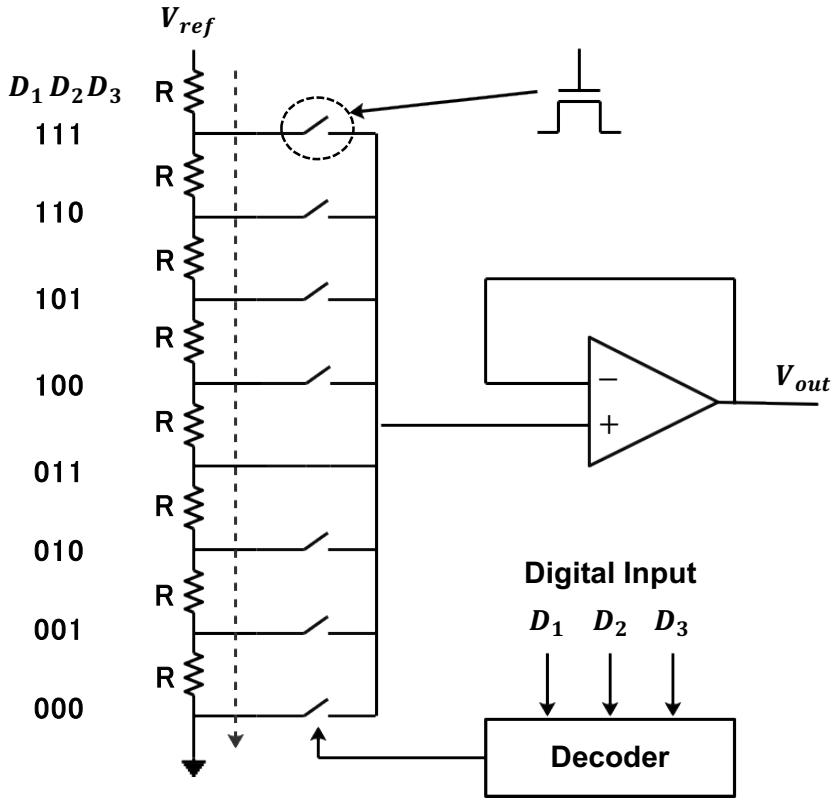


Figure 2.6 Decoding DAC using resistive voltage divider

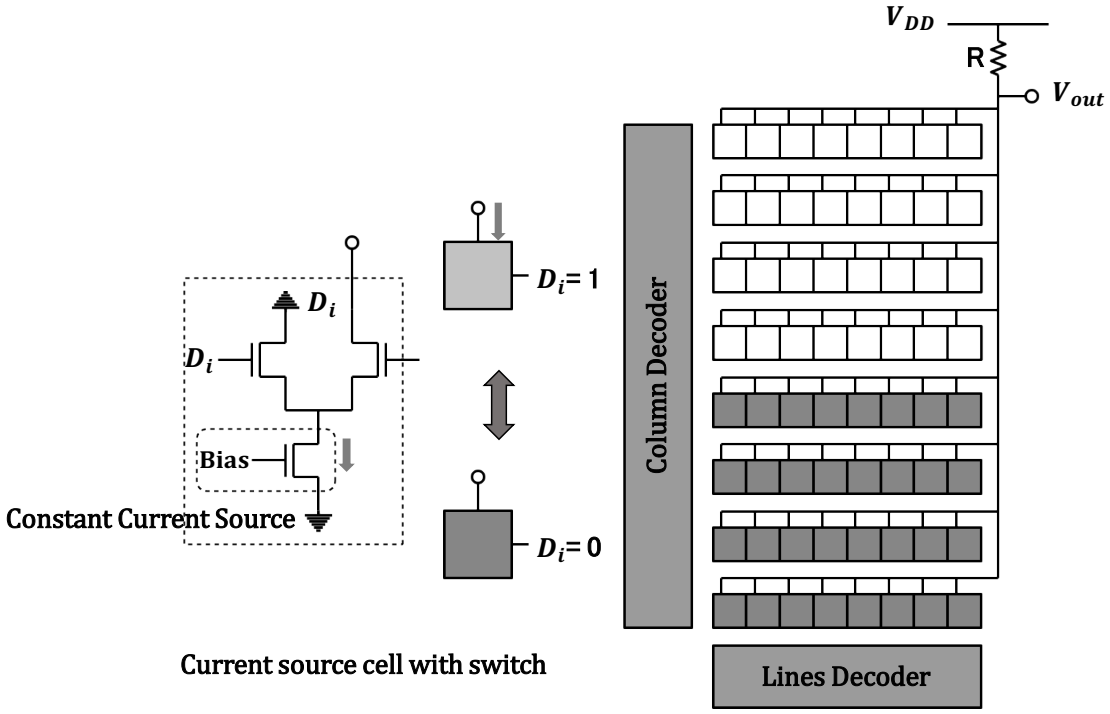


Figure 2.7 Decoding D/A transformer using current source

2.2.3 Binary DAC and Decoding DAC

The binary DAC can be miniaturized due to the small number of components, but on the other hand, the disadvantage is that the component equivalent to MSB has very high sensitivity. Now, assume that the element corresponding to the MSB is shifted by α and becomes $(1+\alpha)$.

Currently, the digital code is [0, 1, 1, ..., 1] and [1, 0, 0, 0], the digital value is only 1 difference, the error becomes $\frac{\alpha}{2}$ for the full scale. If it is represented by LSB, the error is assumed to be $\alpha \cdot 2^N - 1$. The scope of α must be,

$$\alpha < \frac{1}{2^N} \tag{2-8}$$

For example, when the resolution is 10 bits, the accuracy below 0.1% is required.

In contrast, in the decoder type DAC, the differential nonlinearity of 0.5 LSB can be obtained even if the deviation of each component is 50%.

However, the disadvantage is that there are many elements. Compared with the resolution N, the binary DAC can only have about N elements, while the decoder DAC needs about 2N elements.

Therefore, in the actual DAC, as shown in Fig. 2.8, a combination of these two types is used. The upper bit uses the decoder type DAC with low component sensitivity, and the lower bit uses the binary type DAC with few components. In the binary D/A converter, the element sensitivity is high, but it can be reduced by using the low bit.

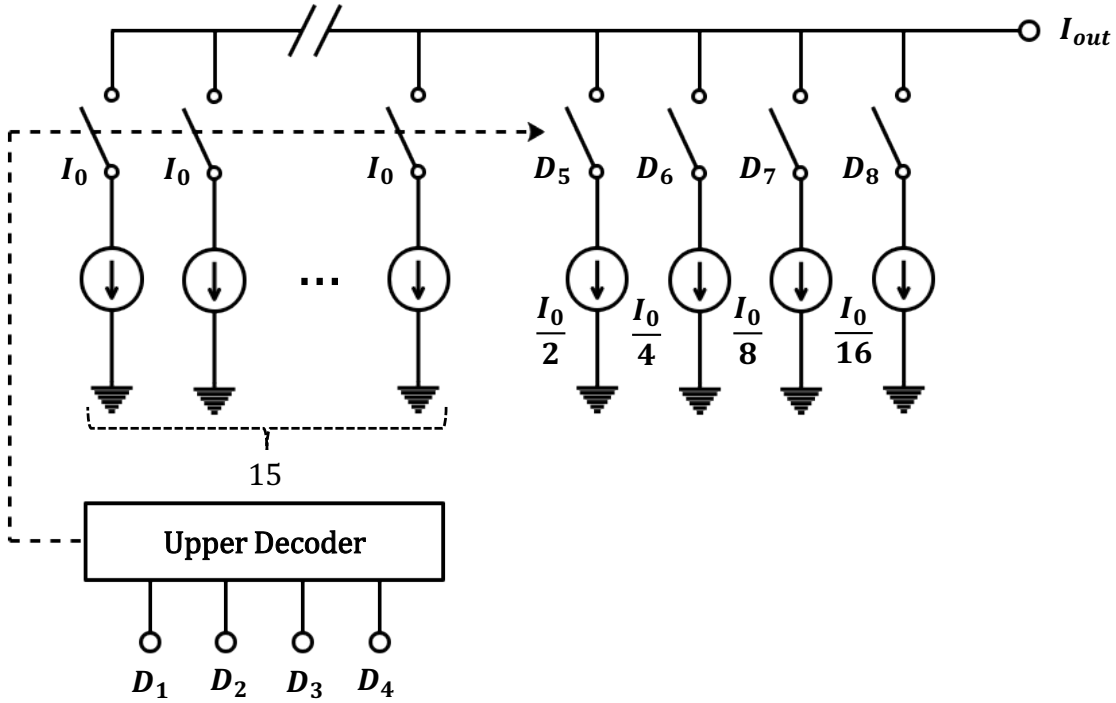


Figure 2.8 DAC using binary type in lower bits, decoding type in higher bits

2.3 Glitch

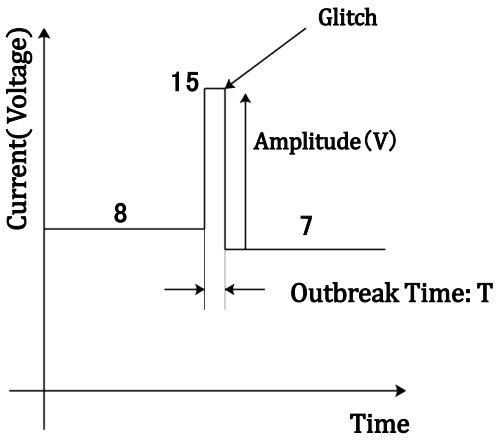
In DACs, a unique phenomenon called glitch is sometimes observed. The glitch, as shown in Fig. 2.9, is a phenomenon that large errors occur only in a short time when the transformation value is transferred, and its beak voltage and electric current sometimes reach half of the full scale. The reason is the time deviation of switch switching. For example, when switching from 81 to 7, all the states of the binary switch are required to change in an instant.

However, if the MSB switch is slightly slower than other switches, the instant 1111=15 is taken as the migration state. Therefore, unwanted components are generated in the signal. The magnitude of change is V, the generation period T is often represented by the glitch energy shown below.

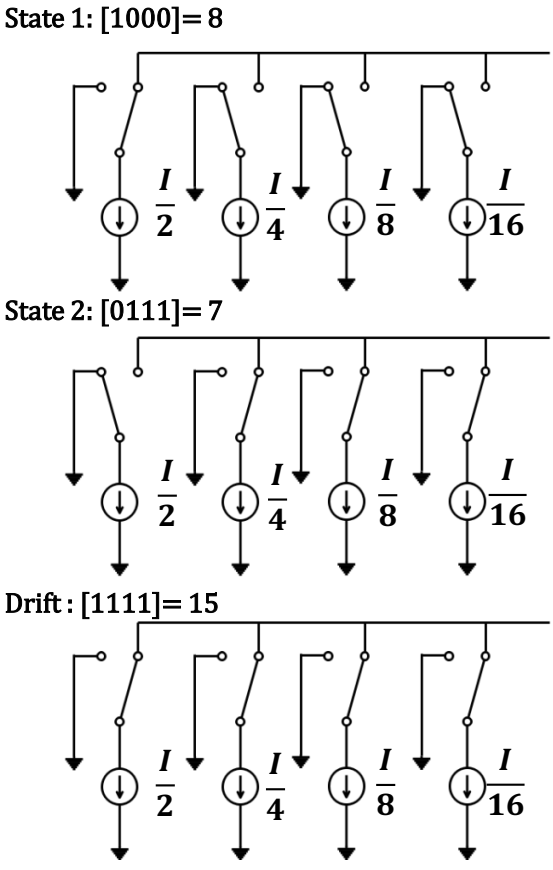
$$E_{glitch} = \frac{VT}{2} \tag{2-9}$$

The generation period is several pico-seconds.

Since the gate is signal dependent, it is considered to distorted, and the conversion characteristics such as SFDR deteriorate when there are many gates. In the generation mechanism, it is easy to occur in the binary DAC, but it is unlikely to occur in the complete decoding type.



(a) Glitch



(b) Circuit status

Figure 2.9 Glitch generation.

2.4 Zero-order Hold Effect

In the D/A converter that converts digital values to analog values, it is difficult to achieve a circuit that only has a value at a certain moment for pulse response, so as shown in Fig. 2.10, the same value is maintained in a cycle for zero time holding. In this case, attention should be paid to the reduction of high-frequency components.

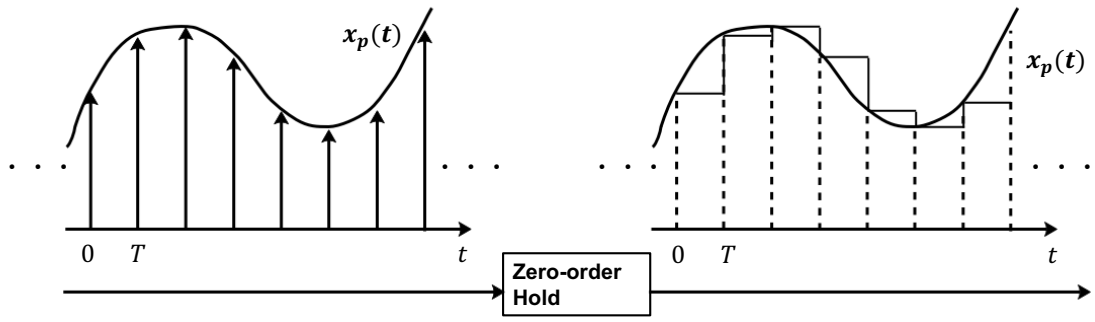


Figure 2.10 Zero-order hold

Fourier transform of zero order hold waveform from 0 to T,

$$X(\omega) = \int_0^T e^{-i\omega t} dt = \frac{1 - e^{-i\omega T}}{j\omega} = T \frac{sin\left(\frac{\omega T}{2}\right)}{\frac{\omega T}{2}} e^{-i\frac{\omega T}{2}} \quad (2\text{-}10)$$

Fig. 2.11 shows the characteristics of absolute value when $x = fT$ and $T = 1$. According to the function shown in Eq. (2-10), it represents the high-frequency attenuation characteristics of zero $\pm N f_s$ ($f_s = \frac{1}{T}$). Therefore, in some cases, it is necessary to compensate for this effect.

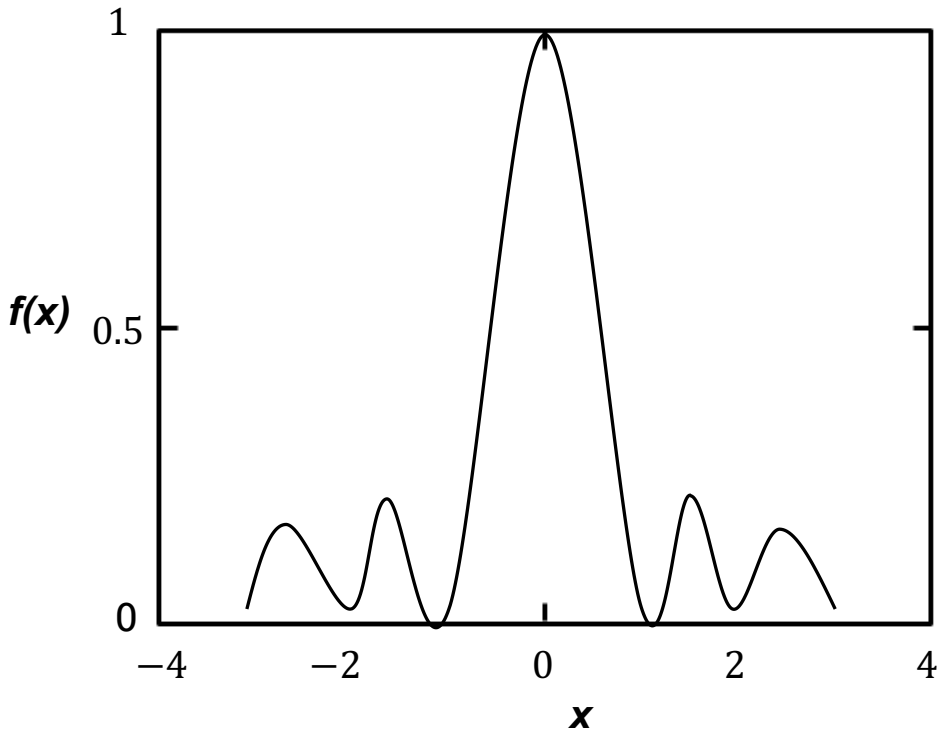


Figure. 2.11 Frequency characteristics of zero-order hold waveforms.

Chapter 3

Polygonal Number DAC

This section describes derivation of our polygonal number DACs.

3.1 Polygonal Number Theory

This subsection briefly explains polygonal numbers in number theory. We take the triangular number as an example, and infer that this consideration can also applicable to other polygonal numbers through the simulation results of the triangular number.

Polygonal numbers are represented as dots or pebbles arranged in the shape of a regular polygon; they are triangular numbers, square numbers, pentagonal numbers, hexagonal numbers, heptagonal numbers, octagonal numbers, and so on, as shown in Fig. 3.1.

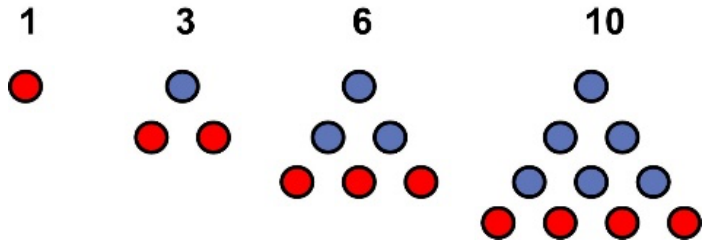
For example, the triangular numbers are given by as follows (see Fig. 3.1 (a)):1, 3, 6, 10, 15, 21, 28, 36, 45, 55, 66, 78, 91, 105…, n(n+1)/2, …

We design DACs based on the following triangular number theoretical properties.

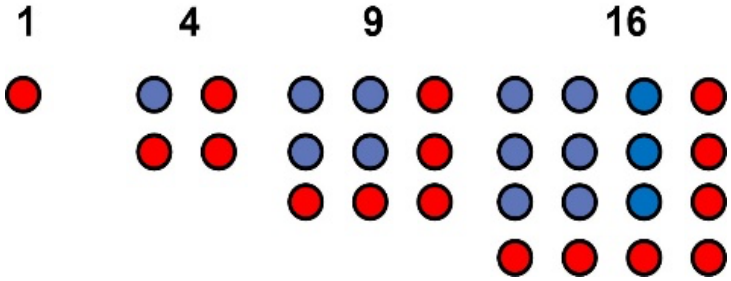
Triangular number theorem:

“Any natural number is composed of 3 or less than 3 triangular numbers”.

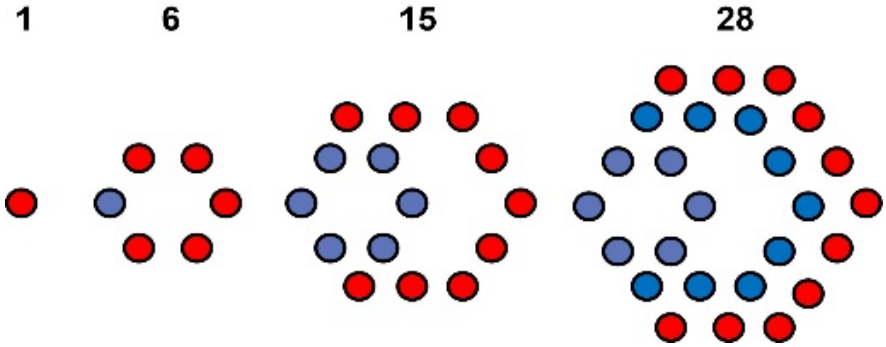
Fig. 3.2 shows its explanation.



(a) Triangular numbers.



(b) Square numbers.



(c) Hexagonal numbers.

Figure 3.1 Explanation of polygonal numbers.

1 :	1	16 :	1+15
2 :	1+1	17 :	1+1+15
3 :	3	18 :	3+15
4 :	1+3	19 :	1+3+15
5 :	1+1+3	20 :	10+10
6 :	6	21 :	21
7 :	1+6	22 :	1+21
8 :	1+1+6	23 :	1+1+21
9 :	3+6	24 :	3+21
10 :	10	25 :	1+3+21
11 :	1+10	26 :	1+10+15
12 :	1+1+10	27 :	6+21
13 :	3+10	28 :	28
14 :	1+3+10	29 :	1+28
15 :	15	30 :	1+1+28

Figure 3.2 Explanation of triangular number theorem.

3.2 Triangular Number DAC

Our derived DAC based on the triangular number theorem is shown in Fig. 3.3. It consists of 3 current sources, 3 switch arrays, a triangular number weighted resistor network and a decoder circuit.

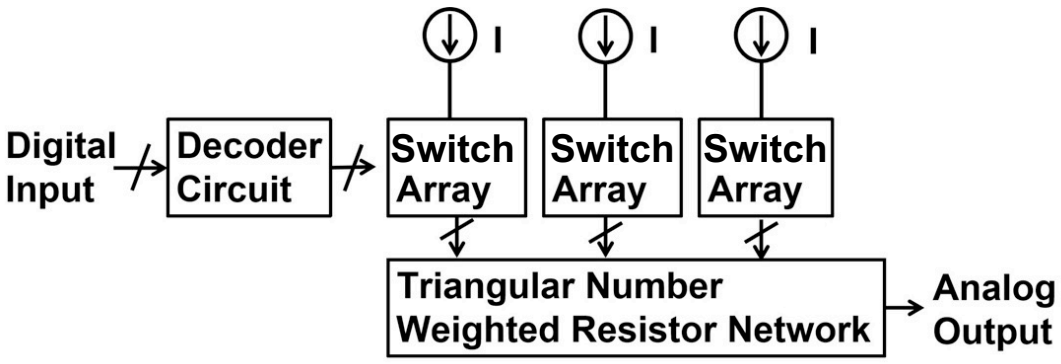


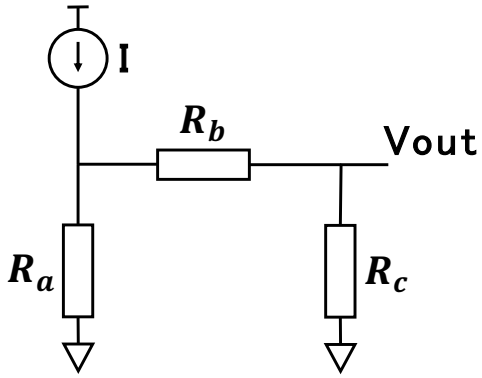
Figure 3.3 Proposed triangular number DAC.

Triangular Number Weighted Resistor Network:

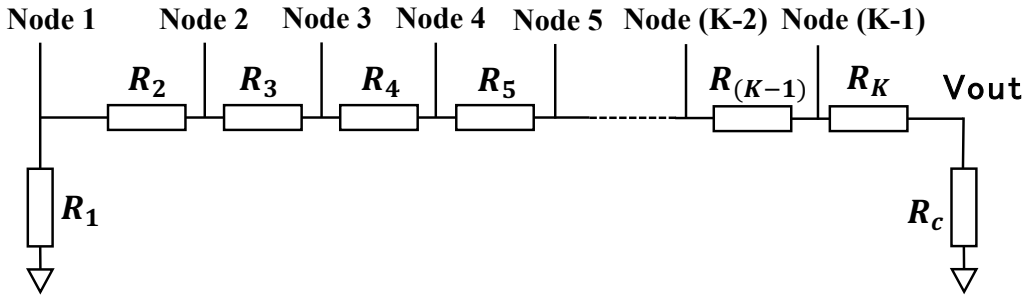
First, we consider the resistor network in Fig. 3.4 (a) and we obtain the output voltage V_{OUT} as follows:

$$V_{OUT} = I \frac{R_a R_c}{R_a + R_b + R_c} \tag{3-1}$$

Here R_c is a load resistor and we see that it changes the gain of the resistive network. Its extension to the network of K resistors and a load resistor R_c is shown in Fig. 3.4 (b).



(a) Three resistors with an input current source.



(b) Extension to K resistors and a load resistor R_c

Figure 3.4 Basic resistor networks.

The key component of the triangular number DAC is the triangular number weighted resistor network in Fig. 3.5, where R_n in Fig. 3.4 (b) is replaced with n R (n=1, 2,…, K) and R is a unit resistor.

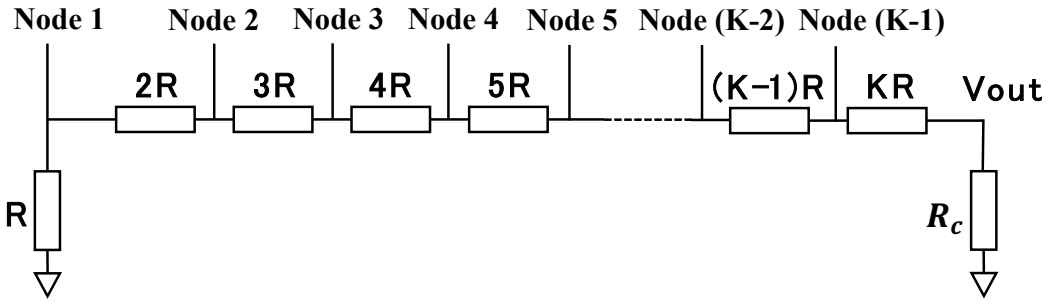


Figure 3.5 Triangular number weighted resistor network.

Fig. 3.6 shows the triangular number weighted resistor network with K=5 and an input current source applied to each node.

We have the following from Fig. 3.4 (a) and Eq. (3-1):

$R_a + R_b = R + 2R + 3R + 4R + 5R = 15R$

$V_{OUT} = I\, R_a\, [R_c \,/\, (R_a + R_b + R_c)]$.

Also $R_c = R$, and then $V_{OUT} = \left(\frac{1}{16}\right) R_a I$.

In Fig. 6 (a), $R_a = R$, $R_b = 2R + 3R + 4R + 5R = 14R$

And $V_{OUT} = \left(\frac{1}{16}\right) RI$.

In Fig. 6 (b), $R_a = R + 2R = 3R$, $R_b = 3R + 4R + 5R = 3R$

And $V_{OUT} = \left(\frac{3}{16}\right) RI$.

In Fig. 6 (c), $R_a = R + 2R + 3R = 5R$, $R_b = 4R + 5R = 9R$

And $V_{OUT} = \left(\frac{6}{16}\right) RI$.

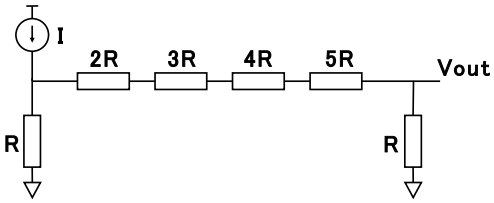
In Fig. 6 (d), $R_a = R + 2R + 3R + 4R = 10R$, $R_b = 5R$

And $V_{OUT} = \left(\frac{10}{16}\right) RI$.

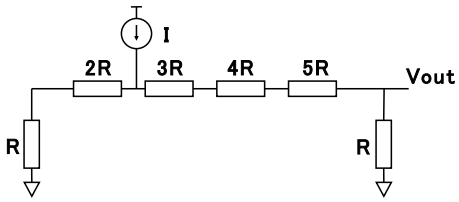
In Fig. 6 (e), $R_a = R + 2R + 3R + 4R + 5R = 15R$, $R_b = 0$

And $V_{OUT} = \left(\frac{15}{16}\right) RI$.

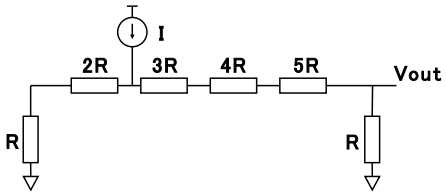
Notice that 1, 3, 6, 10, 15 are triangular numbers. We see that the triangular number weighted resistor network generates a triangular number weighted voltage at V_{OUT} when a current is injected to one node.



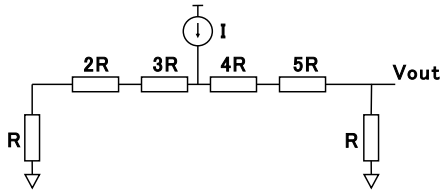
(a) V_{OUT} = (1/16) RI.



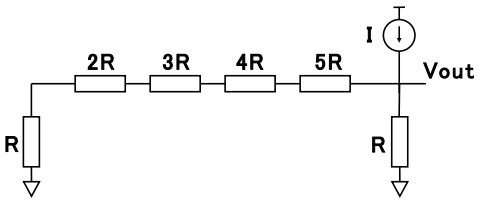
(b) V_{OUT}= (3/16) RI.



(c) V_{OUT}= (6/16) RI.



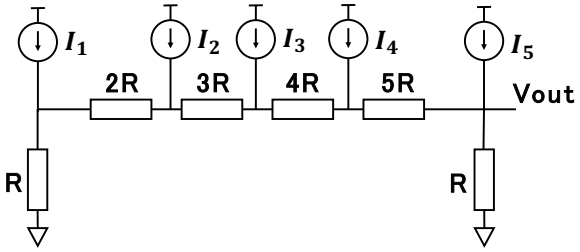
(d) V_{OUT}= (10/16) RI.



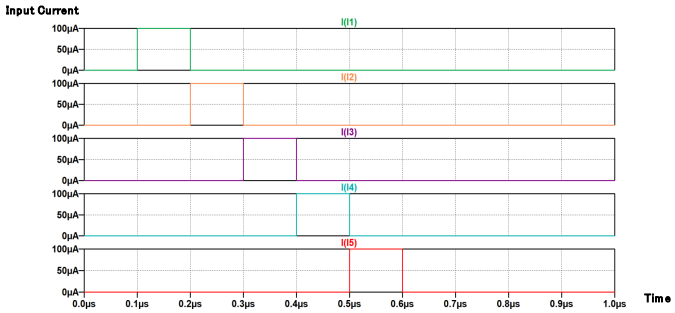
(e) V_{OUT} = (15/16) RI.

Figure 3.6 Operation of the triangular number weighted resistor network, which generates a triangular number weighted voltage at V_{out}.

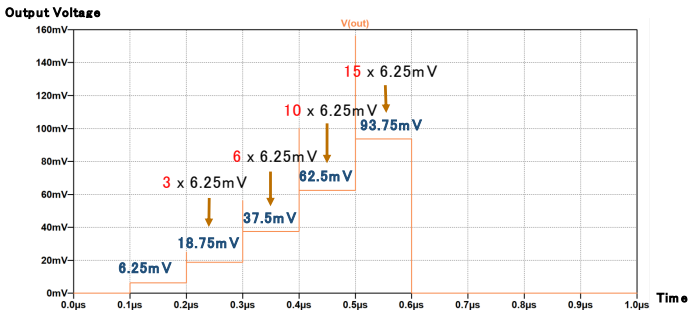
We have performed SPICE simulation for the circuits in Fig. 3.7. Simulation circuit is shown in Fig. 3.7 (a), where $R = 1k\Omega$. The waveforms of the input current sources $I_1 \sim I_5$ are shown in Fig. 3.7 (b) and the waveform of Vout is shown in Fig. 3.7 (c); we see that this simulation result confirms the operations of the circuits in Fig. 3.6, with $R = 1k\Omega$ and $I = 100\mu A$.



(a) Simulation circuit.



(b) Input current source waveforms.

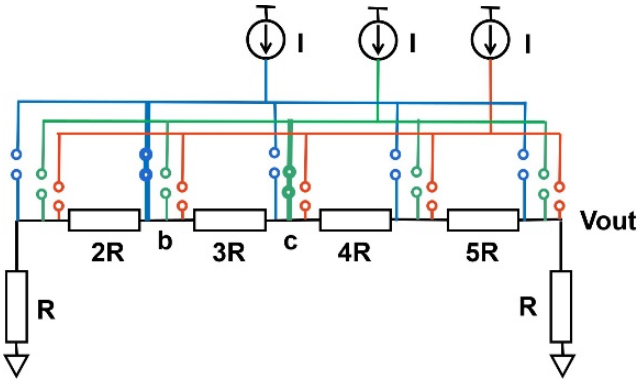


(c) Output voltage (V_{OUT}) waveform.

Figure 3.7 SPICE simulation of the proposed triangular number weighted resistor network.

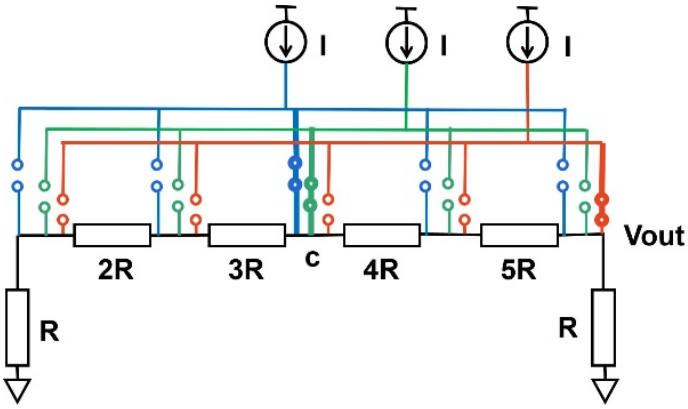
Three Current Sources and Three Switch Arrays:

Based on the theoretical properties of the triangular numbers and the superposition principle, we obtain the input combination for the digital input from 0 to 30 by controlling three switch arrays for three current sources, according to Fig. 3.2. The output of the three current sources is the superposition of the output results of a single current source, so we obtain the results as shown in Fig. 3.7. For example, in the case of the input 9, we need to input two current sources, that is, superimposition of Fig. 3.6 (b) and Fig. 3.6 (c) becomes Fig. 3.8 (a).



(a) In case that the digital input is 9.

$$V_{out} = [(3 + 6)/16]RI$$



(b) In case that the digital input is 27.

$$V_{out} = [(6 + 6 + 15)/16]RI$$

Figure 3.8 Superposition of three current sources to the investigated triangular number weighted resistor network.

Decoder Design:

We have designed a decoder logic for a 6-bit triangular number DAC. Its digital inputs are from 0 to 63, and three switch arrays corresponding to three current sources is represented by Sa, Sb and Sc respectively. There are 11 switches in the switch array of each current source, which are represented by Sa00... Sa10, Sb00... Sb10, Sc00... Sc10.

Due to the large number, we cannot verify the assumptions one by one, so we write an automatic verification program to detect whether all the input conditions are in line with our conjecture. The following is the design principle of the verification program:

Suppose that the digital input is 5 in decimal or B5, B4, B3, B2, B1 and B0 are 000101 in binary. Notice that 1+1+3=5 as shown in Fig. 3.2. Then three switches of Sa1, Sb1, and Sc2 are ON (Sa1 =1, Sb1 = 1, Sc2 = 1) and the other switches are OFF, as shown in Figs. 3.9, 3.10.

The triangular number DAC decoder has the digital inputs of B5, B4, B3, B2, B1, B0 (from 0 to 63 in decimal) and the digital outputs of Sa00, Sa01, Sa02, … Sa10, Sb00, …Sb10, Sc00, … Sc10. Each output logical expression from B5, B4, B3, B2, B1, B0 can be obtained from Fig. 3.2, and each logical expression is verified by a C program with the following algorithm:

Data A, Data B, Data C and Data are defined as follows:

$$\begin{aligned}\text{DataA} = {} & 0\cdot\text{Sa00}+1\cdot\text{Sa01}+3\cdot\text{Sa02}+6\cdot\text{Sa03}+10\cdot\text{Sa04}+15\\ & \cdot\text{Sa05}+21\cdot\text{Sa06}+28\cdot\text{Sa07}+36\cdot\text{Sa08}+45\cdot\text{Sa09}\\ & +66\cdot\text{Sa10}.\end{aligned}$$

$$\begin{aligned}\text{DataB} = {} & 0\cdot\text{Sb00}+1\cdot\text{Sb01}+3\cdot\text{Sb02}+6\cdot\text{Sb03}+10\cdot\text{Sb04}+15\\ & \cdot\text{Sb05}+21\cdot\text{Sb06}+28\cdot\text{Sb07}+36\cdot\text{Sb08}+45\cdot\text{Sb09}\\ & +66\cdot\text{Sb10}.\end{aligned}$$

$$\begin{aligned}\text{DataC} = {} & 0\cdot\text{Sc00}+1\cdot\text{Sbc01}+3\cdot\text{Sbc02}+6\cdot\text{Sbc03}+10\cdot\text{Sbc04}\\ & +15\cdot\text{Sc05}+21\cdot\text{Sc06}+28\cdot\text{Sc07}+36\cdot\text{Sc08}+45\cdot\text{Sc09}\\ & +66\cdot\text{Sc10}.\end{aligned}$$

$$\text{Data} = \text{B0}+2\cdot\text{B1}+4\cdot\text{B2}+8\cdot\text{B3}+16\cdot\text{B4}+32\cdot\text{B5}.$$

Here Sa00, Sa01, Sa02, … Sa10, Sb00, …Sb10, Sc00, … Sc10 are written as designed decoder logical expressions of B5, B4, B3, B2, B1, B0.

The program runs from B5 B4 B3 B2 B1 B0 = 000000 to 11111 and verified the following in all cases:

If $\text{Data} = \text{DataA} + \text{DataB} + \text{DataC}$, the output is OK.

If Data ! = DataA + DataB + DataC, the output is WRONG.

When for all B5, B4, B3, B2, B1, B0, the output is OK, then the decoder logical expressions are correct. The verification program execution results are as shown as Fig. 3.11.

B5	B4	B3	B2	B1	B0					
0	0	0	1	0	1					
Sa0	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Sa7	Sa8	Sa9	Sa10
0	1	0	0	0	0	0	0	0	0	0
Sb0	Sb1	Sb2	Sb3	Sb4	Sb5	Sb6	Sb7	Sb8	Sb9	Sb10
0	1	0	0	0	0	0	0	0	0	0
Sc0	Sc1	Sc2	Sc3	Sc4	Sc5	Sc6	Sc7	Sc8	Sc9	Sc10
0	0	1	0	0	0	0	0	0	0	0

Figure 3.9 DAC decoder logic for the digital input of 5.

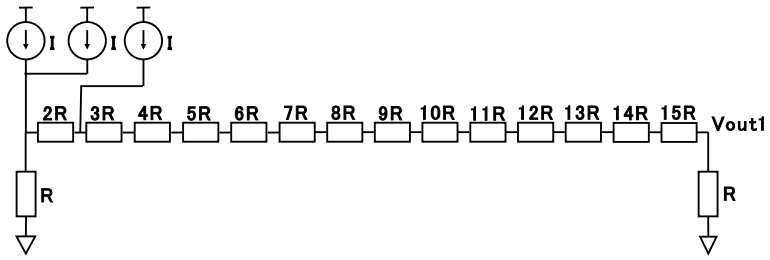


Figure 3.10 Three current sources connection to the triangular number weighted network for the digital input of 5.

```
B5=0, B4=0, B3=0, B2=0, B1=0, B0=0   OK   0=0+0+0
B5=0, B4=0, B3=0, B2=0, B1=0, B0=1   OK   1=1+0+0
B5=0, B4=0, B3=0, B2=0, B1=1, B0=0   OK   2=1+1+0
B5=0, B4=0, B3=0, B2=0, B1=1, B0=1   OK   3=3+0+0
B5=0, B4=0, B3=0, B2=1, B1=0, B0=0   OK   4=1+3+0
B5=0, B4=0, B3=0, B2=1, B1=0, B0=1   OK   5=1+1+3
B5=0, B4=0, B3=0, B2=1, B1=1, B0=0   OK   6=6+0+0
B5=0, B4=0, B3=0, B2=1, B1=1, B0=1   OK   7=1+6+0
B5=0, B4=0, B3=1, B2=0, B1=0, B0=0   OK   8=1+1+6
B5=0, B4=0, B3=1, B2=0, B1=0, B0=1   OK   9=3+6+0
B5=0, B4=0, B3=1, B2=0, B1=1, B0=0   OK   10=10+0+0
```

Figure 3.11 Execution result of the triangular number DAC decoder verification program.

Remark: According to the triangular number theory, any natural number is the sum of three, two or one of triangular numbers. However, notice that its expression is not unique; a given natural number n can be represented by $n = n_1 + n_2 + n_3$ and $n = m_1 + m_2 + m_3$ where n_1, n_2, n_3, m_1, m_2 and m_3 are triangular numbers or 0. For example, in case n=29, 25=10+15 and 25=1+3+21. For the decoder design, we choose one of them for a given input data.

3.3 General Polygonal Number DAC

In general, N-polygonal number theorem is given as follows (N=3, 4, 5, 6, …):

The polygonal number theory:

"Any natural number is composed of N or less than N-polygonal numbers."

This polygonal number theorem was conjectured by French mathematician, Pierre de Fermat and proved by French mathematician, Augustin-Louis Cauchy.

Fig. 3.12 shows out proposed DAC configuration using N-polygonal number properties, which is composed of N current sources, N switch arrays, an N-polygonal number weighted resistor network and a decoder circuit; these are based on the above polygonal number theorem.

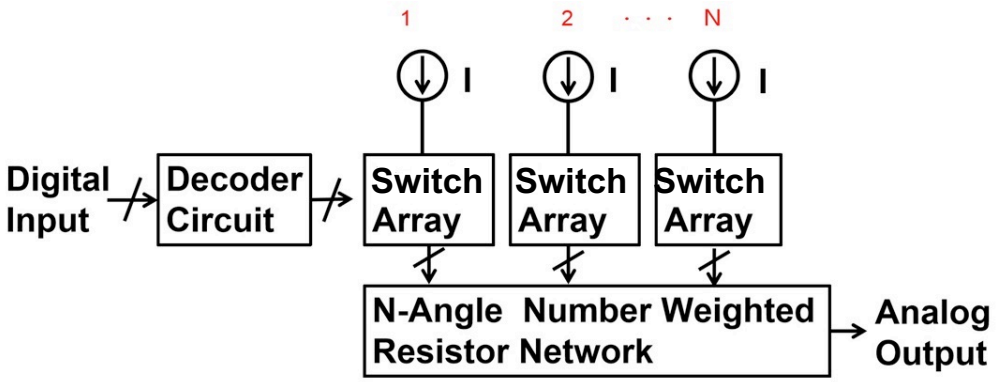
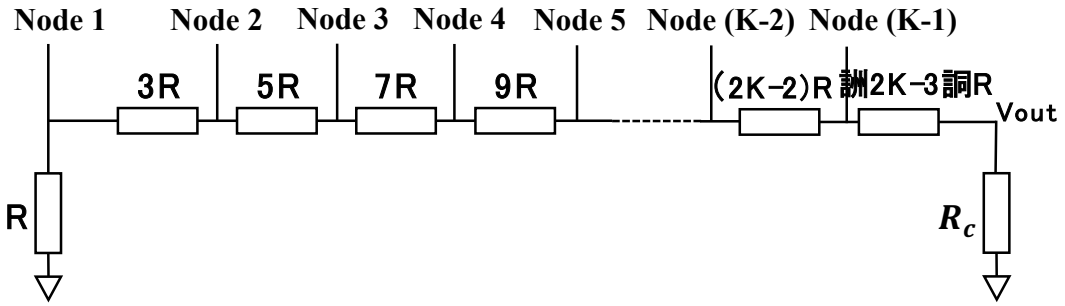


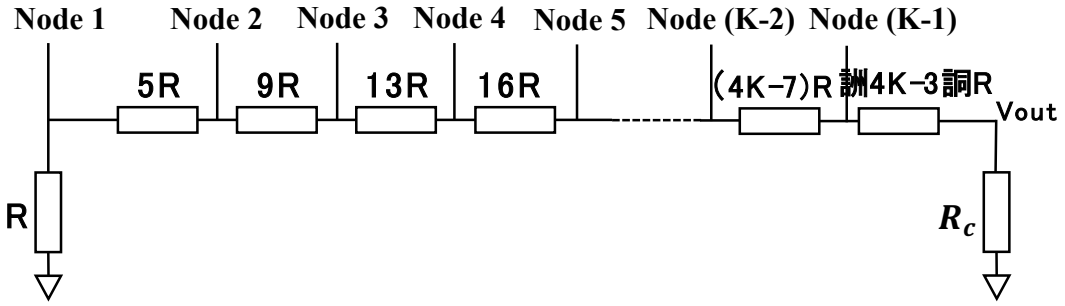
Figure 3.12 DAC configuration based on N-polygonal number.

N-Polygonal Number Weighted Resistor Network:

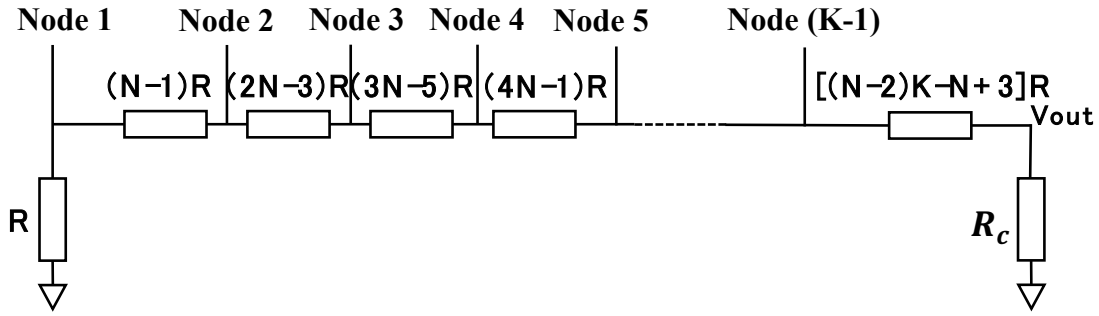
Now we will explain N-polygonal number weighted resistor networks.



(a) Square number weighted resistor network (N=4).



(b) Hexagonal number weighted resistor network (N=6).



(c) N-polygonal number weighted resistor network.

Figure 3.13 Designed N-polygonal number weighted resistor network.

The n-th N-polygonal number $P_N\ (n)$ is given as follows:

$$P_N\ (n) = \frac{(n^2-n)N}{2} - n^2 + 2n \quad \text{(n=1, 2, 3, 4, 5, ….)} \qquad (3\text{-}2)$$

or 1, N, 3N-3, 6N-8, 10N-15, ….

Then the N-polygonal number resistor network using Fig. 3.4 (b) is designed as follows:

R1=R

R2= (N-1) R

R3= (3N-3) R – (R1+R2) = (3N-3) R – (1+(N-1)) R

=(2N-3) R

R4 = (6N-8) R – (R1+R2+R3) R

= (6N-8) R – [1+(N-2) + (2N-3)] R

= (3N-4) R

R5 = (10N-15) R – (R1+R2+R3+R4) R

= (10N-15) R – [1+(N-2) + (2N-3) + (3N-4)] R

= (4N-7) R

Fig. 3.13 shows the N-polygonal number weighted resistor network with K=5 and an input current source is applied to each node.

$$R_a + R_b = R + (N-1)R + (2N-3)R + (3N-5) + (4N-7)R$$
$$= (10N-15)\,R$$
$$V_{OUT} = I\,R_a\,[R_c\,/\,(R_a + R_b + R_c)].$$

Also $R_c = R$, and then $V_{OUT} = \left(\frac{1}{10N-14}\right) R_a I.$

In Fig. 3.13 (a), $R_a = R$, and $V_{OUT1} = \left(\frac{1}{10N-14}\right) RI.$

In Fig. 3.13 (b), $R_a = R + (N-1)R = NR$, and $V_{OUT3} = \left(\frac{N}{10N-14}\right) RI.$

In Fig. 3.13 (c), $R_a = R + (N-1)R + (2N-3)R = (3N-3)\,R$,

and $V_{OUT6} = \left(\frac{3N-3}{10N-14}\right) RI.$

In Fig. 3.13 (d), $R_a = R + (N-1)R + (2N-3)R + (3N-5)R = (6N-9)\,R$,

and $V_{OUT10} = \left(\frac{6N-9}{10N-14}\right) RI.$

In Fig. 3.13 (e), $R_a = R + (N-1)R + (2N-3)R + (3N-5)R + (4N-7)R = (10N-15)\,R$,

and $V_{OUT15} = \left(\frac{10N-15}{10N-14}\right) RI.$

Notice that 1, N, 3N-3, 6N-9, 10N-15 are N-polygonal numbers. They are 1, 3, 6, 9, 15 for N=3 and they are 1, 4, 9, 25, 36 for N=4, while they are 1, 6, 15, 27, 45 for N=6.

We see that the N-polygonal number weighted resistor network generates an N-polygonal number weighted voltage at Vout when a current is injected to one node.

Chapter 4

Prime Number DAC

This section describes derivation of our prime number DACs.

4.1 Prime Number Theory

Prime number is a natural number greater than 1 that cannot be formed by multiplying two smaller natural numbers.

Prime numbers：2, 3, 5, 7, 11, 13, 17, 19, 23, 29, ……

Goldbach conjecture is given as follows (Fig. 4.1):
"All even numbers can be represented by the sum of two prime numbers."
The above conjecture has not been proved yet. However, we can check with numerical calculation that the above conjecture is valid, for example, up-to 2^{21} for 20-bit DAC design.

2 :	2	32 :	13+19
4 :	2+2	34 :	17+17
6 :	3+3	36 :	17+19
8 :	3+5	38 :	19+19
10 :	3+7	40 :	17+23
12 :	5+7	42 :	19+23
14 :	7+7	44 :	13+31
16 :	5+11	46 :	23+23
18 :	7+11	48 :	19+29
20 :	7+13	50 :	19+31
22 :	11+11	52 :	23+29
24 :	11+13	54 :	23+31
26 :	13+13	56 :	19+37
28 :	11+17	58 :	29+29
30 :	13+17	60 :	29+31

+	2	3	5	7	11	13	17	19
2	4	5	7	9	13	15	19	21
3	5	6	8	10	14	16	20	22
5	7	8	10	12	16	18	22	24
7	9	10	12	14	18	20	24	26
11	13	14	16	18	22	24	28	30
13	15	16	18	20	24	26	30	32
17	19	20	22	24	28	30	34	36
19	21	22	24	26	30	32	36	38

Figure 4.1 Explanation of Goldbach conjecture

4.2 Prime Number DAC

Fig. 4.2 shows our proposed prime number DAC circuit based on Goldbach conjecture, which consists of 2 current sources, 2 switch arrays, a prime number weighted resistor network and a decoder circuit.

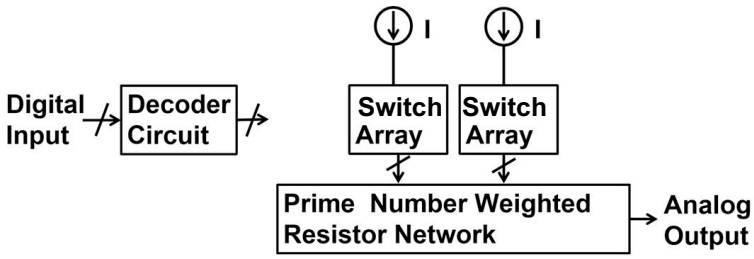


Figure 4.2 Proposed prime number DAC.

We consider the mapping from even number obtained by addition of two prime numbers to the DAC digital input, as shown in Fig. 4.3. Then we have the digital input by "divide by 2 (1-bit right shift)" of two-prime-number addition.

Digital Input		Digital Input	
1 ← 2 :	2	16 ← 32 :	13+19
2 ← 4 :	2+2	17 ← 34 :	17+17
3 ← 6 :	3+3	18 ← 36 :	17+19
4 ← 8 :	3+5	19 ← 38 :	19+19
5 ← 10 :	3+7	20 ← 40 :	17+23
6 ← 12 :	5+7	21 ← 42 :	19+23
7 ← 14 :	7+7	22 ← 44 :	13+31
8 ← 16 :	5+11	23 ← 46 :	23+23
9 ← 18 :	7+11	24 ← 48 :	19+29
10 ← 20 :	7+13	25 ← 50 :	19+31
11 ← 22 :	11+11	26 ← 52 :	23+29
12 ← 24 :	11+13	27 ← 54 :	23+31
13 ← 26 :	13+13	28 ← 56 :	19+37
14 ← 28 :	11+17	29 ← 58 :	29+29
15 ← 30 :	13+17	30 ← 60 :	29+31

Figure 4.3 Mapping from even number obtained by addition of two prime numbers to digital input.

Prime Number Weighted Resistor Network:

Fig. 4.4 shows the prime number weighted resistor network and an input current source applied to each node. Here

$R + R_{p2}$=2R

$R + R_{p2} + R_{p3}$=3R

$R + R_{p2} + R_{p3} + R_{p4}$=5R

$R + R_{p2} + R_{p3} + R_{p4} + R_{p5}$ =7R

$R + R_{p2} + R_{p3} + R_{p4} + R_{p5} + R_{p6}$=11R,

$R + R_{p2} + R_{p3} + R_{p4} + R_{p5} + R_{p6} + R_{p7}$=13R

$R + R_{p2} + R_{p3} + R_{p4} + \cdots + R_{p(K+1)}$

$=$ [K-th prime number] R

Notice that 2, 3, 5, 7, 11, 13 are prime numbers. Then we have the following:

$R_{p2} = R, R_{p3} = R, R_{p4} = 2R, R_{p5} = 2R,$

$R_{p6} = 4R, R_{p7} = 3$

$R_{p(K+1)} = \{K$-th prime number –

$(1+\sum_{i=1}^{K-1}[(K-1)$-th prime number$])\}$ R

(K=1, 2, 3, …)

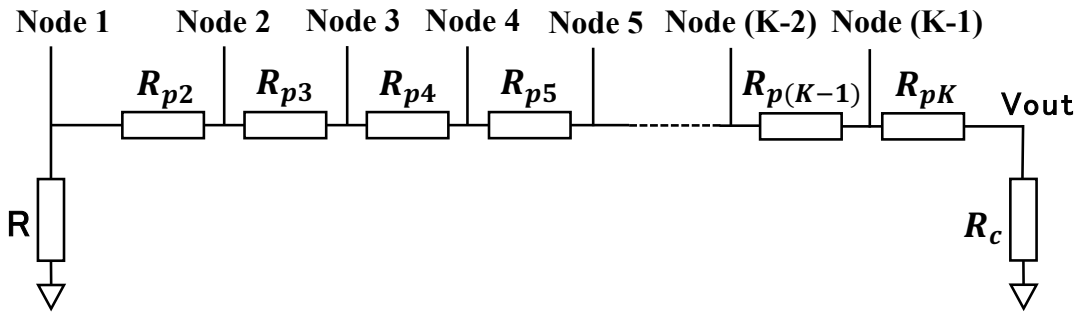


Figure 4.4 Designed prime number weighted resistor network.

We have the following in Fig. 4.5.

$$R_a + R_b = R + R + R + 2R + 2R + 4R + 2R = 13R$$

$$V_{OUT} = I\ R_a\ [R_c\ /\ (R_a + R_b + R_c)].$$

Also $R_c = R$, and then $V_{OUT} = \left(\frac{1}{14}\right) R_a I$.

In Fig. 4.5 (a), $R_a = R$, and $V_{OUT1} = \left(\frac{1}{14}\right) RI$.

In Fig. 4.5 (b), $R_a = R + R = 2R$, and $V_{OUT2} = \left(\frac{2}{14}\right) RI$.

In Fig. 4.5 (c), $R_a = R + R + R = 3R$, and $V_{OUT3} = \left(\frac{3}{14}\right) RI$.

In Fig. 4.5 (d), $R_a = R + R + R + 2R = 5R$,

And $V_{OUT5} = \left(\frac{5}{14}\right) RI$.

In Fig. 4.5 (e), $R_a = R + R + R + 2R + 2R = 7R$,

And $V_{OUT7} = \left(\frac{7}{14}\right) RI$.

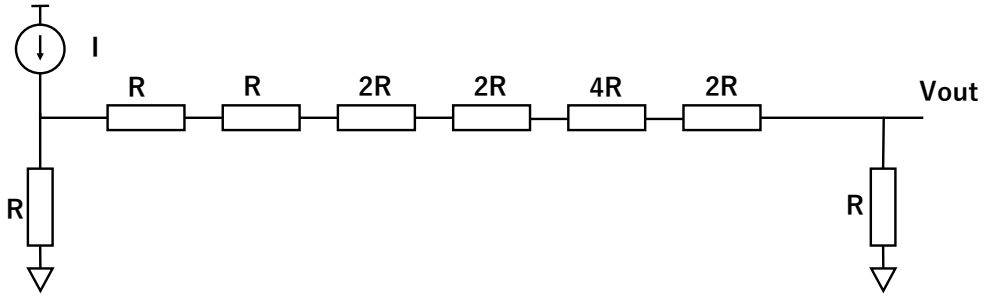
In Fig. 4.5 (f), $R_a = R + R + R + 2R + 2R + 4R = 11R$,

And $V_{OUT11} = \left(\frac{11}{14}\right) RI$.

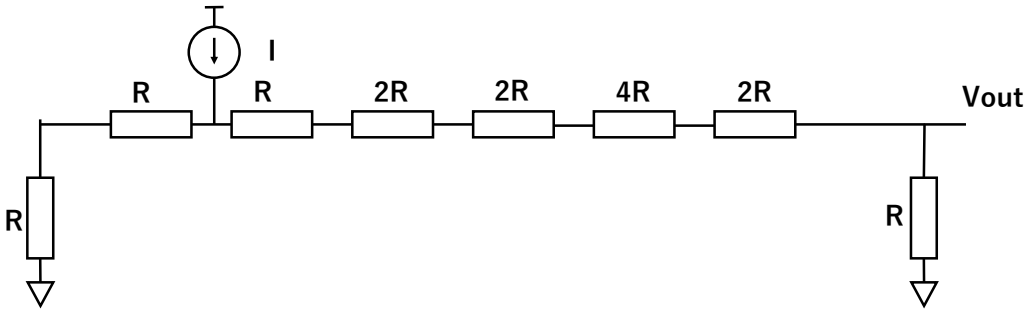
In Fig. 4.5 (g), $R_a = R + R + R + 2R + 2R + 4R + 2R = 13R$,

And $V_{OUT13} = \left(\frac{13}{14}\right) RI$.

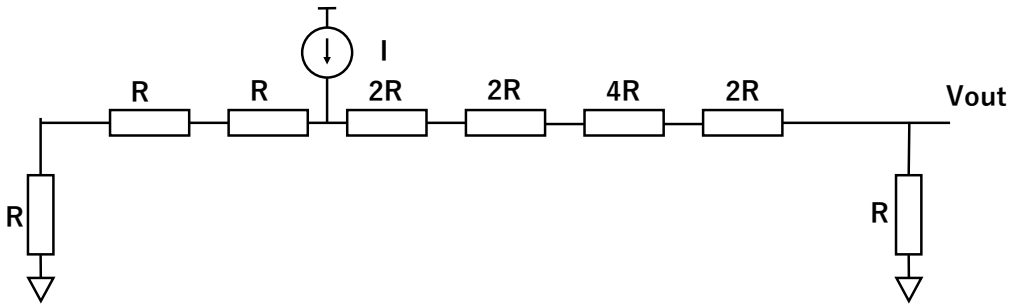
Fig. 4.6 (a) shows the case that the digital input is 6 while Fig. 4.6 (b) is the case it is 8. Note that 5+7 = 2x6 and 5+11 = 2x8. Fig. 4.7 shows the SPICE simulation verification.



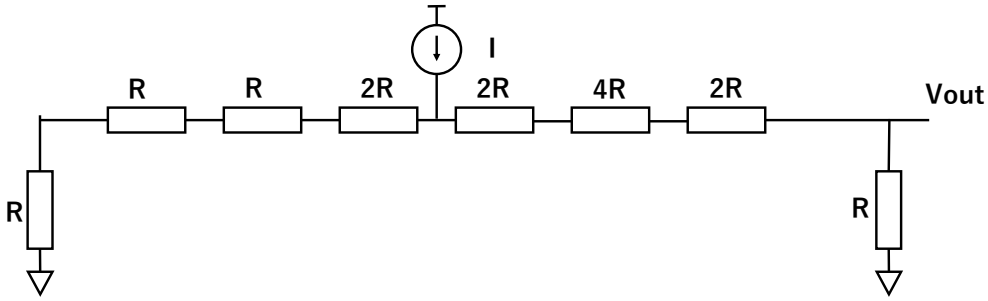
(a) V_{OUT} = (1/14) RI.



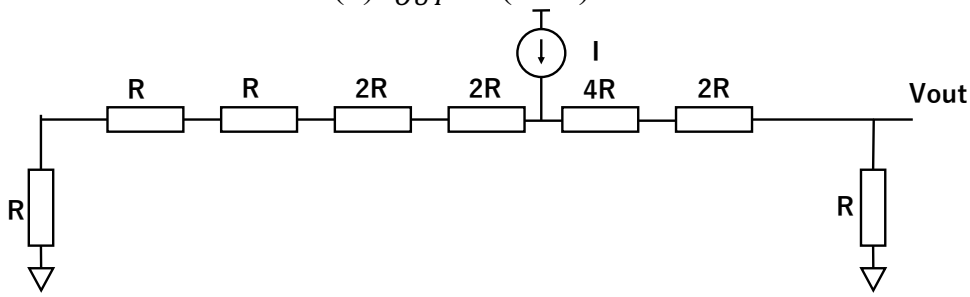
(b) V_{OUT} = (2/14) RI.



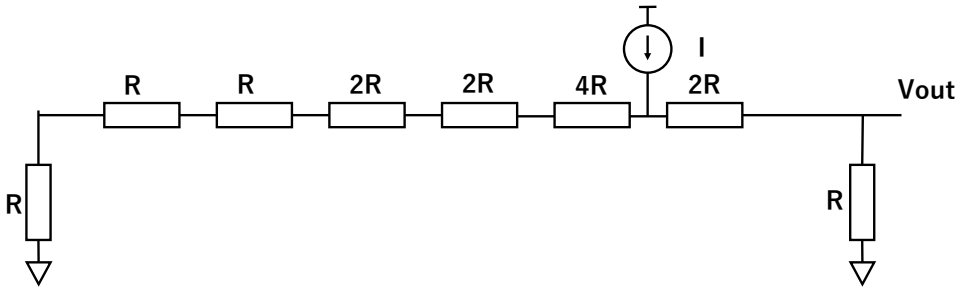
(c) V_{OUT} = (3/14) RI.



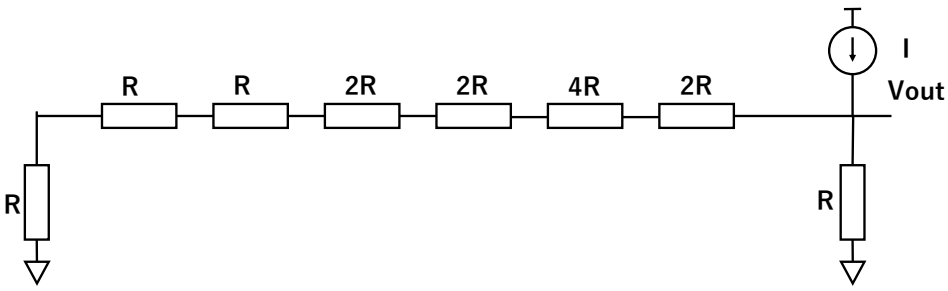
(d)V_{OUT} = (5/14) RI.



(e) V_{OUT} = (7/14) RI.

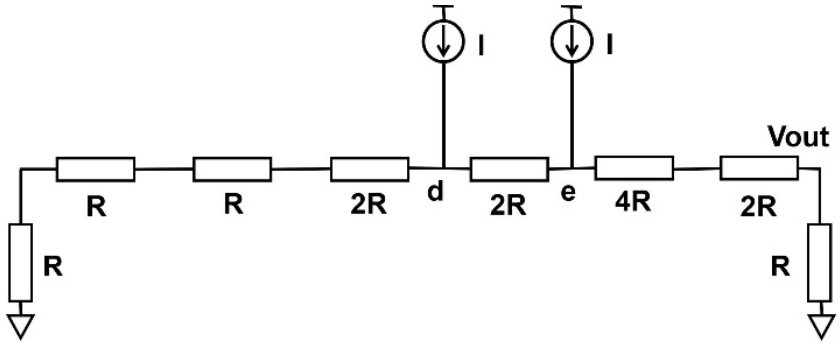


(f) V_{OUT} = (11/14) RI.

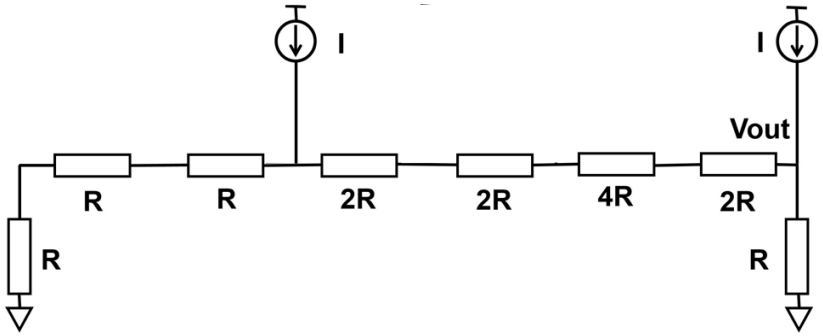


(g) V_{OUT} = (13/14) RI.

Figure 4.5 Operation of the prime number weighted resistor network, which generates the prime number weighted voltage.

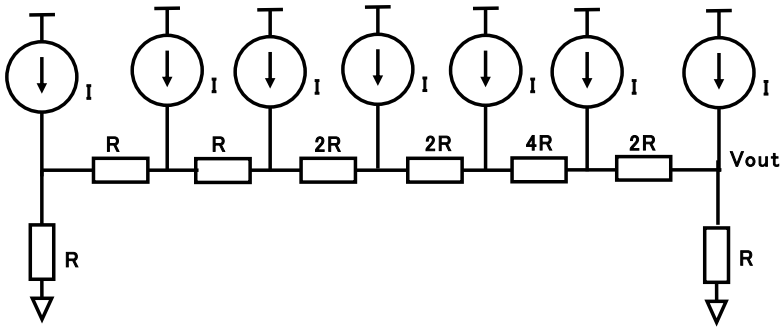


(a) Digital input = 6 and Vout = (6/7) RI.

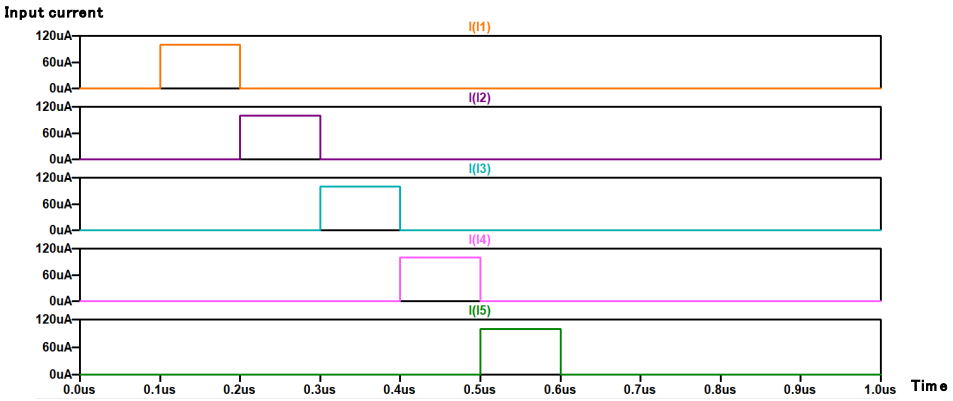


(b) Digital input = 8 and Vout = (8/7) RI.

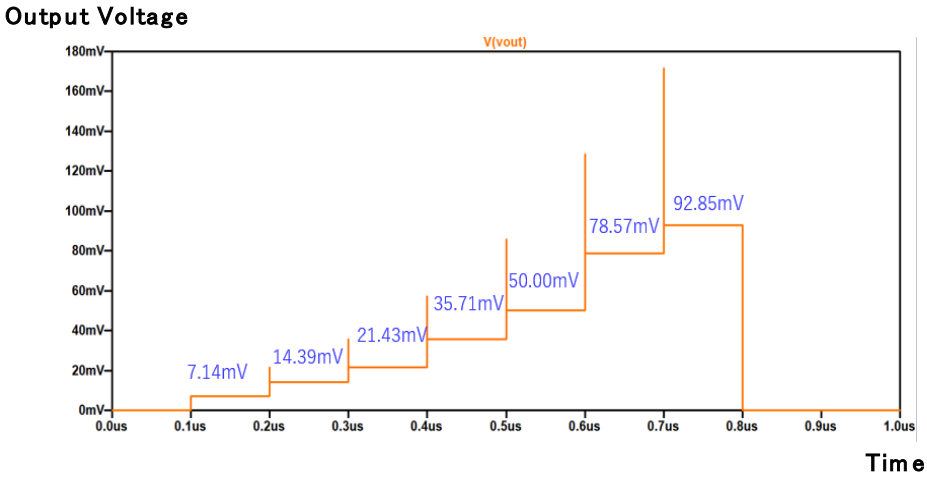
Figure 4.6 Prime number DAC operation



(a) Simulation circuit.



(b) Input current source waveforms.



(c) Output voltage (V_{OUT}) waveform.

Figure 4.7 SPICE simulation of the proposed prime number weighted resistor network.

Switch Arrays and Decoder Design:

We have also designed a decoder logic for a prime number DAC. Its digital inputs are from 0 to 63, and two switch arrays corresponding to two current sources is represented by Sa and Sb. There are 23 switches in the switch array of each current source, which are represented by Sa00... Sa22, Sb00... Sb22.

Due to the large number, we cannot verify the assumptions one by one, so we write an automatic verification program to detect whether all the input conditions are in line with our conjecture. The following is the design principle of calibration program:

Suppose that the digital input is 10 in decimal or B5, B4, B3, B2, B1 and B0 are 000101 in binary. Notice that 3+7=10 as shown in Fig. 4.6. Then three switches of Sa1 and Sb1 are ON (Sa3 =3, Sb5 = 7) and the other switches are OFF, as shown in Figs. 4.8, 4.9.

The prime number DAC decoder has the digital inputs of B5, B4, B3, B2, B1, B0 (from 0 to 63) and the digital outputs of Sa00, Sa01, Sa02, … Sa22, Sb00, …Sb22. Each logical expression is verified by a C program with the following algorithm:

Data A, Data B, and Data are defined by

$$\mathrm{DataA} = 0 \cdot \mathrm{Sa00} + 1 \cdot \mathrm{Sa01} + 2 \cdot \mathrm{Sa02} + 3 \cdot \mathrm{Sa03} + 5 \cdot \mathrm{Sa04} + 7 \cdot \mathrm{Sa05} + 11 \cdot \mathrm{Sa06} + \cdots$$

$$\mathrm{DataB} = 0 \cdot \mathrm{Sb00} + 1 \cdot \mathrm{Sb01} + 2 \cdot \mathrm{Sb02} + 3 \cdot \mathrm{Sb03} + 5 \cdot \mathrm{Sb04} + 7 \cdot \mathrm{Sb05} + 11 \cdot \mathrm{Sb06} + \cdots$$

$$\mathrm{Data} = \mathrm{B0} + 2 \cdot \mathrm{B1} + 4 \cdot \mathrm{B2} + 8 \cdot \mathrm{B3} + 16 \cdot \mathrm{B4} + 32 \cdot \mathrm{B5}.$$

Here Sa00, Sa01, Sa02, … Sa22, Sb00, …Sb22, Sc00 are written as designed decoder logical expressions of B5, B4, B3, B2, B1, B0.

The program runs from B5 B4 B3 B2 B1 B0 = 000000 to 11111 and verified the following in all cases.

If $2 * \mathrm{Data} = \mathrm{DataA} + \mathrm{DataB}$, the output is OK.

If $2 * \mathrm{Data} != \mathrm{DataA} + \mathrm{DataB}$, the output is WRONG.

When for all B5, B4, B3, B2, B1, B0, the output is OK, then the decoder logical expressions are correct. The verification program execution results are as shown as Fig. 4.10.

B5	B4	B3	B2	B1	B0						
0	0	1	0	1	0						
Sa0	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Sa7	Sa8	Sa9	···	Sa22
0	0	0	0	0	1	0	0	0	0	0	0
Sb0	Sb1	Sb2	Sb3	Sb4	Sb5	Sb6	Sb7	Sb8	Sb9	···	Sb22
0	0	0	0	0	0	0	1	0	0	0	0

Figure 4.8 DAC decoder logic for the digital input of 10.

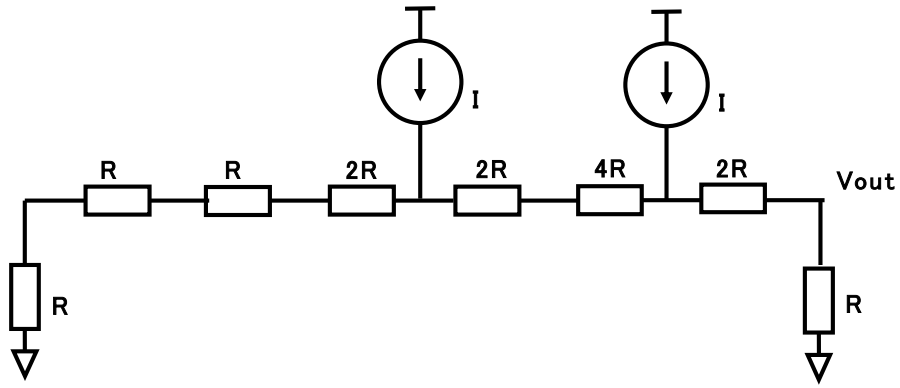


Figure 4.9 Two current sources connection to the prime number weighted network for digital input of 10.

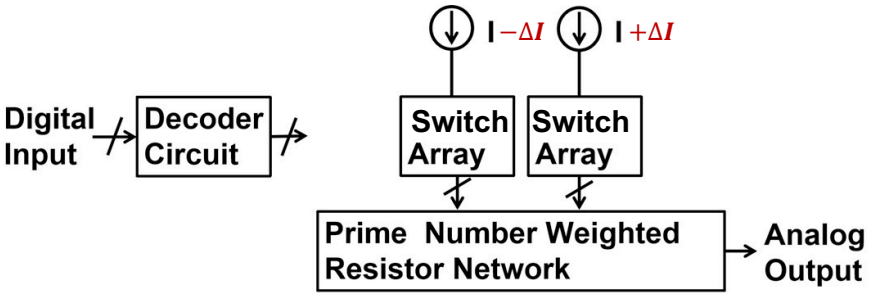
```
B5=0, B4=0, B3=0, B2=0, B1=0, B0=0   OK   0=0+0
B5=0, B4=0, B3=0, B2=0, B1=0, B0=1   OK   2=2+0
B5=0, B4=0, B3=0, B2=0, B1=1, B0=0   OK   4=1+3
B5=0, B4=0, B3=0, B2=0, B1=1, B0=1   OK   6=3+3
B5=0, B4=0, B3=0, B2=1, B1=0, B0=0   OK   8=3+5
B5=0, B4=0, B3=0, B2=1, B1=0, B0=1   OK   10=3+7
B5=0, B4=0, B3=0, B2=1, B1=1, B0=0   OK   12=5+7
B5=0, B4=0, B3=0, B2=1, B1=1, B0=1   OK   14=7+7
B5=0, B4=0, B3=1, B2=0, B1=0, B0=0   OK   16=5+11
B5=0, B4=0, B3=1, B2=0, B1=0, B0=1   OK   18=7+11
B5=0, B4=0, B3=1, B2=0, B1=1, B0=0   OK   20=7+13
```

Figure 4.10 Execution result of the prime number DAC decoder verification program.

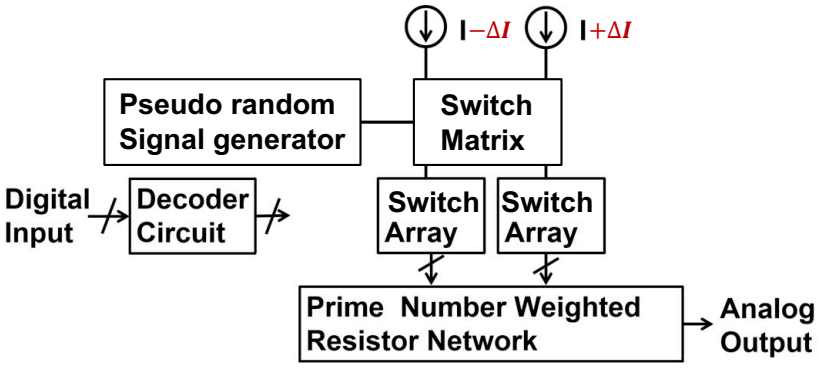
Remark: According to the Goldbach conjecture, any even number is the sum of two prime numbers. However, notice that its expression is not unique; a given even number n can be represented by $n = n_1 + n_2$ and $n = m_1 + m_2$ where n_1, n_2, m_1 and m_2 are prime numbers. For example, in case n=18, 18=5+13 and 18=7+11. For the decoder design, we choose one of them for a given input data.

Dynamic Element Matching (DEM) Techniques [3, 12]

(i)The prime number DAC has two current sources and in actual circuit, they can have mismatches ΔI as shown in Fig. 4.11 (a). However, using the pseudo-random switching, the mismatches can be time-averaged and the spurious components due to them can be spread out in frequency domain using simple circuitry as shown Fig. 4.11 (b).



(a) Current source mismatches.



(b) Dynamic element matching.

Figure 4.11 Current source mismatches and the prime number DAC with dynamic element matching circuit.

(ii) Also the resistors can have mismatches as shown in Fig. 4.12. However, as the above "Remark 2" says, for a given input data, there can be multiple expressions of two-prime number sum. Suppose that the input is DC and its value is 9, and at time *n*, 9x2=5+13 is used while at time *n*+1, 9x2=7+11 is used. If such selections are done dynamically in a pseudo-random manner with modified decoder design, the resistor mismatch effects may be time-averaged and also the spurious components due to them may be spread out in frequency domain.

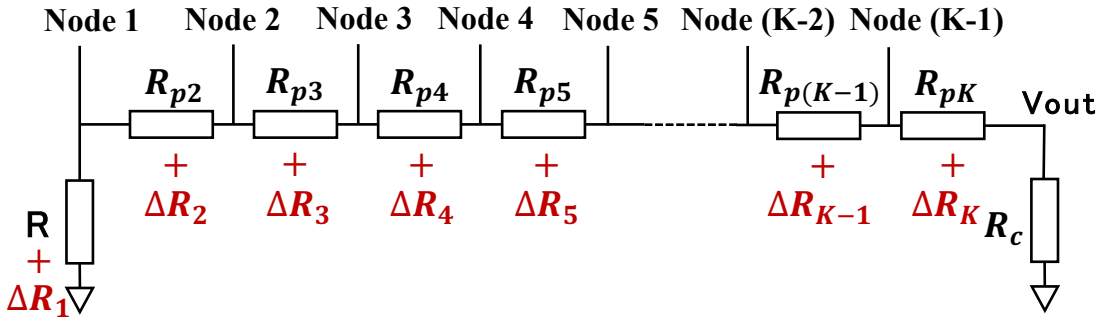


Figure 4.12 Resistor mismatches in the prime number DAC.

Application of these DEM techniques to the prime number DACs and also the N-polygonal number DACs should be further investigated as the next step.

Chapter 5

Conclusion

This paper has demonstrated that new DAC architectures can be derived, based on number theory by integrating the knowledge of mathematics and physical electricity, and their operations are verified by simulation; the theoretical conjecture is consistent with the simulation results. Integers have very interesting properties, but they have not been fully exploited yet for the mixed-signal system and circuit design. We conclude this paper by remarking that in most cases, mixed-signal architecture design is based on designer's experiences but not mathematics, and the attempt of its new architecture derivation from mathematics may have possibilities to lead to very new ones. As the next step, we will consider the derivation of the DAC architectures considering their practical aspects.

Finally, we summarize the number of switches for four types of 6bit ADC. The proposed polygonal number and prime number DACs would be placed between binary and unary DACs in terms of circuit size and possibly performance. Evaluation of the proposed DACs is left as a future work.

Table 3 Comparison of 4 types of 6-bit ADC

	Triangular number DAC	Prime number DAC	Binary DAC	Segment DAC
Number of switches	33	46	6	63
Circuit scale	Medium	Medium	Small	Large
Characteristic	Future work	Future work	Small circuit large glitch, NOT monotonous.	Large circuit small glitch, monotonicity.

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Summary and Future Work

Part 1

The proposed ADC uses switches, capacitors and CMOS chopper-type comparators without operational amplifiers. Hence it can operate with low supply voltage (as below as CMOS switches can work) and low power and is suitable for fine CMOS implementation.

The proposed ADC employs open-loop configuration and hence it can be fast, but its linearity may not be good if care is not taken. It can be used inside a multi-bit ΔΣ AD modulator (Fig. 5.1) [26, 27] where the ADC nonlinearity is noise-shaped. Also it is suitable as a sub-ADC inside a pipelined ADC (Fig. 5.2) [1], where the sub-ADC errors can be compensated by the redundancy of the pipelined ADC circuits. In these applications, kT/C noise and capacitor mismatch effects inside the proposed ADC are compensated and hence its capacitor sizes can be minimized.

The circuits use a minus reference voltage of $-V_{ref}$, but with some circuit design, the usage of $-V_{ref}$ can be avoided (Fig. 5.3).

The proposed ADC is similar to an asynchronous SAR ADC [6-12], a pipelined ADC [1], a sub-ranging ADC [1], or a binary-search ADC [28-31] in some aspects, but has several different points.

This paper has proposed a new ADC architecture with the following features:

1. It uses switches, capacitors and N CMOS chopper-type comparators without operational amplifiers for N-bit resolution. Hence it can operate with low supply voltage (as below as CMOS switches can work) and low power.
2. In each bit generation circuit, each corresponding DAC is embedded.
3. All N comparators as well as the above DACs operate in parallel and the total AD conversion time is the sum of comparator propagation delays and capacitor charge/discharge settling time.
4. Its possible applications are for a sub-ADC inside a multi-bit ΔΣ AD modulator and a pipelined ADC.

The basic circuits of the proposed ADC are shown and its operation is confirmed with LTspice simulation with TSMC 0.18um CMOS process parameters.

We close this part by remarking that the proposed ADC can be extended to a non-binary weighted structure [13-18]; since it can have some redundancy, the decision mistakes of the upper bits can be digitally corrected if the lower bits are obtained correctly, the upper bit generation circuits can be designed with minimum size and power. This would be the next project.

Part 2

This part has demonstrated that new DAC architectures can be derived, based on number theory by integrating the knowledge of mathematics and physical electricity, and their operations are verified by simulation; the theoretical conjecture is consistent with the simulation results. Integers have very interesting properties, but they have not been fully exploited yet for the mixed-signal system and circuit design. We conclude this paper by remarking that in most cases, mixed-signal architecture design is based on designer's experiences but not mathematics, and the attempt of its new architecture derivation from mathematics may have possibilities to lead to very new ones. As the next step, we will consider the derivation of the DAC architectures considering their practical aspects.

List of Publications

Journal Paper

1. **Xueyan Bai**, Shogo Katayama, Dan Yao, Anna Kuwana, Zifei Xu, Haruo Kobayashi, "Asynchronous Capacitive SAR ADC based on Hopfield Network", IEICE Electronics Express, Vol. 19 No. 18. Pages 20220276 (Advance online publication: August 09, 2022) (Published: September 25th, 2022) J-STAGE ELEX
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2. **Xueyan Bai**, Dan Yao, Yuanyang Du, Minh Tri Tran, Shogo Katayama, Jianglin Wei, Yujie Zhao, Anna Kuwana, Haruo Kobayashi, Kazuyoshi Kubo, "Derivation of digital-to-analog converter architectures based on number theory", Journal of Pure and Applied Mathematics, accepted.

3. Dan Yao, Xuanyan Bai, Shogo Katayama, Anna Kuwana, Kazuyuki Kawauchi, Haruo Kobayashi, Kouji Hirai, Akira Suzuki, Satoshi Yamada, Tomoyuki Kato, Ritsuko Kitakoga, Takeshi Shimamura, Gopal Adhikari, Nobuto Ono, Kazuhiro Miura, Shigeya Yamaguchi,
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3. Dan Yao, **Xueyan Bai**, Anna Kuwana, Kazuyuki Kawauchi, Yujie Zhao, Jianglin Wei, Shogo Katayama, Masashi Higashino, Haruo Kobayashi
   "Segmented DAC Unit Cell Selection Algorithm and Layout/Routing Based on Classical Mathematics"
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5. Dan Yao, Xueyan Bai, Anna Kuwana, Kazuyuki Kawauchi, Yujie Zhao, Jianglin Wei, Shogo Katayama, Masashi Higashino, Haruo Kobayashi "Segmented DAC Unit Cell Selection Algorithm and Layout/Routing Based on Classical Mathematics"
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International Conference

1. **Xueyan Bai**, Yuanyang Du, Minh Tri Tran, Anna Kuwana, Haruo Kobayashi, "Digital-to-Analog Converter Architectures Based on Goldbach Conjecture for Prime Numbers in Mixed-Signal ULSI", 30th International Workshop on Post-Binary ULSI Systems (ULSIWS2021), (May 28th, 2021).

2. Dan Yao, **Xueyan Bai**, Anna Kuwana, Kazuyuki Kawauchi, Masashi Higashino, Haruo Kobayashi, Akira Suzuki, Satoshi Yamada, Tomoyuki Kato, Nobuto Ono, Kazuhiro Miura, Kouji Hirai, Ritsuko Kitakoga, "Segmented DAC Unit Cell Selection Algorithm and Layout/Routing Based on Euler's Knight Tour", International Conference on Analog VLSI Circuits (AVIC 2021), (Oct. 18-21, 2021).

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4. Haruo Kobayashi, **Xueyan Bai**, Yujie Zhao, Shuhei Yamamoto, Dan Yao, Manato Hirai, Jianglin Wei, Shogo Katayama, Anna Kuwana, "Classical Mathematics and Analog/Mixed-Signal IC Design", IEEE 14th

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5. Zifei Xu, **Xueyan Bai**, Dan Yao, Anna Kuwana, Haruo Kobayashi, "Revisit to Hopfield Network for Asynchronous SAR ADC and DAC", (Abstract Only) IEEE 3rd International Conference on Circuits and Systems (IEEE ICCS 2021), Chengdu, China (Oct. 29-31, 2021).

6. Haruo Kobayashi, **Xueyan Bai**, Yujie Zhao, Shuhei Yamamoto, Dan Yao, Manato Hirai, Jianglin Wei, Shogo Katayama, Anna Kuwana, "Smart Mathematics Leads to Sophisticated Analog/Mixed-Signal Circuit", 5th International Conference on Technology and Social Science (ICTSS 2021), Kiryu, Japan, (Dec. 7-9, 2021) Online.

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8. Yuanyang Du, **Xueyan Bai**, Manato Hirai, Shuhei Yamamoto, Anna Kuwana, Haruo Kobayashi, Kazuyoshi Kubo, "Digital-to-Analog Converter Architectures Based on Polygonal and Prime Numbers", 17th International SOC Design Conference (ISOCC), Yeosu, Korea (Oct. 21-24, 2020).

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11. **Xueyan Bai**, Dan Yao, Anna Kuwana, Haruo Kobayashi, "Numerical Simulation for Optimization of Unsteady Rotating Wind Turbine", 3rd International Conference on Technology and Social Science (ICTSS2019) Kiryu, Japan (8-10 May, 2019).

12. **Xueyan Bai**, Anna Kuwana and Haruo Kobayashi "Numerical Simulation for Optimization of Unsteady Rotating Wind Turbine", P078, 5th International Symposium of Gunma University Medical Innovation and 9th International Conference on Advanced Micro-Device Engineering, (Dec. 6, 2018).

Domestic Conferences / Seminars

1. **白雪妍**, 杜遠洋, チャンミンチー, 桑名杏奈, 小林春夫(群馬大学)「多角数を用いた DA 変換器アーキテクチャの設計」pp.54-57 (21-19), 2020 年度(第 11 回)電気学会東京支部栃木・群馬支所合同研究発表会, オンライン開催 (2021 年 3 月 1, 2 日).
2. ケイ浩, 桑名杏奈, **白雪妍**, 姚丹, 小林春夫(群馬大学)「CFD 技術を用いたブレード数の異なる S 字型風車の最適形状の検討」pp.76-79 (21-25), 2020 年度(第 11 回)電気学会東京支部栃木・群馬支所合同研究発表会, オンライン開催 (2021 年 3 月 1, 2 日).
3. **白雪妍**, 杜遠洋, 桑名杏奈, 小林春夫, 久保和良, 「多角数および素数の性質に基づくデジタル・アナログ変換器構成の提案」, 電気学会 電子回路研究会, ECT-020-066, Web 開催(2020 年 10 月 8 日(木)).
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5. **Bai Xueyan**, Yao Dan, 桑名 杏奈, 小林 春夫, 「非定常回転風車の最適化のための数値シミュレーション」, ETG-19-38, ETT-19-38, 平成 30 年度 第 9 回 電

気学会東京支部栃木・群馬支所 合同研究発表会, 小山高専 2019 年 3 月 4 日(月), 5 日(火).

Award

1. BEST PRESENTATION AWARD

Xueyan Bai, Dan Yao, Anna Kuwana, Haruo Kobayashi, "Numerical Simulation for Optimization of Unsteady Rotating Wind Turbine", 3rd International Conference on Technology and Social Science (ICTSS2019) Kiryu, Japan (8-10 May, 2019).