学 位 論 文 の 要 旨

DAC Linearity Improvement Algorithms Using Randomization Methods

DA 変換器のランダム化手法による線形性向上アルゴリズム

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The digital-to-analog converter (DAC) is a key component in electronic measurement instruments, communication systems and audio systems, and many applications require highly linear DAC. However, the DAC circuit suffers from manufacturing variations, which degrades the DAC linearity. In this dissertation, two technologies using randomization methods are proposed to reduce the manufacturing variation effects and improve the linearity of the unary DAC. The first one is unit cell selection algorithms in a pseudo random manner based on Magic Square, Latin Square and Euler Knight Tour. This is a static randomization method. It is shown in numerical simulations that these can reduce the systematic mismatch effects among unit cells and improve the DAC linearity. Also the layout and routing EDA tools are developed for these selection algorithms and it is shown that they are feasible for IC implementation. The second one is the method of scrambling both systematic and random mismatches among unit cells dynamically. If it is implemented directly for 2D unit cell array layout, relatively complicated circuit and routing are required. Here the scrambling circuit for virtual 3D unit cell array layout (but actually 1D layout) is considered and it is shown that its circuit and routing are relatively simple. Simulation verifications for the linearity improvement are also demonstrated.

The dissertation consists of five chapters.

Chapter 1 introduces research background for importance of DAC linearity improvement as well as the research motivation and purpose. Also, our approaches are introduced and possible applications of the linear segmented DAC are described.

Chapter 2 introduces basic circuit structure and operation principle of the unary DAC. Also, performance criteria of DAC characteristics and definitions of various characteristic parameters are explained. Error sources for mismatches among unit cells of the unary DAC are studied.

In Chapter 3, various unit cell selection algorithms of the unary DAC for 2D layout are studied. Mathematical characteristics of Magic Square, Latin Square and Euler Knight Tour are introduced. Magic Square has the balance of rows, columns and diagonals, and Latin Square has the balance of each unit, while Euler Knight Tour has both attributes of Knight Tour and Magic Square. Cell selection algorithms in a static pseudo random manner based on Magic Square, Latin Square and

Euler Knight tour are proposed to improve the linearity of the unary DAC by cancelling system mismatch effects among unit cells. Simulation verifications have shown that they can improve the linearity of the unary DAC with the practical assumption of linear, quadratic or linear/quadratic commination systematic mismatches. The effectiveness comparison of the three algorithms as well as the regular conventional algorithm is also shown in simulations. We have also developed a layout and routing design EDA tool for the 2D unit cell arrays for regular, Magic Square, Latin Square, and Euler Knight Tour algorithms, and shown their feasibilities for DAC implementation in an IC.

Chapter 4 studies a unit cell mismatch scrambling method for a high-resolution unary DAC based on virtual 3D layout. DAC for communication applications requires good spurious free dynamic range (SFDR) performance. The SFDR of the unary DAC is degraded due to static characteristics mismatches among its unit cells as well as its dynamic characteristics.

In this dissertation, we focus on the care for the static characteristic mismatches using the dynamic element matching (DEM) for the unary DAC. We consider here the signal bandwidth of the DAC is from DC to the Nyquist rate (half of the sampling frequency) so that the DEM technique only needs to spread the spectrum of the spurious tones caused by the mismatches in the entire signal band uniformly without need for mismatch shaping; this is called as mismatch scrambling. However, direct implementation circuit of such mismatch scrambling for the high-resolution unary DAC becomes complicated. Therefore, first in simulations, a mismatch scrambling technique utilizing the features of 2D regular layout and routing for the unit cells was investigated, utilizing row and column decoders features and this method can reduce the hardware compared to the direct method. Then, we have investigated a more hardware efficient method for a higher resolution DAC, by considering a virtual 3D case, considering X-,Y- and Z-decoders, but there 1D layout is actually used. Its circuit implementation requires only small amount of circuits compared to the conventional methods. Simulation results show that its SFDR can be improved compared to the case without the proposed scrambling method.

Chapter 5 summarizes the research work of this dissertation as well as describes the future work.