Doctoral Thesis

Separate-heater Phase-change Memory for Multilevel Storage

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Abstract

In this work, I have proposed a new phase-change memory (PCM) device with a separate-heater, in order to fulfill the demand of multilevel storage in the non-volatile memories. In typical PCM devices, it still has got some potential problems regarding their crystallization process to obtain intermediate resistance levels for multilevel storage. Rapid change of the resistance value occurs when a SET pulse is induced at the memory layer, $Ge_2Sb_2Te_5$ (GST). This makes the crystallization process difficult to control an intermediate resistance levels for multilevel storage is not likely to be obtained.

 In order to overcome this problem, new device structure of PCM has been proposed. The ability of the separate-heater structure to control the crystallization process in order to obtain multilevel storage was investigated. As the resistance of the heater is constant, the power can be controlled by only amplitude of the SET pulse. Therefore, the annealing temperature for crystallization process can be controlled. This can lead to many intermediate resistance levels, allowing multilevel storage.

This thesis fits the demand of obtaining multilevel storage for PCM device. The manuscript is organized as follows.

In chapter 1, I described a brief introduction on phase-change memory and the issues of flash memory. In addition, as research background for multilevel PCM device, the problem and the objectives of this work were explained.

Chapter 2 was focused on the principle of PCM device, the phase-change material of GST and the cell architecture of PCM device to develop multilevel storage. The electrical properties and the structure of GST were explained.

Chapter 3 described the principle and the structure of proposed separate-heater PCM. Previous device architecture was used with direct-heating of the phase change material. In proposed device, indirect-heating was used with the separate-heater near the phase change memory part only in crystallization process.

In chapter 4, simulation on the separate-heater PCM structure was been done. Intermediate resistance was likely to be obtained through the simulation work. This enables the possibility to achieve multilevel storage for the separate-heater PCM.

Chapter 5 was focused on the fabrication of the device, which consisted of three important processes, wet etching process to expose phase change memory area to outside for sputtering, sputtering process of GST, insulator and heater material, and lift-off process to form both phase change memory and separate heater simultaneously. The device was first being wet etched for 8 min. Then, GST/ZnS-SiO$_2$/TiSi$_3$ layers were

sputtered using a RF sputtering machine model MNS-3000-RF ULVAC. The thicknesses of these layers were 150 nm, 20 nm and 50 nm, respectively. The resist was been lift-off from the device surface by cleaning it with PGMEA solution for 2 min, using an ultrasonic vibration. In the lift-off process, I improved lift-off process by increasing thickness of device isolated insulator to obtain completely prototyped PCM.

Chapter 6 is the most important part for this work. The SET and RESETexperiments were done using the prototyped separate-heater PCM device. A waveform generator (Model 2571, Tabor Electronics, Ltd.) was used to apply SET pulse voltage ranging from 0 V to 2 V for 100 ns to the heater $TiSi_3$ layer. The phase change device resistance R was read at a low pulse voltage. After applying the 100-ns- wide pulse, the PCM resistance dropped from 10^7 to $10^4\,\Omega$, which corresponded to about 10 multilevels as intermediate resistance value. This result agreed with the simulation result. After the resistance of the GST layer became constant in SET mode, a RESET voltage pulse was applied directly to the GST layer until it reached its initial amorphous state. As the results, 3 cycle of SET and RESET switching was obtained. Consequently, it demonstrated that my proposed separate-heater PCM device was operated to be stable and was reproducible together with multilevel PCM.

Lastly, in chapter 7, the work of this thesis was summarized.

要　旨

　本論文は、次世代不揮発性メモリの１つとして期待される相変化不揮発性メモリについて、特に、多値記録に特化した相変化メモリについてまとめたものである。本研究では、相変化材料の結晶相とアモルファス相の２相を利用し、この間に多数の中間点を設けることにより多値記録が実現できる方法を基礎に、このコンセプトに、従来にない構造、新たにヒータを設置し、結晶化時にこれを用いて加熱できる高精度多値記録相変化素子(独自ヒータ相変化素子)を提案し、その可能性について検討した。独自ヒータ相変化素子は、従来素子で行っているメモリ部、相変化材料の直接加熱方式の問題である加熱温度に対する抵抗値変化による加熱温度制御の低下を解消するために提案した。構造は、ラテラル型相変化素子を用いて、相変化記憶部上部に絶縁物を介して独自ヒータを設けた相変化素子を提案した。研究では、メモリ部と独自ヒータ部がクロス構造をしたラテラル型多値記録相変化素子を設計試作した。独自ヒータ相変化素子は、GST（相変化メモリ）の上に、絶縁膜 $ZnS\text{-}SiO_2$ を、その上に $TiSi_3$（独自ヒータ）を成膜し、$TiSi_3$ の電極に電源を結線し、電圧パルス印加可能な素子とした。構造や材料は、コムソル社マルチフィジックスシミュレーションを使用して決定し、素子試作後、実験により、提案した素子が多値記録相変化素子として可能であることを実証した。この結果は、従来技術にない新しい多値記録素子を示し、多値記録相変化メモリ素子の高精度制御の分野、特に、結晶化制御という点で新たらしい一面を拓くものであると考える。

　以下に、本論文の各章の内容について簡単に述べる。

第 1 章では、研究の背景、及び相変化メモリとフラッシュメモリの必要性や性能を比較する。このなかで、相変化の利点と将来性について述べ、次にその技術課題について述べ、本研究の目的を述べる。

第 2 章では、相変化メモリと多値記録の原理を述べる。相変化材料の電気的特性および結晶構造について述べ、問題点について議論する。

第 3 章では、上記問題点を解決するため、本研究で提案した独立ヒータ相変化素子の原理と構造について述べる。従来技術である我々が実験に用いたラテラル型相変化素子の相変化モデルと比較して、議論する。

第 4 章では、有限要素法の原理と構造について、説明する。

第 5 章では、相変化メモリのおける温度分布と抵抗変化を確認するためにはシ

ミュレーションを行った。ここで、独立ヒータ相変化メモリのモデルを使って有限要素法でシミュレーションを行った。最後に温度分布と電圧パルスによる抵抗変化の結果を議論する。

第 6 章では、独立ヒータ相変化メモリデバイスのプロセスについて述べる。ウェットエッチング、スパッタリング及びリフトオフの実験方法と結果について理論する。

第 7 章では、独立ヒータデバイスを用いてパルス印加実験と SET−RESET 実験を行った。抵抗変化の結果を得られて、多値記録の可能性が確認でき、スイッチングサイクルは 3 回を得た。この結果から相変化メモリが安定であることが分かった。

　さらに、多値記録のための素子抵抗制御実験においては、独立ヒータに印加するパルス電圧を徐々に高くしていくと、抵抗が徐々に減少する特性を得た。この結果より、アモルファス相から結晶相に変化し、徐々に相変化層の抵抗値が減少した。このことは、パルス電圧により、高精度に抵抗値を制御できることが分かった。

第 8 章では、この論文のまとめを述べた。

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Chapter 1 Introduction

1.1 Non-volatile Memory technologies

Non-volatile Memory (NVM) technologies are a promising technology in the microelectronics industry. The increasing of functionalities and performances of consumer electronic products such as digital cameras, MP3 players, smart-phones, personal computers, and, more recently for a continuous improvement of memory capacity and features.

At present, Flash memory is by far the dominant semiconductor non-volatile storage technology. Researches are aiming at reducing the cost per bit and recently brought the floating-gate storage concept to its technological limit. In fact, data retention and reliability of floating-gate based memories are related to the thickness of the gate oxide, which becomes thinner and thinner with increasing downscaling [1].

Up to today, more than 30 emerging NVM technologies are have been competing to enter in the fast growing NVM market. Among these, one of the more interesting is the Phase-Change Memory (PCM). PCM relies in the property of special materials, the chalcogenide alloys, having two stable states of the matter, which have different electrical resistivity. Phase transition in PCM is a reversible phenomenon, and is achieved by stimulating the cell with suitable electrical pulses that appropriately heat the material, triggering the phase-change.

The history of phase-change materials began in the 1950s by Dr. Stanford Ovshinky who was researching the properties of a class of glassy materials that exhibited the ability to easily and stably change between two phases. By the late 1960s, he had reported that certain of these materials exhibited a reversible change both in resistivity and reflectivity when changing between a crystalline state and an amorphous state. It

was recognized that this effect could be exploited both for optical memory as well as electronic memory. In a September 28, 1970 issue of Electronics, Energy Conversion Devices, a company formed by Dr. Ovshinsky, in collaboration with Intel's Gordon Moore, reported the world's first electronic phase change array, a 256-bit semiconductor device.

Although the discovery of phase-change materials suitable to be integrated in semiconductor memories dates back to the '70s, the development of viable PCM prototypes has been demonstrated only recently. Today's PCM is the result of the employment of new, faster, phase-change materials, and of manufacturing expertise acquired in more than 10 years of industrial activity. PCMs have the potentiality to improve the performances compared to Flash, featuring faster program, better endurance, and, most of all, much higher scaling potential.

In PCM, information is stored by the process of phase changing form an amorphous phase to a crystal phase of a chalcogenide alloy, which have different electrical resistivity. This phase transition is reversible, which is achieved by applying electrical pulses. Reading the resistance of a PCM cell is achieved by sensing the current through the chalcogenide alloy under bias voltage conditions. The read state, the range from the amorphous state, RESET and the maximum read current, crystalline state SET, is considerably wide, which allows safe storage of an information bit in the cell and also opens the way to the multilevel approach to achieve low-cost high-density storage. Multilevel storage consists in programming the PCM memory cell to one in a plurality of intermediate resistance levels, which allows storing more than one bit per cell. This multi-level storage depends on the electrical properties of the cell materials as well as on the architecture and the size of the memory cell.

1.2 Flash memory issues

Starting in 1980, Toshiba has invented both NOR and NAND types of Flash memory, thanks to Dr. Fujio Masuoka. The name "flash" was used because of the erasure process of the memory contents was the same as the flash of a camera. This invention has been presented at the IEEE 1984 International Electron Devices Meeting held in San Francisco, California.

Flash memory is a non-volatile computer storage chip that can be electrically erased and re-programmed. It is usually used in memory cards, USB flash drives, MP3 players and solid-state drives for general storage and transfer of data between computers and other digital products. Flash memory is non-volatile, meaning no power is needed to maintain the information stored in the chip. In addition, it offers fast read access times and better kinetic shock resistance than hard disks. These characteristics explain the popularity of flash memory in portable devices.

Flash memory stores information in an array of memory cells made form floating-gate transistors. It has two gates of transistor, which are the control gate and the floating gate. Floating gate is electrically isolated by its insulating layer, any electrons placed on it are trapped there and, under normal conditions, will not discharge for a long time. When a floating gate holds a charge, it partially cancels the electric field from the control gate. This modifies the threshold voltage, V_T of the cell. The current flow through the channel is sensed and forms a binary code allowing data to be stored.

Despite all the good things of flash memory, it has its own limitation. Although it can be read or programmed a byte or a word at a time in a random access, it can only be erased a 'block" at a time. In other word, flash memory offers random access read and programming operations, but cannot offer random-access rewrite or erase operation.

Moreover, due to size reduction, the number of electrons stored in the floating gate and flowing in the device channel decreases. For this reason, since a reduced number of electrons are involved in the electronic processes of the cell, effects from trapping and de-trapping phenomena cause threshold voltage instabilities and reading errors [2]. For all these reasons, industry is searching for alternatives to replace the Flash memory. Novel memory strategies have been explored in the last years both by industry and by research centers all over the world, including Ferroelectric RAM and Magnetic RAM [3].

Ferroelectric RAM (FeRAM) is a random access memory that uses a ferroelectric layer instead of a dielectric layer to achieve non-volatility, proposed by researcher from MIT in year 1952 [4]. It is one of the growing number of alternative non-volatile memory technologies that offer the same functionality as Flash memory. The advantages of FeRAM over a flash memory are lower power usage, faster write performance and much number of write-erase cycles. Apart from the advantages, it also have its own disadvantages such as much lower storage densities than Flash memory device, storage capacity limitations and higher cost.

Magnetic RAM (MRAM), in the other hand has been developed since the 1990s. MRAM data is not stored as electric charge or current flows, but by magnetic storage. The elements forms by two ferromagnetic plates, of each of which can hold a magnetic field, separate by a thin insulating layer. One of the two plates is a permanent magnetic magnet set to a particular polarity, the other`s field can be changed to match that of an external field to store memory. It has lower power consumption, faster and does not degrade over time like Flash memory. However, it also has some disadvantages such as high cost and difficult to scale down the size.

Among these, the Phase-Change memory (PCM) technology, based on the reversible phase transformation capability of special alloys named chalcogenides, appears to be particularly promising [5].

Phase change memory (PCM) exploits the large resistance contrast between the amorphous and crystalline states in phase change materials [6]. The amorphous phase tends to have high electrical resistivity, while the crystalline phase exhibits a low resistivity, sometimes 3 or 4 orders of magnitude lower. Due to this large resistance contrast, the change in read current is quite large, opening up the opportunity for the intermediate levels needed for multi-level storage operations [7].

Even though the principle of applying phase change materials to electronic memory was demonstrated as long ago as the 1960s [8], interest in PCM was slow to develop compared to other NVM candidates. However, renewed interest in PCM technology was triggered by the discovery of fast (<100 nanosecond) crystallizing materials such as $Ge_2Sb_2Te_5$ (GST) or Ag and In doped Sb_2Te (AIST) [9] by optical storage researchers. Over the past few years, a large number of sophisticated integration efforts have been undertaken in PCM technology, leading to demonstration of high endurance, fast speed, inherent scaling of the phase change process and high scalability.

Table 1.1 Memory technologies

	Flash	FERAM	MRAM	PCM
Cell size	7-11	30-100	10-30	8-10
Endurance(Write/Read)	10^6	10^{12}	10^{14}	$>10^{12}$
Read time	60 ns	80 ns	30 ns	20 ns
Write time	1 μs	80 ns	30 ns	10 ns
Erase time	1-100 ms/block	80 ns	30 ns	50 ns
Scalability	Fair	Poor	Poor	Good
Scalability limits	Tunnel oxide	Capacitor	Current density	Litho
Multi-state scalability	Yes	No	No	Yes
3D potential	No	No	No	Yes
Relative cost per bit	Medium	High	High	Low

From this Table 1.1, PCM technology turns out to be one of the most interesting candidates among innovative memory technologies. In fact, PCMs present very small cell size with respect to MRAMs and FeRAMs, and much better scalability. The endurance, although lower than in the cases of FeRAM and MRAM, is still high if compared to flash memories. Regarding the programming performances, PCM increases the write speed by at least one order of magnitude with respect to Flash memories, and is suitable for very low-voltage technologies.

The above described properties of PCM technology promise a wide range of potential applications. PCM has about half the cell size, much faster programming, read time on the same order of magnitude and better endurance than Flash memory. Concerning Flash applications, such as solid-states drives, more efforts are needed to reduce the cell size and improve the multilevel capabilities of PCM, in order to reduce the cost per bit.

1.3 Research background

In our lab, lateral structure PCM was used, since it was easier to be controlled and observed than a vertical PCM device. Fig.1.1 shows a SEM image of a lateral PCM device. Switching experiment due to Joule heating was done. The device contained a Si layer at the bottom, with a 15 nm and 200 nm of SiO_2 layer and SiN layer respectively. It has a 50 nm thick TiN electrode on each side. Phase-change material $Ge_2Sb_2Te_5$, insulator $ZnS-SiO_2$ was sputtered with the thickness of 200 nm and 300 nm respectively.
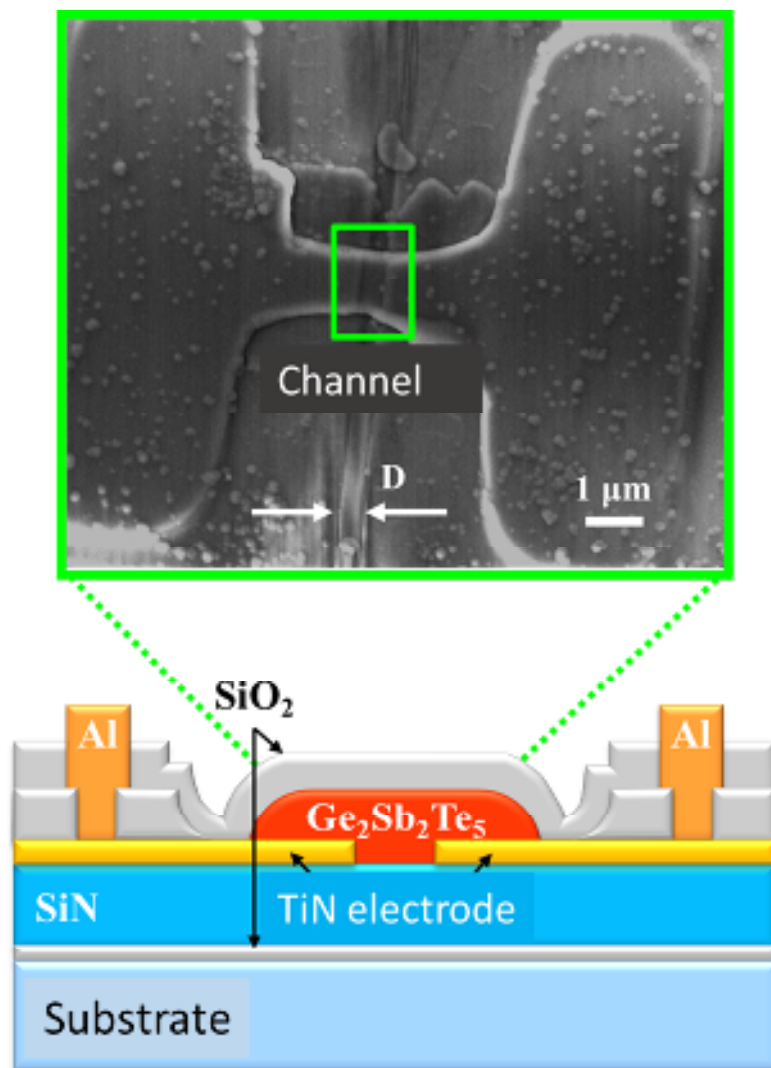
Fig. 1.1 Schematic diagram of a PCM device and its SEM image.

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Fig.1.2 shows switching experiment result of the PCM device due to Joule heating. The graph shows that the PCM was successfully obtained 4 times of switching from amorphous to crystalline and vice versa. The process stopped there because the device was broken and it had been observed using SEM. The figures are shown in Fig. 1.3(a) shows the device image before the experiment and Fig.1.3(b) shows the image after 4 times of switching experiment.
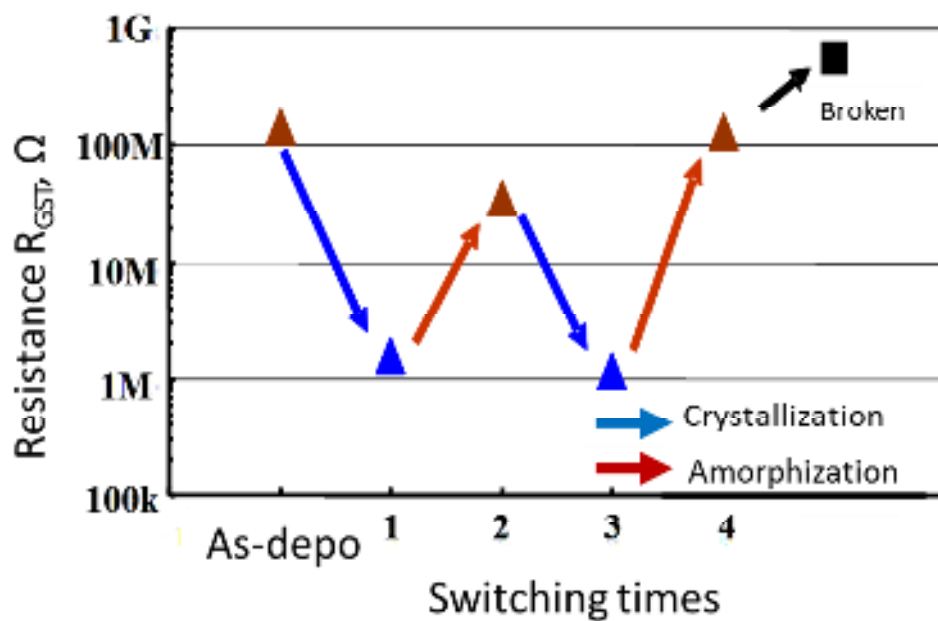

Fig. 1.2 Switching experiment result of the PCM device due to Joule heating.
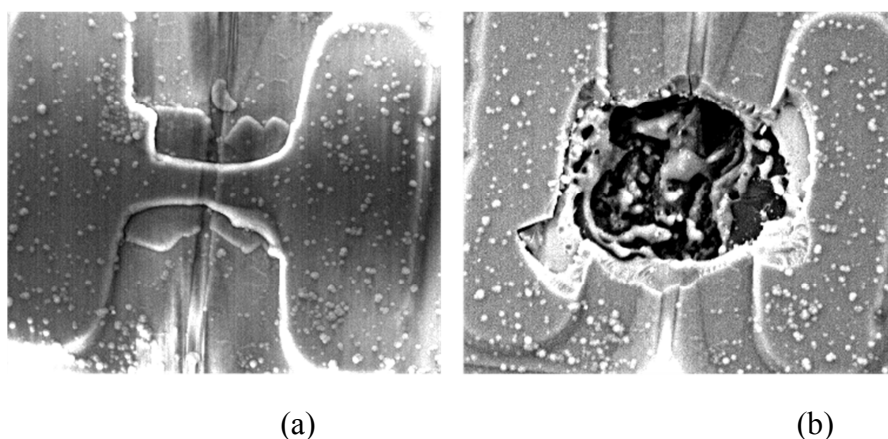

| (a) | (b) |

Fig. 1.3 The device SEM images (a) before the experiment (b) after 4 times of switching experiment.

Other than that, this structure was likely not suitable for multilevel storage, since there was no intermediate resistance level obtained.
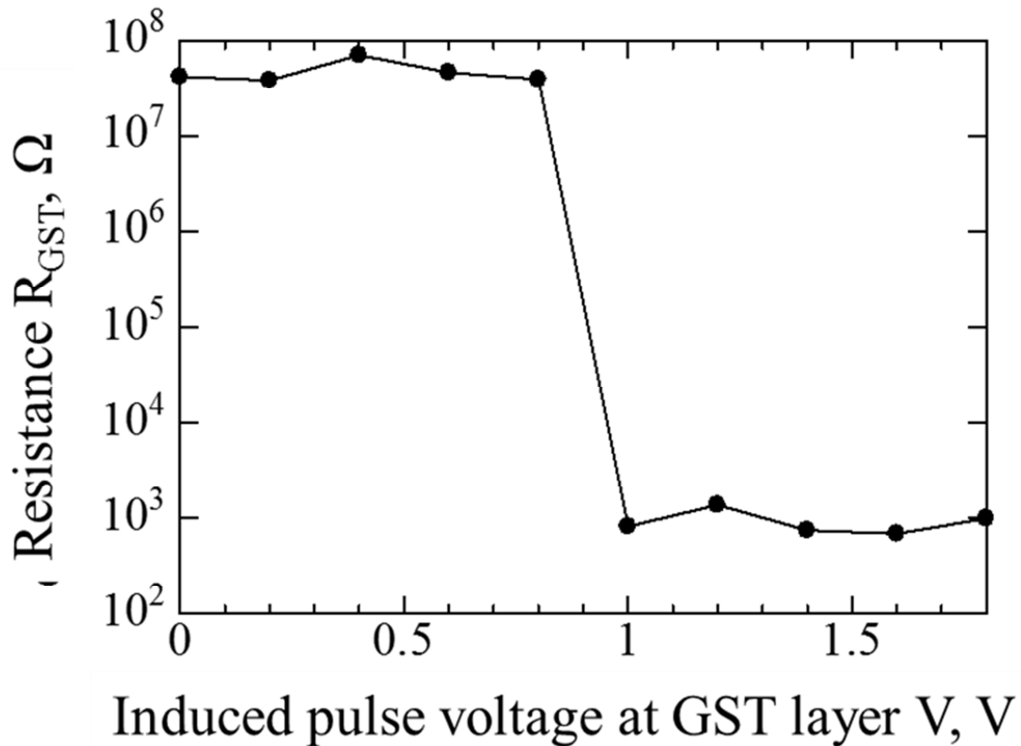

Fig. 1. 4 Resistance drop in GST layer due to increasing pulse voltage.

Fig. 1. 4 shows a resistance drop in the GST layer due to the increasing pulse voltage. It shows a sudden drop of R_{GST} when a SET pulse is applied directly to the GST layer. The as-depo resistance of the GST layer was about 5×10^7 Ω and dropped directly to 7×10^2 Ω at 1 V pulse amplitude without any intermediate resistance level. This indicates that it is difficult to control the crystallization process in order to obtain an intermediate resistance level for multilevel storage in a conventional PCM device.

From the explanations above, the problems are as follows:

1. Precise intermediate resistance levels were not achieved in multilevel PCM during the crystallization process.

2. Only 4 times of switching were demonstrated.

1.4 Objectives

In order to overcome these problems, a PCM device with a separate-heater structure was proposed. It was called separate-heater because the heater layer was not electrically connected to the GST layer since there was an insulator layer to separate the GST memory part from the heat part. The heating of the GST layer is expected be well controlled, allowing a crystallization process with many intermediate resistance levels. This structure will be explained in detail in chapter 3.

The objectives for this thesis are as follows:

1. To propose the separate-heater PCM device.

2. To design our proposed separate-heater PCM device.

3. To develop a fabrication process for the separate-heater PCM.

4. To investigate its possibility to obtain intermediate resistance levels as many as possible based on the crystallization process, which is called SET operation in PCM device.

5. To investigate its reproducibility to switch between amorphous state and crystalline state with many intermediate resistance levels.

1.5 Conclusions

Recently, non-volatile memory (NVM) technologies are in a highly demand der to its increasing of functionalities and performance of consumer electronics. Flash memory is the dominant for this storage technology, however facing problems in reducing the cost because it's already has reached its technological limits.

Phase-change memory, in the other hand, appears to have the potential to overcome this problems. It has lots of advantages such as high endurance, fast speed and high scalability.

Apart of exhibiting lots of advantages, PCM has the disadvantages of difficulties to obtained intermediate resistance level through crystallization process. This makes multilevel storage impossible to achieve. From this, a separate-heater structure PCM device has been proposed. This structure is believed to have the potential to overcome this problem.

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Chapter 2 Phase-Change Memory (PCM)

2.1 The principle of Phase-change memory

Phase-Change Memory devices employ chalcogenide alloys. Chalcogenides are semiconducting glasses made of elements of the VI group of the periodic table, such as sulfur, selenium and tellurium. First investigations on the electrical properties of the chalcogenide materials was done by S.R. Ovshinsky in the late 1960's [1]. The concept of a non-volatile PCM, based on the properties of the chalcogenide alloys, came out at the beginning of 1970's [2]. In these devices, the memory element is basically a variable resistor made of a chalcogenide material.

This alloy possesses a very unique properties. The phases of chalcogenide alloy can be changed from amorphous to crystalline or vice-versa. The resistance of the amorphous phase will be high. After being heated at 450 K, it will transformed to the crystalline phase with low resistance value. The material will returned back to its normal phase, which is amorphous by being melt at 900 K and fast cooling. This process is shown in Fig. 2.1.
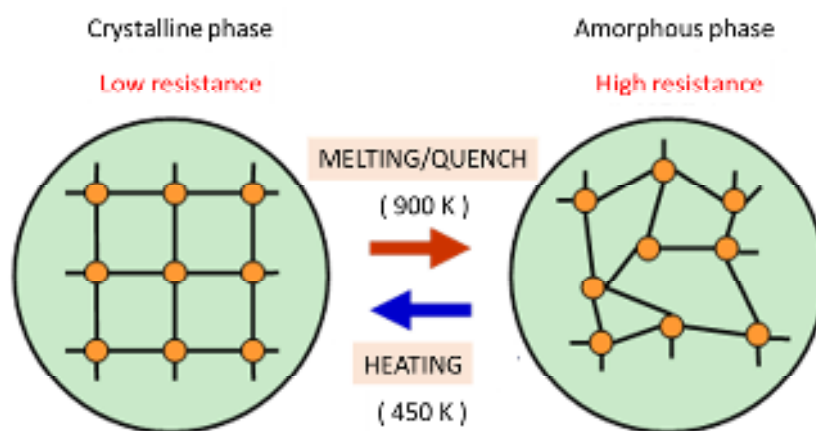

Fig.2.1 Schematic diagram of phase changing of the phase-change material.

To SET the cell into its low-resistance state, an electrical pulse is applied to heat a significant portion of the cell above the crystallization temperature of the phase change material. This SET operation tends to dictate the write speed performance of PCM technology, since the required duration of this pulse depends on the crystallization speed of the phase change material. SET pulses shorter than 10ns have been demonstrated [3-5]. In the RESET operation, a larger electrical current is applied in order to melt the central portion of the cell, as shown in Fig. 2.2.
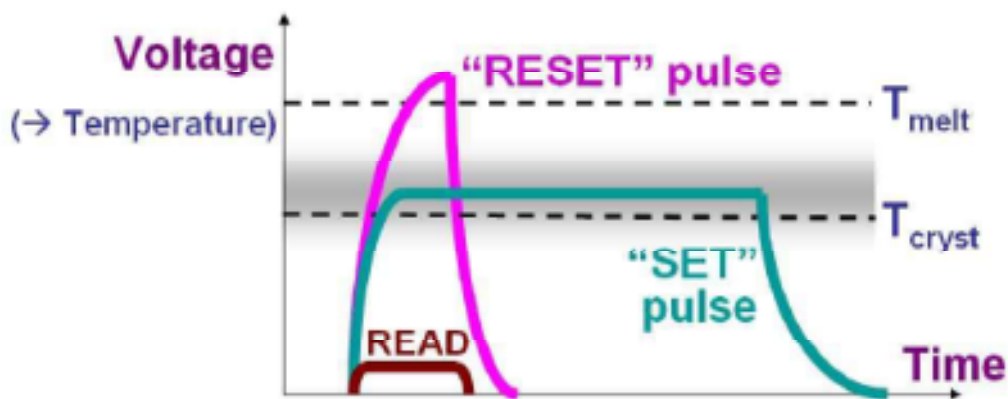
Fig. 2.2 Thermal-induced switching of the phase-change material, either by melting and subsequent quenching in the amorphous phase (RESET pulse), or by heating in the solid state inducing crystallization of the amorphous state (SET pulse).

Today, the most known and used chalcogenide material is $Ge_2Sb_2Te_5$ (GST), but many others are under investigation such as doped GST and GeTe-based alloys in particular. Since early 2000, different semiconductor industries have considered the exploitation of the PCM concept for large-size solid state memories. Compared to the Flash mainstream, the PCM technology features potential of better scalability [6], faster programming time [7] and an improved endurance [8].

2.2 Phase-change materials

Chalcogens on reaction with more electropositive elements results in the formation of an alloy called chalcogenides. These resultant chalcogenide alloys are chameleon compounds, they can be crystalline or amorphous, metallic or semiconducting and conductors of ions or electrons [9]. The chameleon nature of some chalcogenide alloys which possess amorphous and crystalline state holds the following characteristics.

When the alloy is in the amorphous state, characteristics like short range atomic order, low free electron density, high resistivity and high activation energy has been observed. On the contrary while it is in crystalline state, characteristics like long range atomic order, high free electron density, and low resistivity with value of up to four orders of magnitude lower than the one of amorphous state and low activation energy were observed. This tremendous difference in material characteristics paved the path to the discovery of PCM devices. Transmission Electron Microscopy images of amorphous and crystalline phase of a chalcogenide alloy has been shown on the following Fig. 2.3.
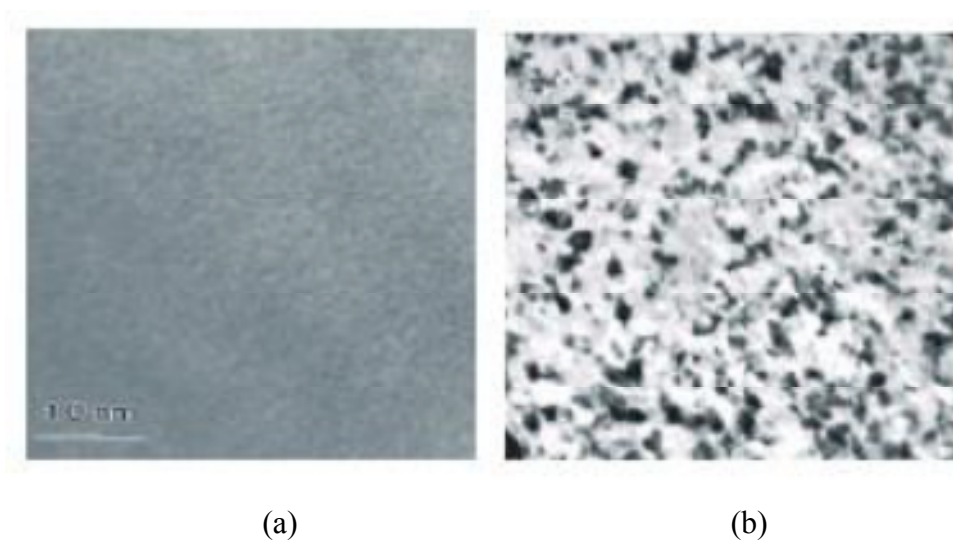

(a)   (b)

Fig 2.3 Transmission Electron Microscopy Images of the amorphous (a) and Crystalline phases (b) of a chalcogenide alloy ($Ge_2Sb_2Te_5$) [10].

The data storage in PCM devices is achieved by the reversible transformation between the amorphous and crystalline phases which exhibit different electrical properties. As the phase transformation of these materials directly corresponds to the speed of the device, fast crystallization and amorphization of the core material is expected.

Out of these, the ternary chaclogenide alloys formed by the composition along the GeTe – Sb_2Te_3 pseudo binary tie line have been chosen as the material for the application to PCM. The following figure shows Ge : Sb : Te ternary phase diagram.
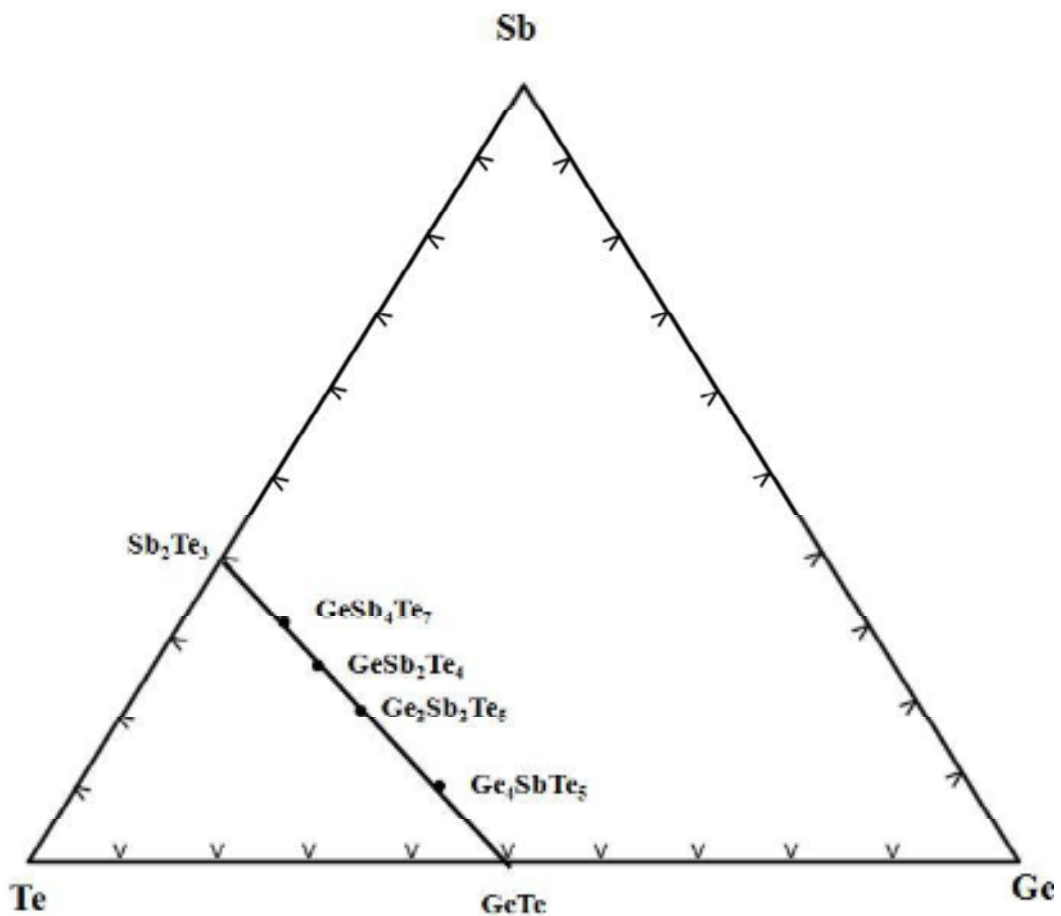
Fig.2.4 : Ge : Sb : Te ternary phase diagram.

Out of the alloys, $Ge_2Sb_2Te_5$ (GST) has been chosen. The reason is that $Ge_2Sb_2Te_5$

has the following characteristics which satisfies the requirement of phase change memory devices.

1. High thermal stability at room temperature (can remain stable for more than 30 years)

2. Very high crystallization rate (can be crystallized in less than 20 ns).

3. Extremely good reversibility between amorphous and crystalline phases (more than 10^{13} cycles).

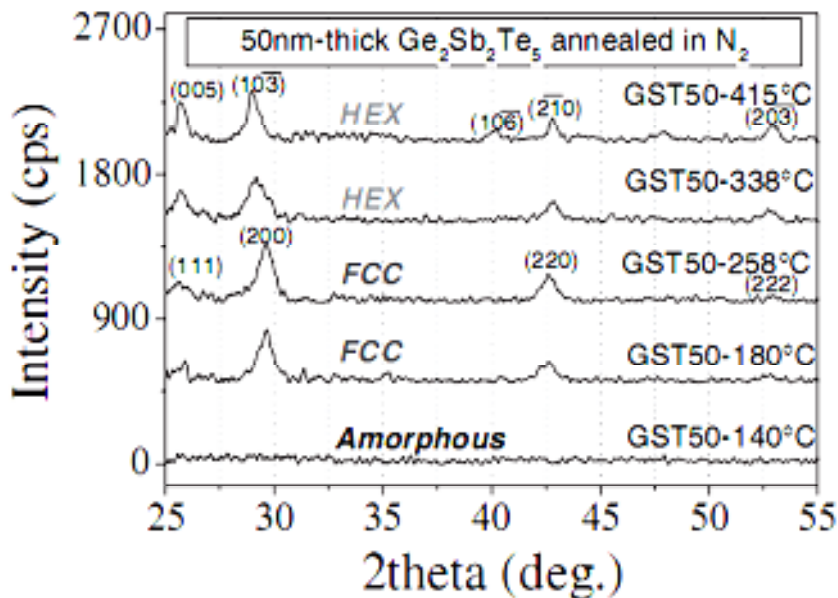4. Also this is the material which is widely used in optical rewritable CD/DVD RW disks.

Fig.2.5 XRD result of GST crystalline structure with an increasing annealing temperature.

It has been reported that the structure of a crystalline GST changed with the anneal temperature [11]. Fig. 2.5 shows a XRD result of the crystalline structure with an

increasing annealing temperature. This experiment was done using a 50 nm thick sputtered GST, anneal in a nitrogen environment. The result shows that, at 180 ℃ and 338 ℃ it turned into a FCC and hexagonal structure respectively. Apart from that, not only the crystalline structure of the GST changed due to increasing annealing temperature, the resistance value of the GST too changed as well. The result is shown in Fig. 2.6. The resistance value of the GST changed for about 5 digits with an increasing annealing temperature. Intermediate resistance level were seen to be obtained from the graph, indicating the possibility of multi-level storage.
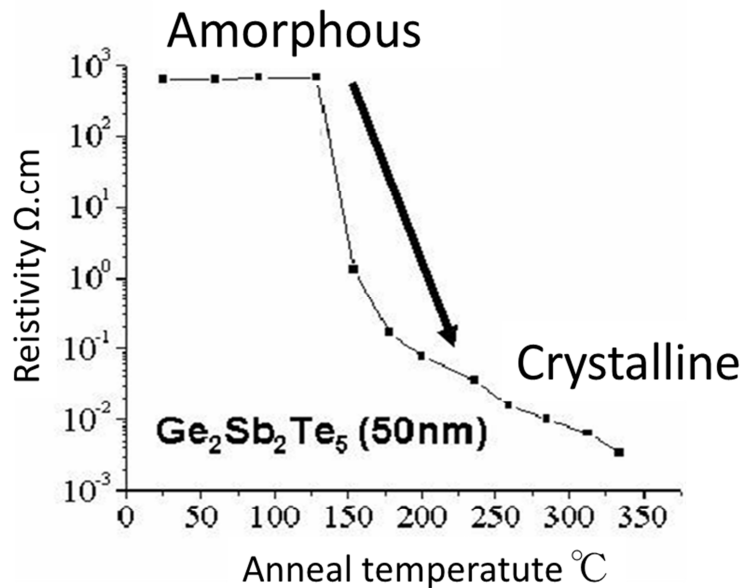

Fig. 2.6 Resistivity of GST due to increasing annealing temperature.

2.3 Phase-change memory cell architectures for multilevel storage

Several memory cell architectures have been investigated to optimize the cell performance, the reproducibility of the device characteristics, and the scalability. A very common vertical PCM cell is shown in Fig. 2.7 that was been proposed by Ovonyx, which is composed of a cylindrical heater above which a thin chalcogenide layer is

deposed [12]. The required programming current and power depend on the electrical and thermal properties of the heater material and the chalcogenide, on the thermal properties of the surrounding materials and on the sizes of the cell. Tungsten was used for the heater and the phase-change material was heated by Joule-heating. This vertical PCM cell has the ability to switch phases for almost 10^{12} times, as shown in Fig. 2.8. However, since the thermal resistance of the tungsten and the phase-change material was high, high current flow was needed for the amorphization process, which was nearly 1 mA. With this disadvantage, researchers are trying to find a way to reduce the current value for the amorphization process.
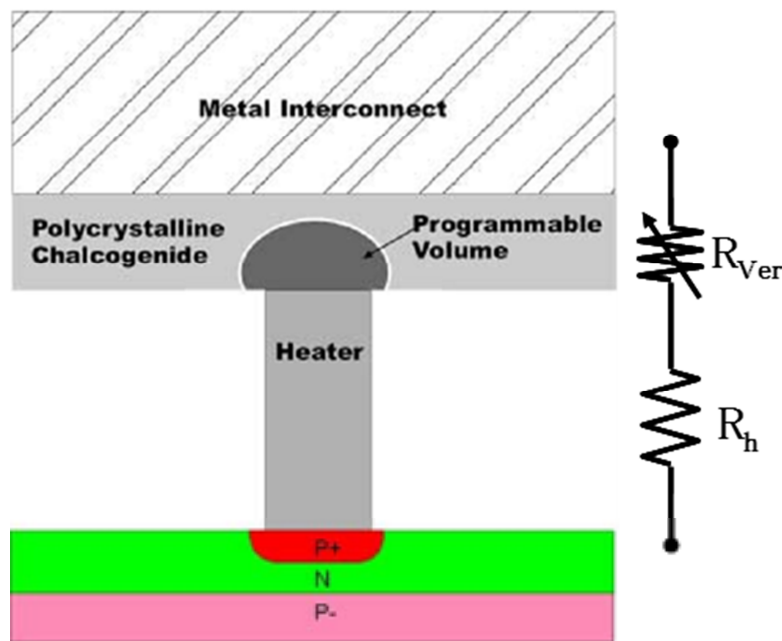

Fig.2.7 Schematic diagram of a common vertical PCM cell.

In our lab, it started by the above cell architectures, the heater element may be considered the main responsible for the chalcogenide heating. However, some cell architectures have been proposed where Joule heating inside the phase change material significantly contributes to the active area heating, thus increasing the thermal

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efficiency of the device and reducing the programming current [13,14].

Fig. 2.9 shows a lateral PCM cell is shown that was been proposed by Phillips Research Laboratories. It has achieved, switching phases of the phase-change material for about 10^6 times. However, this structure has a wide channel, almost 2 μm. This make it not suitable for down scaling of the PCM.
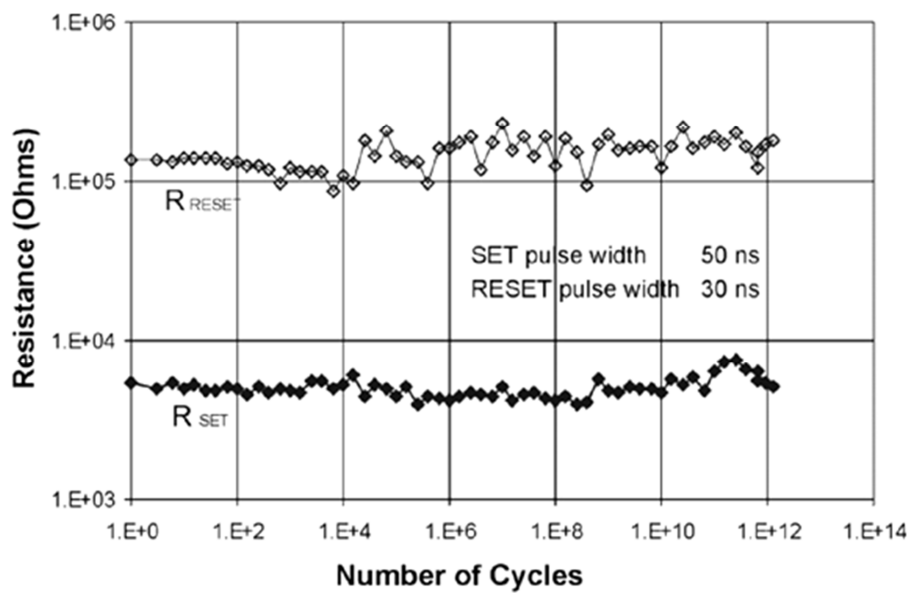

Fig.2.8 Number of cycles changes in a vertical PCM cell by Ovonyx.
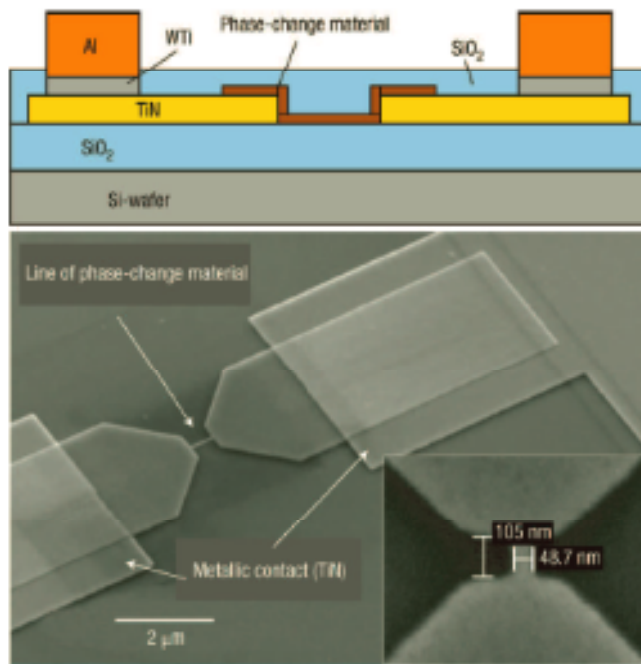
Fig.2.9 SEM picture of the line cell structure realized by Philips Research Laboratories [15].
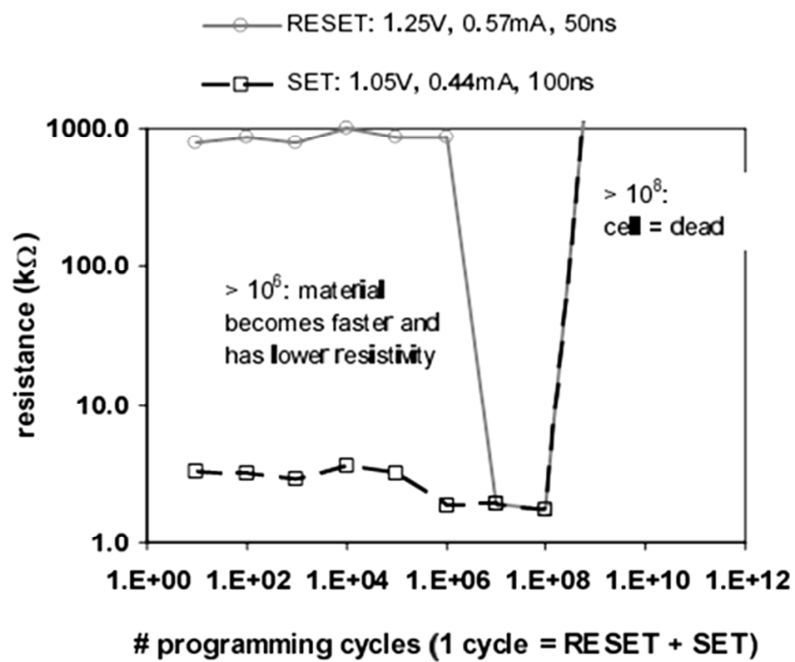

Fig.2.10 Number of cycles changes in a lateral PCM cell by Phillips.

The vertical PCM cell that has been proposed by Ovonyx was likely to have the ability to obtain multi-level storage, shown in Fig.2.11. The heat from the heater layer have been transferred to the phase-change memory layer, allowing amorphization of the cell. From the Fig.2.11 it can be seen that, many intermediate level were achieved, and the switching of phases were obtained for more than 10 times. On the other hand, research on multi-level storage for lateral PCM cell are yet not being done much because of difficulties to control the heat transferred to the phase-change material.
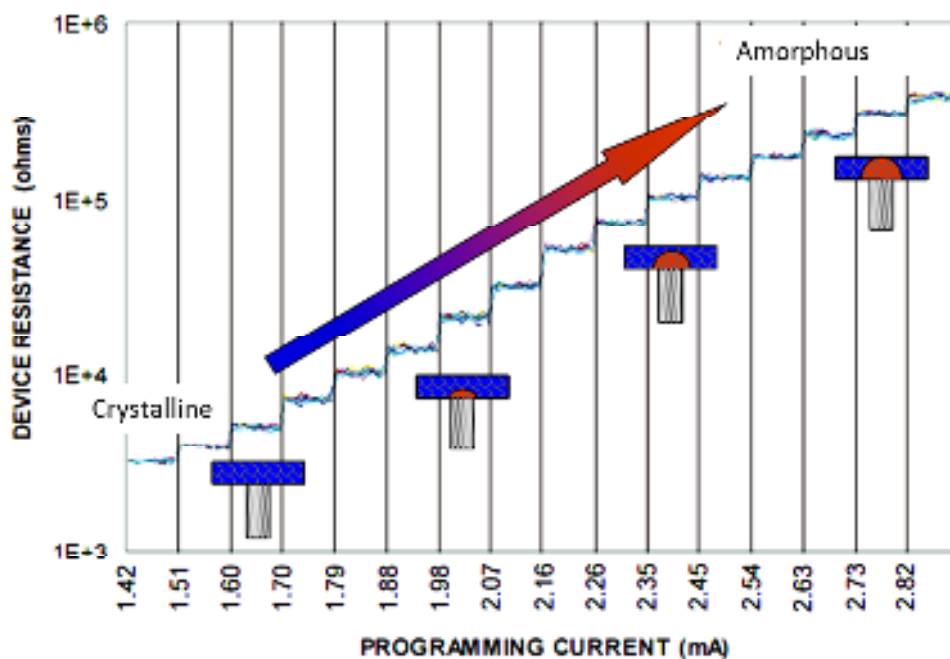

Fig.2.11 Multilevel-storage obtained from the vertical PCM cell.

2.4 Conclusions

From the chapter it can be concluded that the suitable phase-change material for the PCM device is $Ge_2Sb_2Te_5$ (GST). This because GST possess high thermal stability at room temperature. It also has very high crystallization rate that is less than 20 ns and has extremely good reversibility between amorphous and crystalline phases.The structure of the crystalline GST and the resistance value change with the increasing annealing temperature. Intermediate resistance level were obtained, indicating the possibility of multi-level storage.

There are two main structure of the memory cell which are vertical cell and lateral cell. The vertical PCM cell is from Ovonyx, has the ability to switch phases for almost 10^{12} times and possess the possibility for multilevel storage. In other hand, Philips Research Laboratories has come out with lateral PCM cell and achieved switching phases for about 10^6 times.

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Chapter 3 Proposal of separate-heater PCM

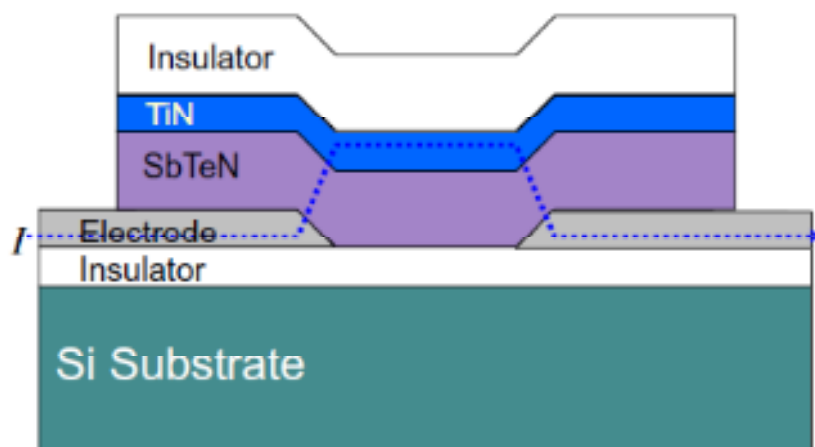## 3.1 Concept of proposed separate-heater PCM

Fig. 3.1 Schematic cross-section of our previous lateral PCM with a top TiN heater layer [1].

So far we have used lateral PCM as shown in Fig. 3.1. Figure 3. 1 shows a schematic cross-section of a lateral PCM with a top TiN heater layer. When a current of higher than its threshold current is induced to the PCM cell, the memory layer of N-doped SbTe (SbTeN) is heated due to Joule-heating of not only self-heating of SbTeN layer directly but also the TiN heater layer indirectly.

Heating mechanism is very complicate because of 2 heating sources. The resistance changes gradually with the increasing programming current pulse with many intermediate resistance levels. 16 levels of resistance changes were achieved in our previous work [1] as shown in Fig. 3. 2. However, the controllability is not good because the self-heating of the SbTeN changes its resistance and heating depends on resistance changed by previous heating.
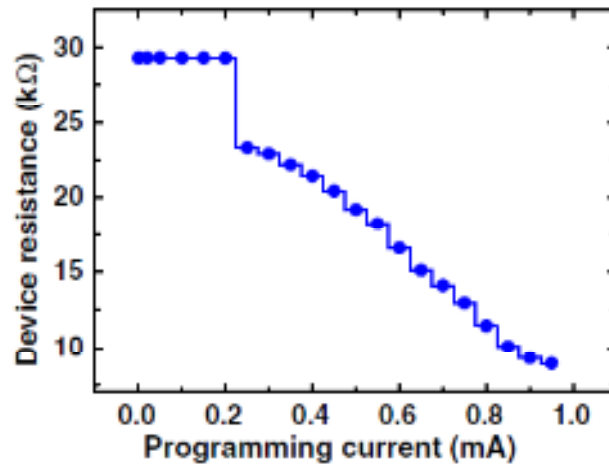
Fig. 3.2 Resistance of the lateral PCM as a function of the programming current I_p in read-out of the resistance at 1 V.

In order to control heating of the PCM precisely, I have proposed new PCM with separate-heater structure. The separate-heater PCM device structure is a little different from our previous PCM device structure explained above as shown in Fig. 3.1. The heater layer is separated from the PCM layer of $Ge_2Sb_2Te_5$ (GST) by an insulator layer of ZnS-SiO_2, which makes the heater layer not connected electrically to the PCM layer (Fig. 3. 3).
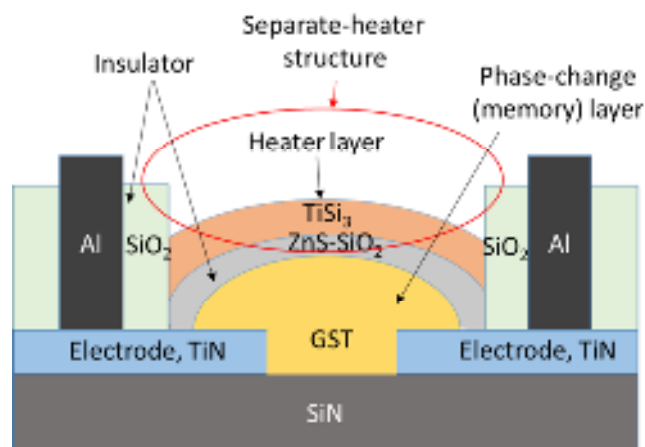

Fig. 3.3 Schematic cross-section of a lateral PCM with a separate-heater structure proposed here.

The device structure is shown in Fig. 3.4 to explain the principle of the separate-heater PCM. The principle is that when a SET voltage pulse is applied to the separate-heater layer characterized by a constant resistance in order to change the PCM from amorphous to crystalline phase, the power ($P = V_{SET}^2 / R_h$) can be well controlled, depending only on the pulse amplitude V_{SET} where the R_a is a resistance of the PCM amorphous phase. Therefore, temperature T_a of the PCM heated by the separate-heater can be well controlled to allow many intermediate resistance levels for multilevel storage. Figure 3.4 shows a schematic circuits diagram of my proposed separate-heater PCM. This device has new 2 electrodes which are connected to SET pulse in SET operation in addition of previous 2 electrodes for read-out of resistance of the PCM. My proposal operation is as following:

1) In SET operation, we use separate-heater indirectly to heat the PCM by applying SET pulse to the separate-heater.

2) In RESET operation, we use direct-heating of the PCM by applying RESET pulse to the PCM (GST memory layer) using the other electrodes.

3) In read-out, we use the PCM electrodes to measure the resistance of the PCM.

The RESET operation is done by using direct-heating because the separate-heater is insufficient to rise the temperature of the PCM up to over the melting point of the PCM or much heating power is needed.
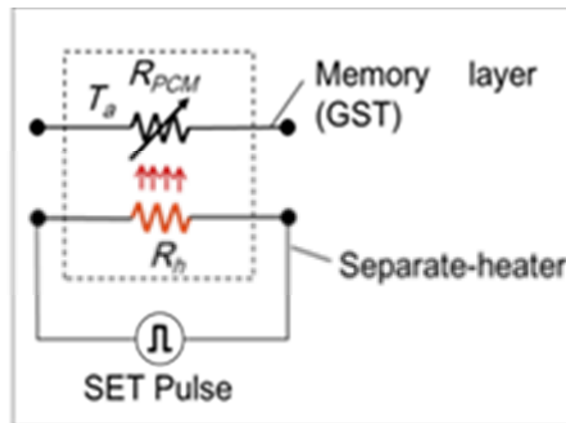
Fig. 3. 4 schematic circuits diagram of a proposed separate-heater PCM.

3.2 Conclusions

Lateral PCM cell with a separate-heater has the potential to achieve many intermediate resistance level through crystallization process. This will enable multilevel storage at low voltage. The power of the heater layer $TiSi_3$ is believed to be stable and can be well controlled. From this, stable heat can be transferred to the GST layer, allowing gradual changes of the GST resistance value for multilevel storage.

Reference

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Chapter 4 COMSOL Simulation for Separate-heater

Phase-change Memory Device

In chapter 4**,** the simulation done in this work will be explained. Simulation was done using the commercially available software COMSOL 3.2. Fig. 5.1 shows the simulation model analyzed in this study. Two types of simulation were done, which are:

1. Simulation to investigate the temperature distribution using different types of capping materials (SiO_2, SiN and ZnS-SiO_2) for a better control of resistance change.

2. Simulation to investigate the resistance change GST (memory) layer.

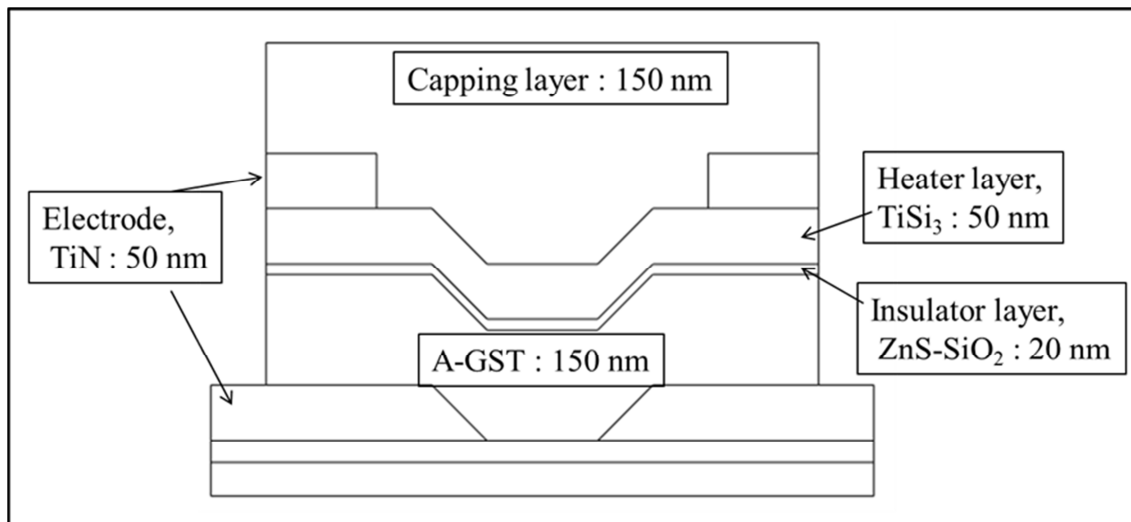## 4.1 Simulation for design of separate-heater PCM

Fig. 4.1 Cross section of the simulation model.

Fig. 4.1 shows the simulation model of the separate-heater PCM device. The separate-heater PCM consists of 4 TiN electrodes, GST, insulator layer for separating

GST from heater, heater layer and capping layer. The GST for PCM is located between 2 TiN electrodes on the SiN and Si substrate, between the electrodes as shown in Fig. 4. 1. The gap is called the channel. The other electrodes on top layer are for supplying the current to the separate-heater.

The channel width and length were 0.8 μm and 0.4 μm, respectively. The thickness of the TiN electrode was 50 nm. The GST memory layer, insulator and heater layer were 150 nm, 20 nm and 50 nm in thickness, respectively. The capping layer was covered over the PCM device to protect from thermal loss emitted from the heater layer to outside.

4.2 Simulation with different capping materials

The materials for the separate heater and the memory layer were TiSi3 and GST with thicknesses of 50 nm and 150 nm, respectively. Between both the layers, 20-nm-thick insulator layer of SiO_2 was inserted so that the layers were not electrically connected to each other. Three kind materials of capping layers with a thickness of 150 nm, such as SiO2, SiN and ZnS-SiO_2, are investigated in this work to prevent from the thermal energy loss. The SET pulse, ranging from 0.5 V to 3 V at 100 ns in a pulse width was applied to the separate heater, and the temperature distribution in the GST layer was investigated. The required thermal and electrical properties of materials used in the simulation are given as Table 4. 1, where A-GST indicates amorphous phase GST.

Table 4.1 Physical properties of materials used in the simulation

Material	Heat Capacity (C) J/(kg*K)	Thermal Conductivity (K) W/(m*K)	Density (ρ) kg/m³	Electrical Conductivity (σ) S/m
SiO_2	1330	1.4	2330	1.0×10^{-14}
SiN	600	25	3180	1.0×10^{-14}
$ZnS-SiO_2$	263	0.657	3650	1.0×10^{-14}
TiN	784	22	5240	5.0×10^{6}
A-GST	202	0.46	6200	3.6×10^{-1}
$TiSi_3$	800	20	4043	1.8×10^{4}

4. 3 Temperature distribution of the PCM

Simulations were done with the materials and their physical parameters described above. As simulation results, the PCM temperature distributions are shown in Fig. 4.2. When 2-V-SET voltage pulse was applied to the separate heater layers, the temperature distributions are typically obtained.

Figs.4.2(a), 4.2(b) and 4.2(c) illustrate the temperature distributions and the heat flux flows of the device in using different materials for the capping layer; SiN, SiO_2 and $ZnS-SiO_2$, respectively. Rising temperature in using the materials can be read out from the level bar on the right side. The heat fluxes are shown as arrows, where the length of arrows relates to the heat flux density and the direction indicates with the heat flux arrow direction.

The maximum temperature of the GST layer for the SiN capping just after applying SET voltage pulse of 2 V is about 460 K, which is slightly higher than the crystallization temperature of GST, 450 K. Crystallization of the GST occurs by applying 2 V pulse with a width of 100 ns. On the other hand, in using SiO_2 and $ZnS-SiO_2$ capping layers, application of 2-V-SET voltage pulse can heat the GST up to

maximum temperature of GST to be about 650 K and 750 K, respectively. It is very clear that the lower the thermal conductivity of the capping layer, the higher the temperature. High temperature is easy for crystallization in the GST layer. The thermal conductivity for each capping material is represented in Table 4. 1. ZnS-SiO$_2$ has the lowest thermal conductivity of 0.657 W/mK, compared with those of SiO$_2$ and SiN.
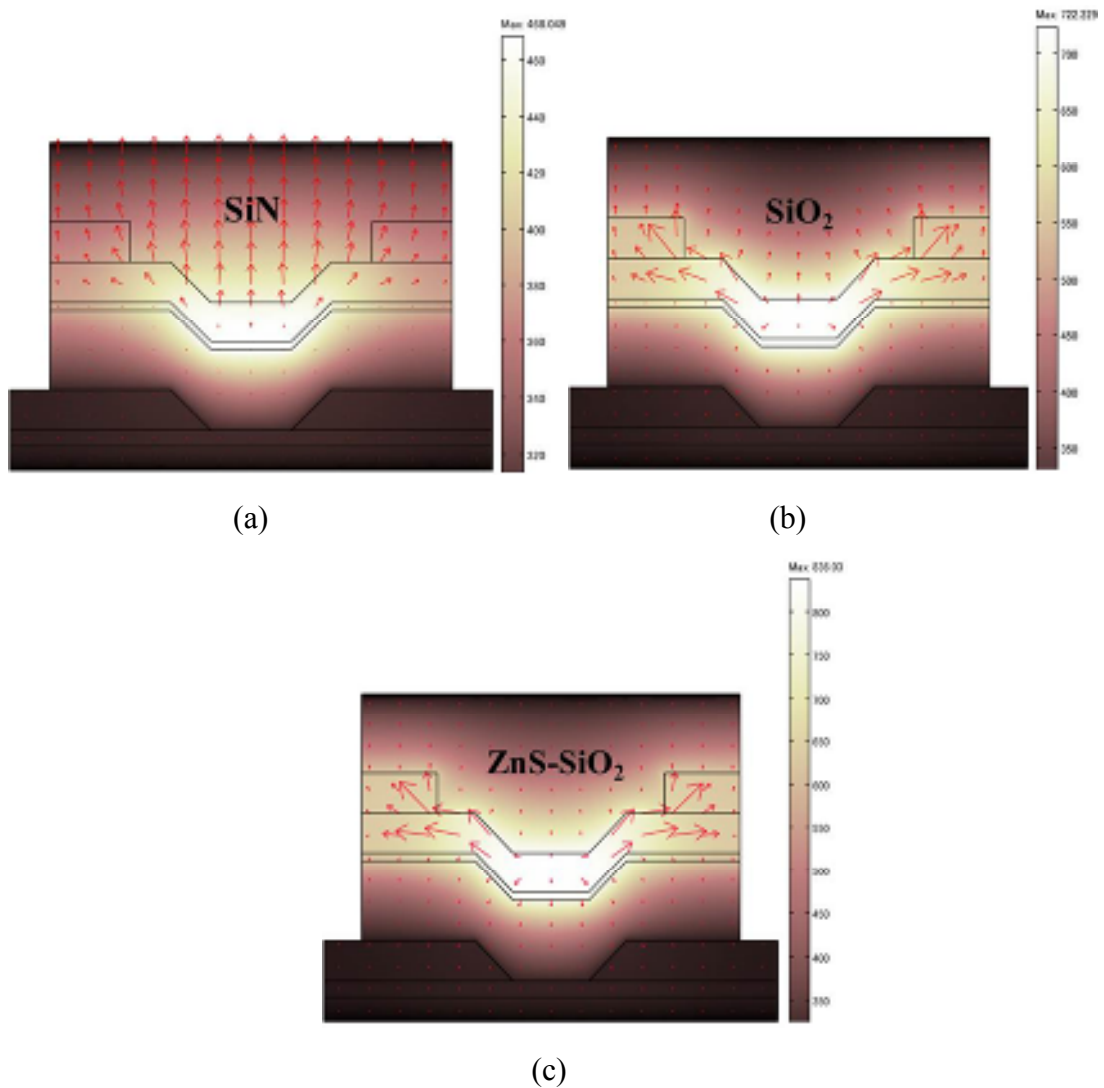

(a)   (b)

(c)

Fig. 4.2. Temperature distribution in the cross section for models with various capping materials at 2 V SET amplitude pulse. (a) SiN, (b) SiO$_2$, (c) ZnS-SiO$_2$

A material with high thermal conductivity tends to dissipate heat greatly. This can be known from the heat flux directions simulated in using the capping layers. SiN has the highest thermal conductivity, 25 W/mK. From Fig. 4. 2(a), we can see that the heat flux directions almost point from the heating layer to the capping layer. It is clear that the heat dissipated easily from the heater to the capping layer and outside without heating the GST layer.

In Fig. 4.2 (c), we can see that the heat flux directions spread all over the places. This shows that the heat from the heater are transferred all over, especially to the GST layer.
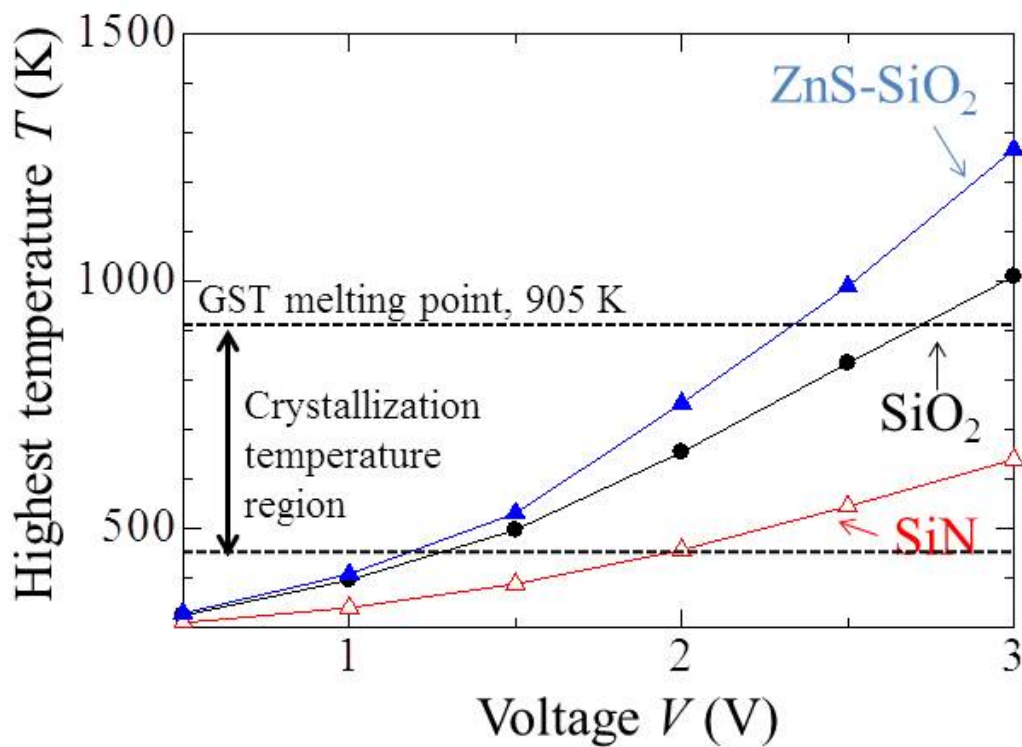

Fig. 4.3 The highest temperature vs. pulse amplitude.

Fig. 4. 3 shows the highest temperature of the GST layer when a SET voltage pulse was applied, ranging from 1 V to 3 V at 100 ns. The crystallization of GST occurs at temperature ranging from 450 K to 905 K. Amorphous GST started to change to

crystalline phase when the SET pulse amplitude was about 1.2 V for the models with a capping layer of SiO_2 or ZnS-SiO_2. Then, when an increasing pulse was applied to the separate heater layer, the temperature of GST increased gradually. This indicates that the crystallization was well controlled by changing the amplitude of the SET pulse.

4.4 Simulation for resistance changes of the GST by applying SET pulse to the separate-heater.

The simulation model is shown in Fig. 4.1. The materials of the separate-heater and the memory layer are $TiSi_3$ and $Ge_2Se_2Te_5$ (GST) with the thicknesses of 50 nm and 150 nm, respectively. An insulating layer ZnS-SiO_2 with thickness of 20 nm is inserted between the two layers and the device is covered by a 150 nm-thick ZnS-SiO_2 as the capping layer from the first simulation results. SET pulse, ranging from 0V to 3V at 100 ns is applied to the separate heater and the temperature distribution in the GST layer and the resistance drop is investigated. The required thermal and electrical properties of materials used in the simulation are given in Table 4.2. The electrical conductivity of ZnS-SiO_2 is an estimated value, which is 1.0×10^{-14} S/m.

Table. 4.2 Physical properties of materials used in the simulation.

Material	Heat Capacity (C) J/(kg*K)	Thermal Conductivity (K) W/(m*K)	Density (ρ) kg/m³	Electrical Conductivity (σ) S/m
ZnS-SiO_2	263	0.657	3650	1.0×10^{-14}
TiN	784	22	5240	5.0×10^6
a-GST	202	0.46	6200	3.6×10^{-1}
c-GST	202	0.46	6200	2.0×10^2
$TiSi_3$	800	20	4043	1.8×10^4

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The simulation results for the device temperature distribution are shown in Fig. 4. 4. The figure shows that when a pulse voltage applied to the separate-heater layer was increased, the temperature in the GST layer increased. When SET voltage pulses of 1.5 V and 2.5 V for 100 ns in a pulse width were applied to the separate-heater, the temperature distributions are obtained, shown in Fig. 4.4 (a) and Fig. 4.4 (b). The temperatures of the device model can be read out from the level bar on the right side. When applying 1.5-V pulse to the heater, the maximum temperature of A-GST layer rises up to about 620 K in a center and top of the GST layer. However, only top layer of the GST was heated so that the temperature rises up to over 450 K. This means that the heating is in sufficient to change the phase from amorphous to crystal. On the other hand, when applying 2.5-V pulse to the heater, the maximum temperature of A-GST layer rises up to about 800 K in a center and top of the GST layer. A region of the GST in temperature range of over 450 K was expanded to 2/3 depth of the GST layer. The 450 K and 800 K indicates the temperature where the phase change from amorphous to crystalline. Consequently, it is clear that almost of the GST layer near the heater changed to crystalline phase. Crystallization occurs due to the efficient heat supplied from the separate-heater. This indicates that the annealing temperature is well controlled by changing the amplitude of applied pulse.
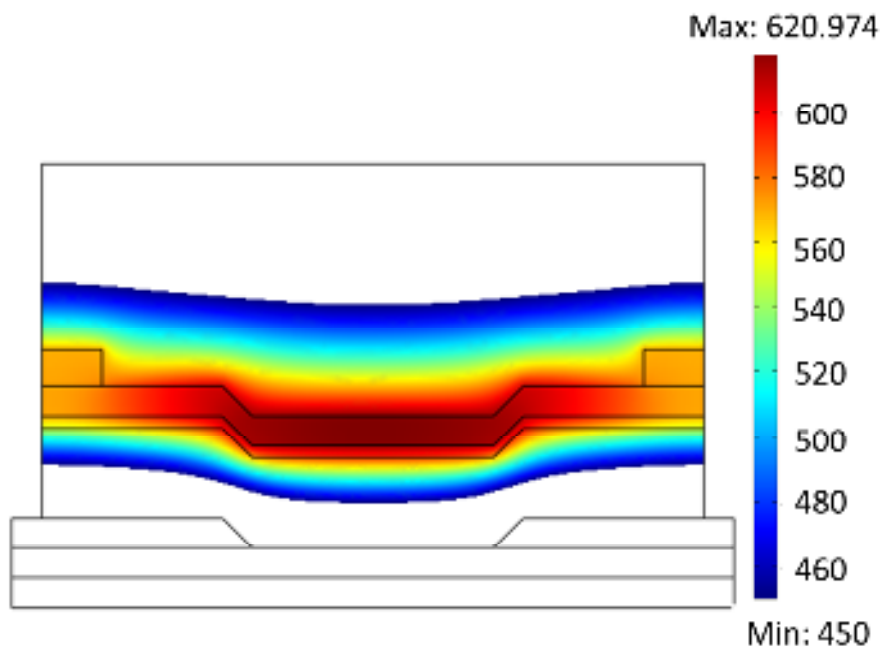
(a)
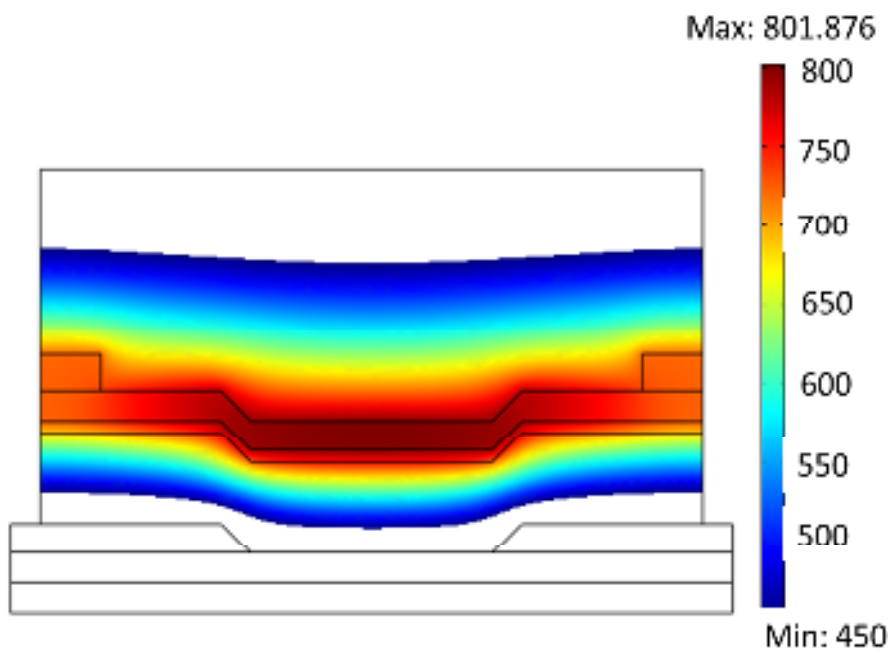
(b)

Fig. 4.4 Temperature distribution in the cross section for models with different SET pulse amplitude. (a) 1.5 V, (b) 2.5 V.

The GST resistance was calculated using the following equation

$$R_{PCM} = \frac{V}{J\,A} \tag{1}$$

where the V is the voltage that was applied to the GST layer, the J is the total current density flowing through the GST layer with a cross area A. Fig. 4. 5 shows that the GST resistance gradually drops down when increasing the SET pulse to be applied to the separate-heater layer. After reaching the crystallization temperature at 1 V, amorphous-GST gradually changes to crystalline-GST and region of changing crystalline phase becomes large, resulting to the resistance drop with the increasing SET pulse amplitude. Above 2.5 V, the resistance becomes almost constant due to saturation of increasing the region. The maximum temperature reaches to 905 K, which corresponds to melting point of GST. It is clear that the applied pulse voltage is less than 2.5 V for crystallization process. It can be concluded that proposed separate-heater PCM structure and materials allow to gradually increase the GST temperature by controlling the SET pulse voltage of ranging from 1 V to 2.5 V, and means that the proposed PCM is suitable to multilevel storage for the memory device in the simulation
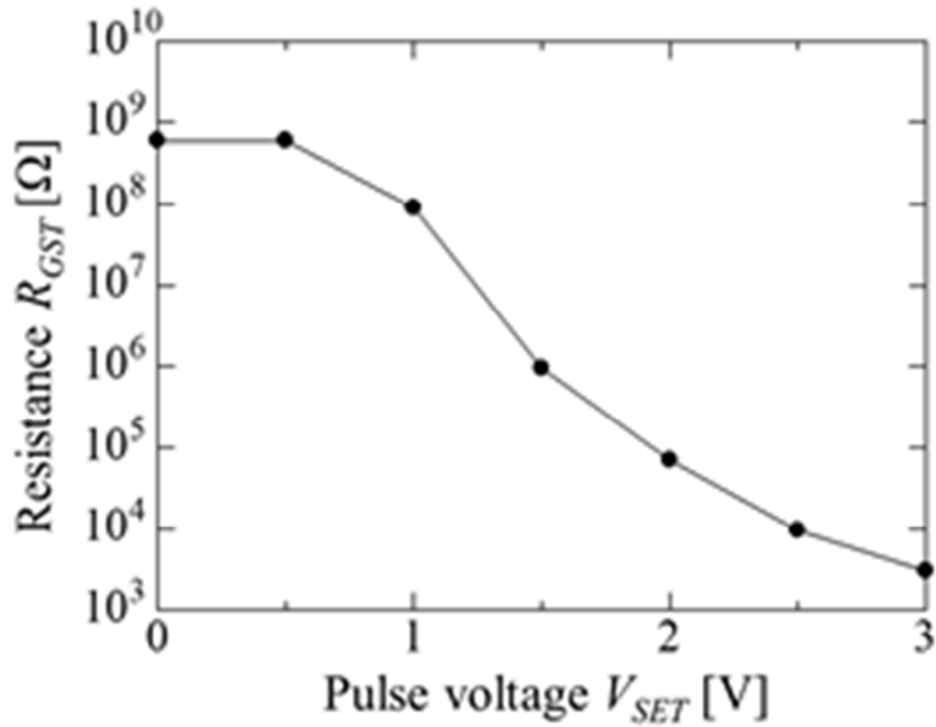
Fig. 4.5 Resistance drop of the memory layer induced by SET pulse voltage at 100 ns (by simulation).

4.5 Conclusions

I simulated the temperature of the proposed PCM and the resistance change of the GST using the PCM structure with the separate-heater and some selected materials of GST, TiSi$_3$ as separate-heater, ZnS-SiO$_2$ as capping layer. As the results, I clarify the following conclusions.

Regarding simulation with different capping materials;

1. The resistance decreased by a factor of 10^5 for the separate heater PCM with ZnS-SiO$_2$ capping layer after application of 2-V-SET pulse.

2. Intermediate resistance value can be easily controlled by simply changing the pulse amplitude from 0.5 to 2V. This enables the possibility to achieve multilevel storage for the separate-heater PCM.

    Regarding simulation for resistance changes in the GST layer;

3. The resistance of the GST gradually decreased by a factor of 10^3 after applying 2.5-V-SET pulse

4. Intermediate resistance can be easily controlled by simply changing the pulse amplitude from 1.0 V to 2.5 V. This enables the possibility to achieve multilevel storage faithfully with the proposed separate-heater PCM.

Chapter 5 Prototype of the Separate-heater PCM

In this chapter, I studied on the fabrication work that was done for this project. First, I explain how a separate-heater PCM device was fabricated. It required 3 steps of processes which were the wet etching, the sputtering and the lift-off. These 3 processes are very essential in order to fabricate a high quality PCM device.

There were several problems that occurred during all these processes. However, I managed to overcome them, and they will be discussed in detail in this chapter.

5.1 Fabrication

A basic and substrate part of the proposed PCM device was fabricated by a production company, although the patent is hold by Hosaka Laboratory. The device element was fabricated on a 200-nm-thick SiN layer on Si substrate. On top of the SiN layer, 2 electrodes were fabricated with 50-nm-thick TiN for measurement of the GST resistance and RESET process. Then, PTEOS deposition of 350-nm-thick SiO_2 was done, followed by Al wiring using 500-nm-thick Al layer sputtering and lift-off technique. Contact holes (CH) photoresist patterning was done to make the contact holes, and Al layer was deposited on top of the photoresist and lift-off process was done to make punch-through electrodes and pad electrodes for supplying the current and voltage to the GST. Finally, the channel patterning for the GST, the insulator, and the separate-heater was done in photoresist layer, by lift-off technique. Until here, these processes were done by the production company.

In our lab, it started by wet etching of the SiO_2 layer using a solution of HF/NH$_4$F. This will etched the middle part of the substrate to form a channel using the photoresist pattern as described above (see scheme in Fig. 5. 1). The optimum time of the wet

etching process will be discussed in section 5. 2. When a channel was formed on parts on the 50-nm-thick TiN electrodes and a gap between the electrodes, some sputtering processes were done. The sputtering was used with RF sputtering machine model MNS-3000-RF made by ULVAC Co. For the separate-heater PCM device, first 150-nm-thick GST was sputtered as the memory layer. Then, a 20-nm-thick $ZnS-SiO_2$ was sputtered followed by 50- nm-thick $TiSi_3$. The $ZnS-SiO_2$ layer works as an insulator layer to separate the memory layer from the separate-heater, and prevent from electrically connecting of the heater layer $TiSi_3$ and the GST layer. These processes are shown in the 3rd illustration in Fig. 5. 1, where the GST, insulator and the separate-heater were formed. This sputtering process will be discussed more in next section.

The last process simultaneously fabricated the memory and the separate-heater using lift-off technique. This lift-off was done by cleaning the sample in a PGMEA solution together with ultrasonic vibration. In this process, the CH-patterned photoresist was stripped from the sample, leaving the Al electrode expose. Details of lift-off process will be discussed later. The flow chart of all three process is shown in Fig. 5. 1
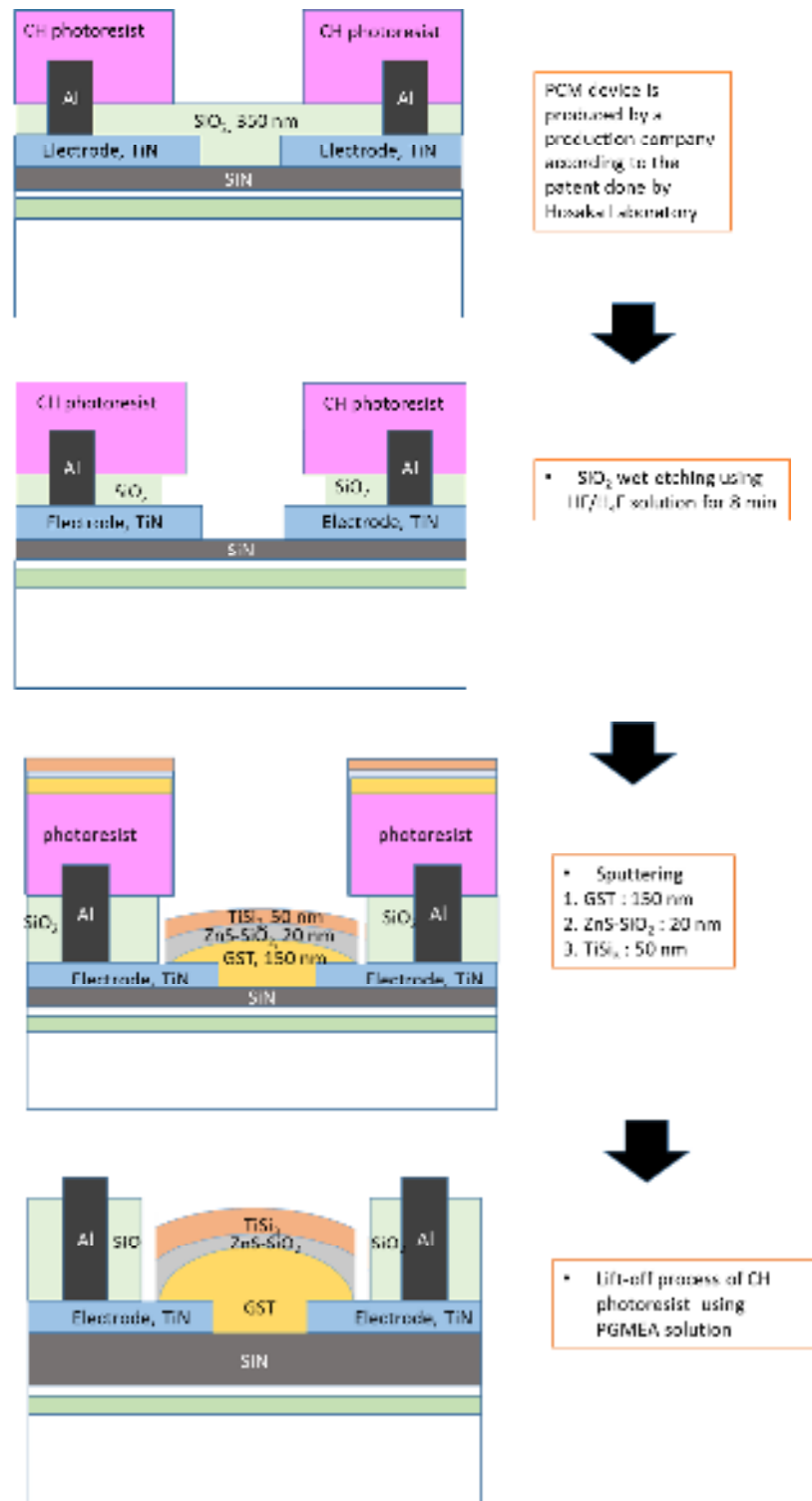
Fig. 5.1 Flow chart of a separate-heater PCM device fabrication process.
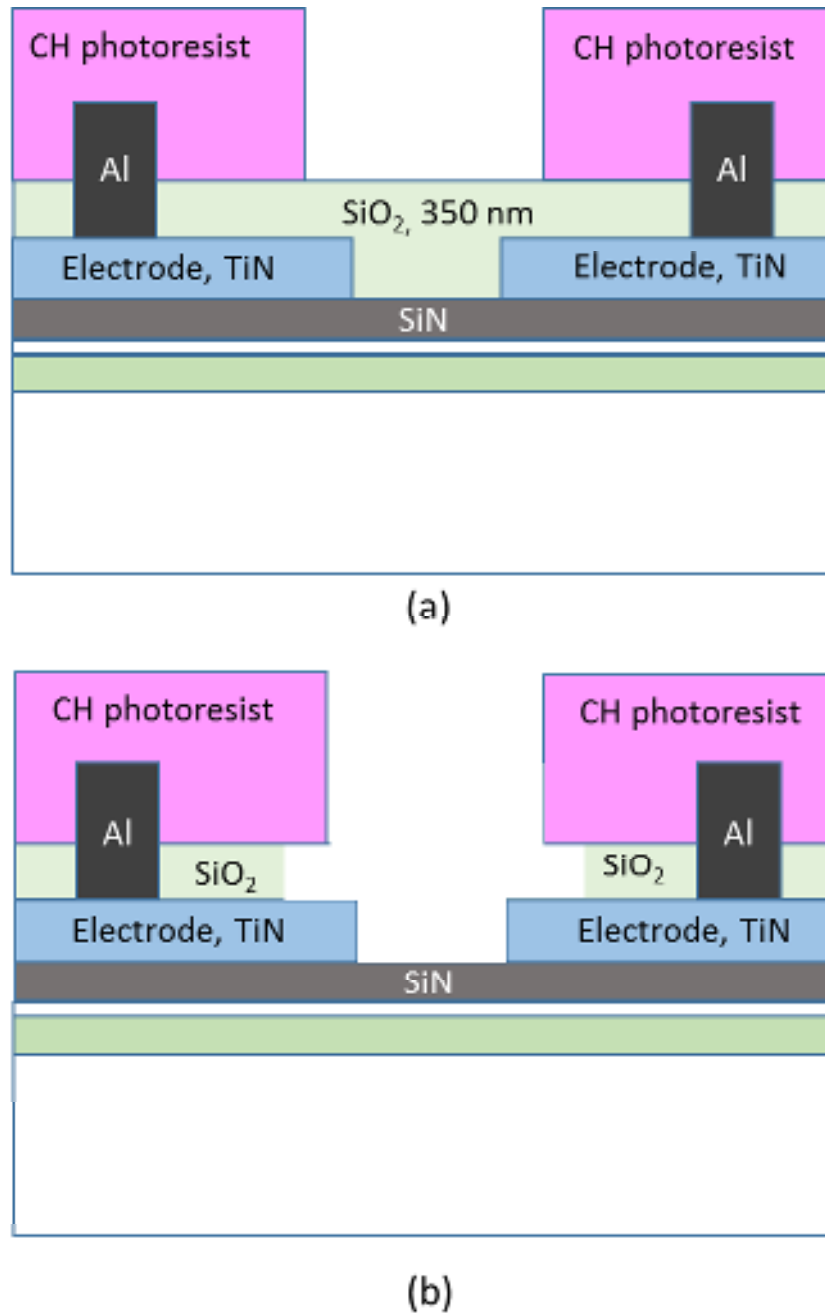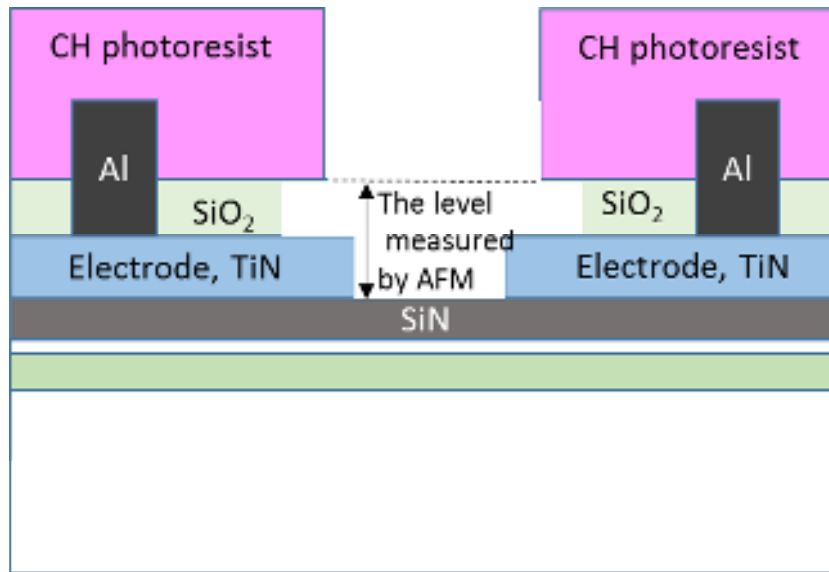
5.1.1 Wet etching process

Fig. 5.2 Schematic diagrams for the wet etching process (a) before wet etching (b) after wet etching.

The wet etching process is one of the important processes for the fabrication of the separate-heater PCM, other than the sputtering process and the lift-off process. The schematic diagram of the PCM substrate before and after the wet etching process is shown in Fig. 5.2 (a) and (b). This process is very essential to form a pattern for the memory and the separate-heater in the SiO_2 layer on the electrodes and the gap (channel) between the TiN electrodes. The channel was formed to enable sputtering process of the phase-change material GST between the TiN electrodes. In order to etch the SiO_2 to form the channel, HF/NH_4F solution was used in this process.

In this experiment, the PCM device was wet-etched for various durations such as 0, 4, 7, 8 and 10 min. The thickness of the SiO_2 layer between the TiN electrodes was measured by atomic force microscope (AFM), after the wet etching process. The wet etching property is shown in Fig. 6. 2. The thickness of the SiO_2 layer to be made with PTEOS was 350 nm. The remained SiO_2 thickness decreased to 68.9, 12.1 nm and 4.2 nm after etching for 4, 7 and 10 min, respectively, as shown in Fig. 5.4. This indicates that the SiO_2 layer was completely etched after 8-min-wet etching process because the depth of etched SiO_2 was saturated. In other words, it can be concluded that the optimized time for wet etching process was 8 min based on AFM measurement.

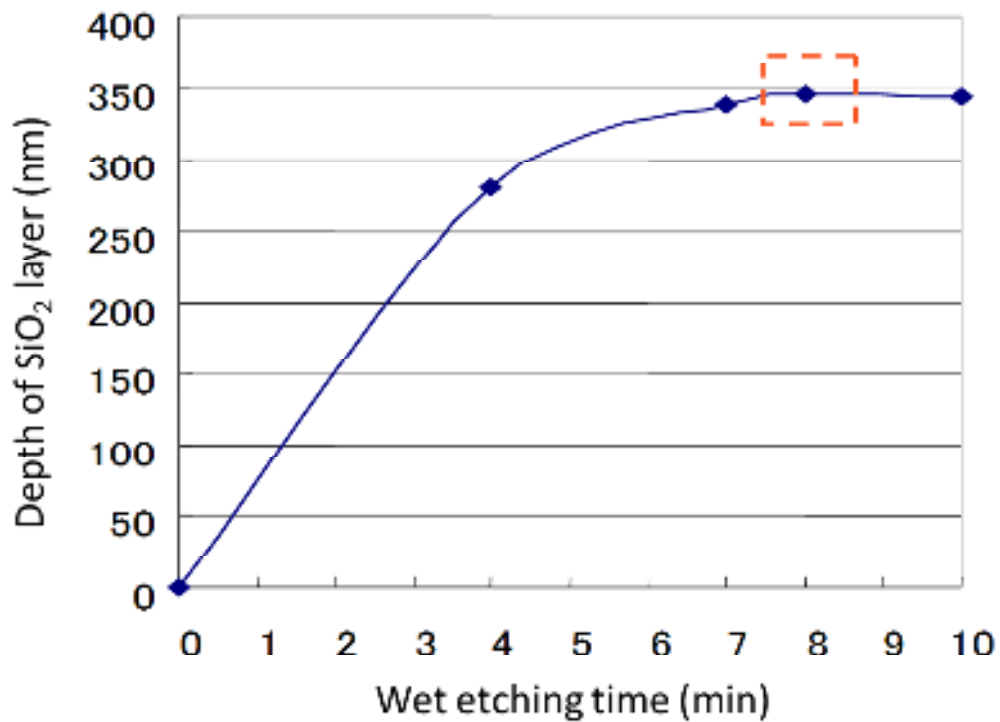5.3 The thickness of the SiO$_2$ measured by AFM during the wet etching process.

Fig. 5.4 The etched depth of the SiO$_2$ layer between the TiN electrodes at different times of wet etching process.

5.1.2 Sputtering process

After the wet-etching process, the memory layer GST, insulator layer ZnS-SiO$_2$ and lastly the heater layer TiSi$_3$ were deposited using the sputtering method.

Prior to the sputtering deposition, the sample undergo a reverse-sputtering process (etching) for 15 min to remove the oxidized or contaminated surface of the TiN electrodes. Next, the sample was moved into the sputtering deposition chamber and then GST, ZnS-SiO$_2$ and TiSi$_3$ were deposited layer by layer using radio-frequency (RF) sputtering equipment (MNS-3000-RF, ULVAC Co.) at 150, 20 and 50 nm in thickness, respectively. The background pressure of the sputtering deposition chamber was below 5×10^{-5} Pa, a sputtering pressure was 0.2 Pa and the RF power was 100 W.
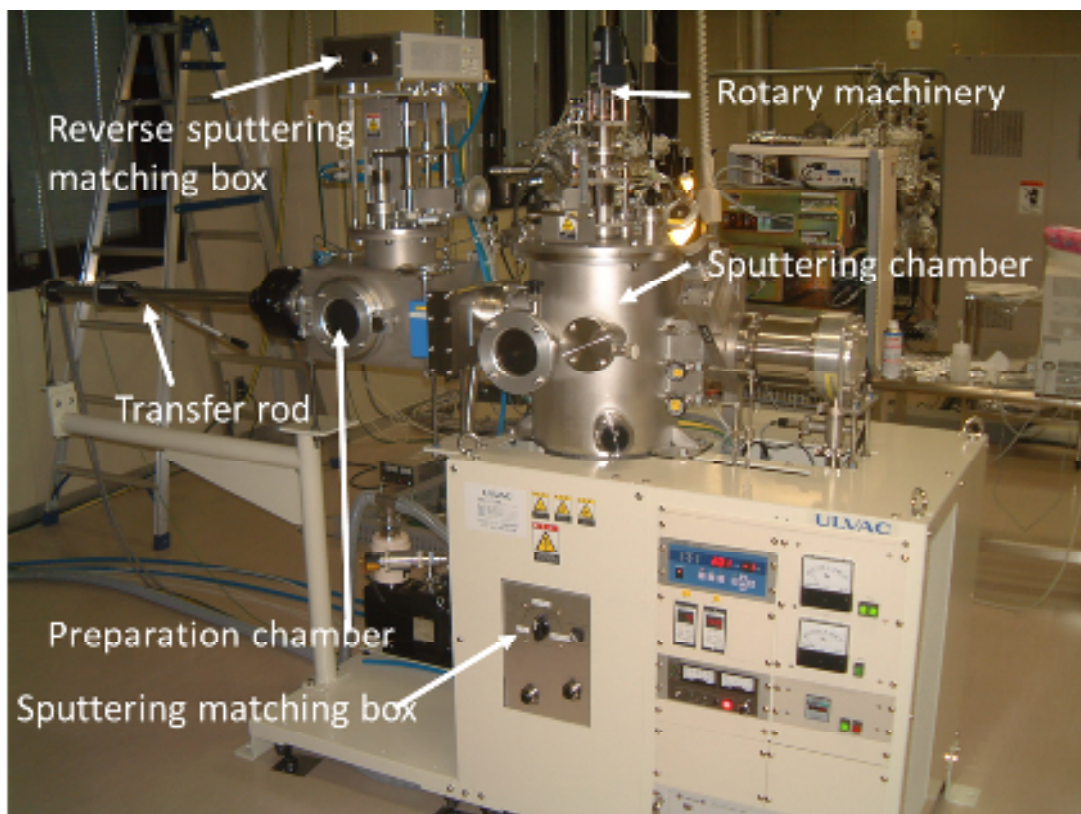

Fig. 5.5 MNS-3000-RF ULVAC sputtering machine.

Fig. 5.5 shows the sputtering machine that was used for the deposition process. The maximum RF (13.56 MHz) output of this sputtering machine is 200 W. It has two main chambers, which are the preparation chamber and the deposition chamber. The deposition chamber is kept in a high vacuum for short turn-around time, evacuating by the turbo molecular pump.
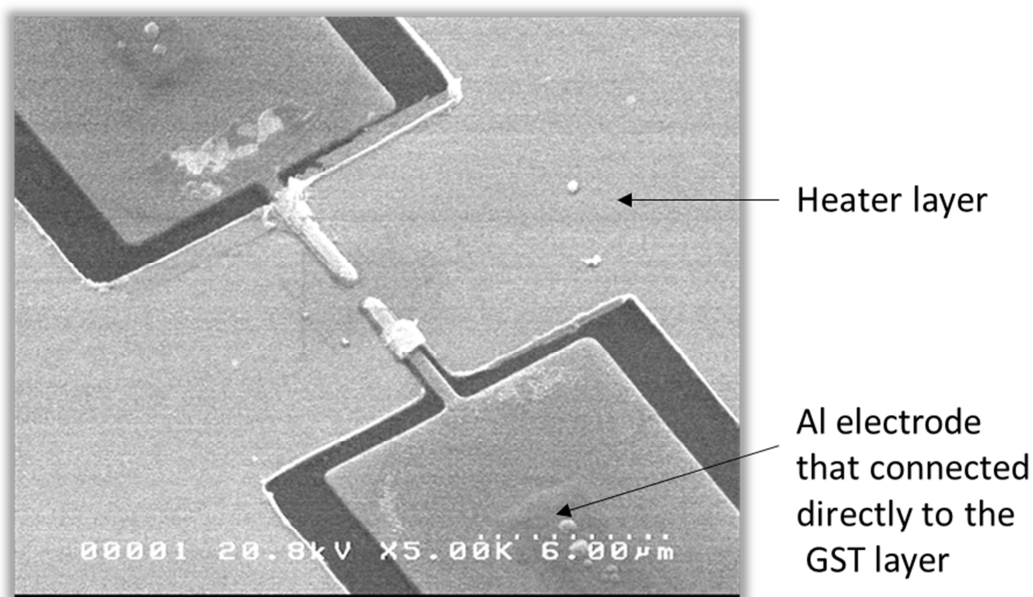

Fig. 5.6 SEM image of a separate-heater PCM device after being sputtered.

Fig. 5.6 shows the SEM image of a separate-heater PCM after being sputtered. The 3 layers of GST, ZnS-SiO$_2$ and TiSi$_3$ were formed as shown in the schematic diagram in Fig. 5. 7, which is essential separate-heater PCM device. As we can see, the heater layer, TiSi$_3$ was sputtered on the insulator ZnS-SiO$_2$. Then, it was surrounded with SiO$_2$ at the left and right sides, for not allowing it to be electrically connected to the memory layer, GST. The heat generated from the heater conducts to the GST by passing it through the insulator ZnS-SiO$_2$. This can control the crystallization process of the GST, allowing intermediate resistance levels for multilevel storage in the PCM device.

The separate-heater PCM structure is schematically illustrated in Fig. 5.7 and the images taken using an optical microscope are shown in Fig. 5. 8 after lift-off process for the separate-heater PCM structure.
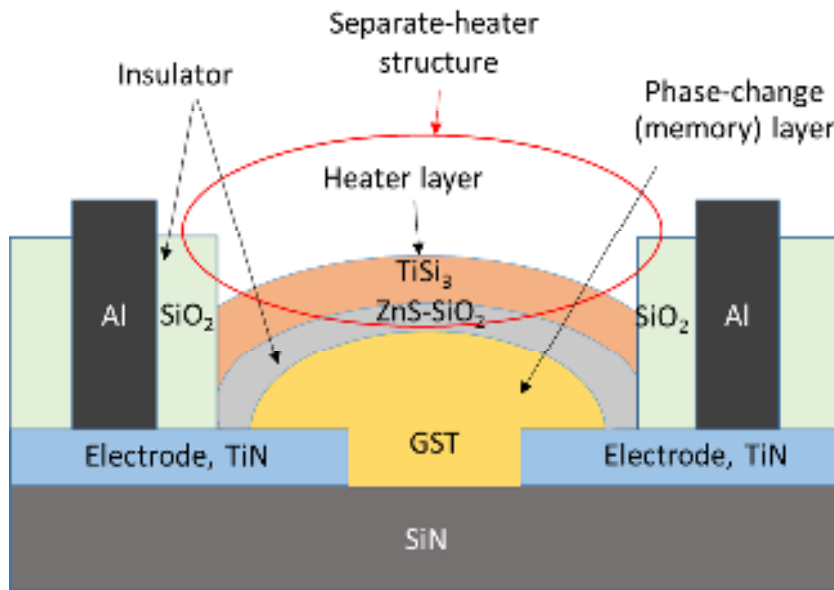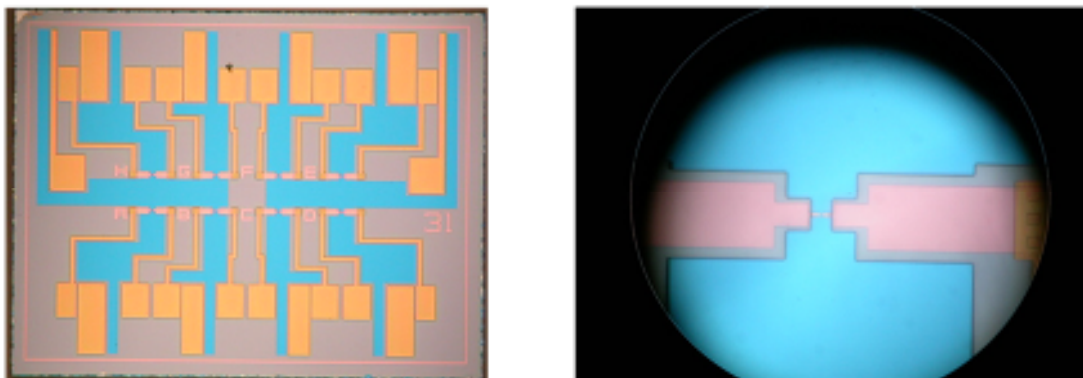

Fig. 5.7 Schematic diagram of a separate-heater PCM.

Fig. 5.8 Optical microscope images of a separate-heater PCM device.

5.1.3 Lift-off process

The lift-off is the last process that is needed in the PCM device fabrication. As same as the wet-etching process, we need to know the optimum condition for this process to allow the resist-layer to peel off cleanly without damaging the memory, the insulator and the heater layer between the electrodes.

After undergoing the sputtering process, the sample was soaked in a PGMEA solution inside a beaker for several minutes for the lift-off process. In order to get the optimum time, some condition was set. It was divided into two conditions. The flow chart of this process is shown in Fig. 5.9.

1. Soaked in a PGMEA solution for several different minutes.

2. Cleaned using an ultrasonic buffer in a PGMEA solution for several different minutes.

For the first condition the substrate was soaked in the PGMEA solution for 1, 2, 4 and 5 minutes. On the other hand, for the second condition the device was cleaned using the ultrasonic vibration in a PGMEA solution for 1, 2, 4 and 5 minute.

Then, the sample was observed by an optical microscope and images were taken to check whether the resist layer was peeled-off cleanly. Finally, an *I-V* measurement was done to double-check the existence of the memory layer, GST and the heater layer, $TiSi_3$.Fig. 5.10 shows optical images after lift-off process for lift-off time. The sample was soaked in a PGMEA solution for 1, 2, 4 and 5 minute without the vibration. From the Fig. 5.10, it shows that the resist layer surface started to become loose after 1 min being soaked in the PGMEA solution. It started to peel the resist layer off for 2 min, and after 5 min it had peeled-off cleanly from the sample surface, as shown in Figs. 6.10(b) and 6.10(d), respectively.
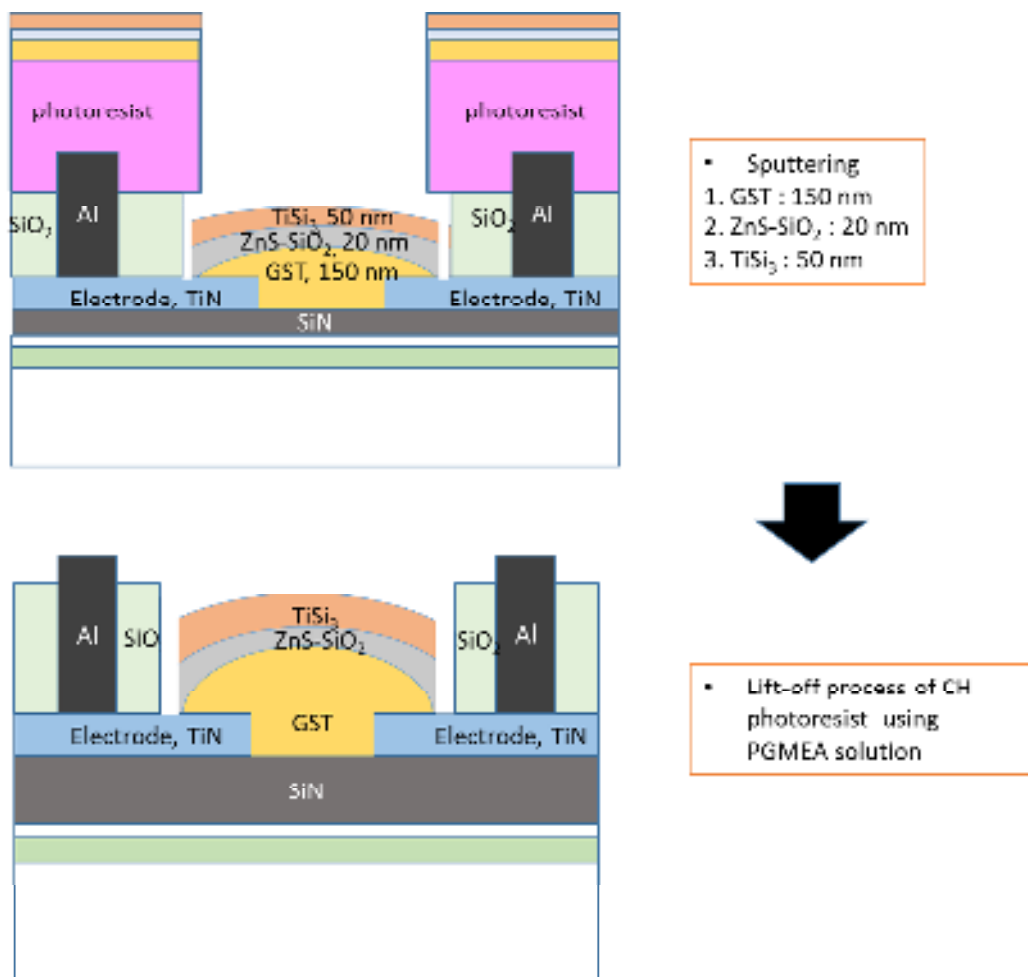
Fig. 5.9 Flow chart of the lift-off process for the separate-heater PCM device.

Figs. 5.11 and 5.12 show the I-V measurement of GST and TiSi$_3$ layer after 4 min of lift-off process. For the GST layer, the resistance was 52.1 MΩ, indicating that although the GST layer existed between the electrodes, the layer was not still connected to both TiN electrodes. On the other hand, in a case of the heater layer, the I-V measurement could not be measured. The graph turned out not to be a linear graph. This can be speculated that the heater layer was cut off during the lift-off process. Figs. 5.13 and 5.14 show the I-V measurement of GST and TiSi$_3$ layer after 5 min of lift-off process.

For the GST layer, the resistance was 5.63 GΩ, showing that the GST layer was not still connected to the TiN electrodes. Unfortunately, for the TiSi$_3$, the I-V graph means that the heater was not connected to the electrodes, as same as in Fig. 5.12 for 4 min in lift-off process. From these results, it can be concluded that soaking of the sample in the PGMEA was not a good method.
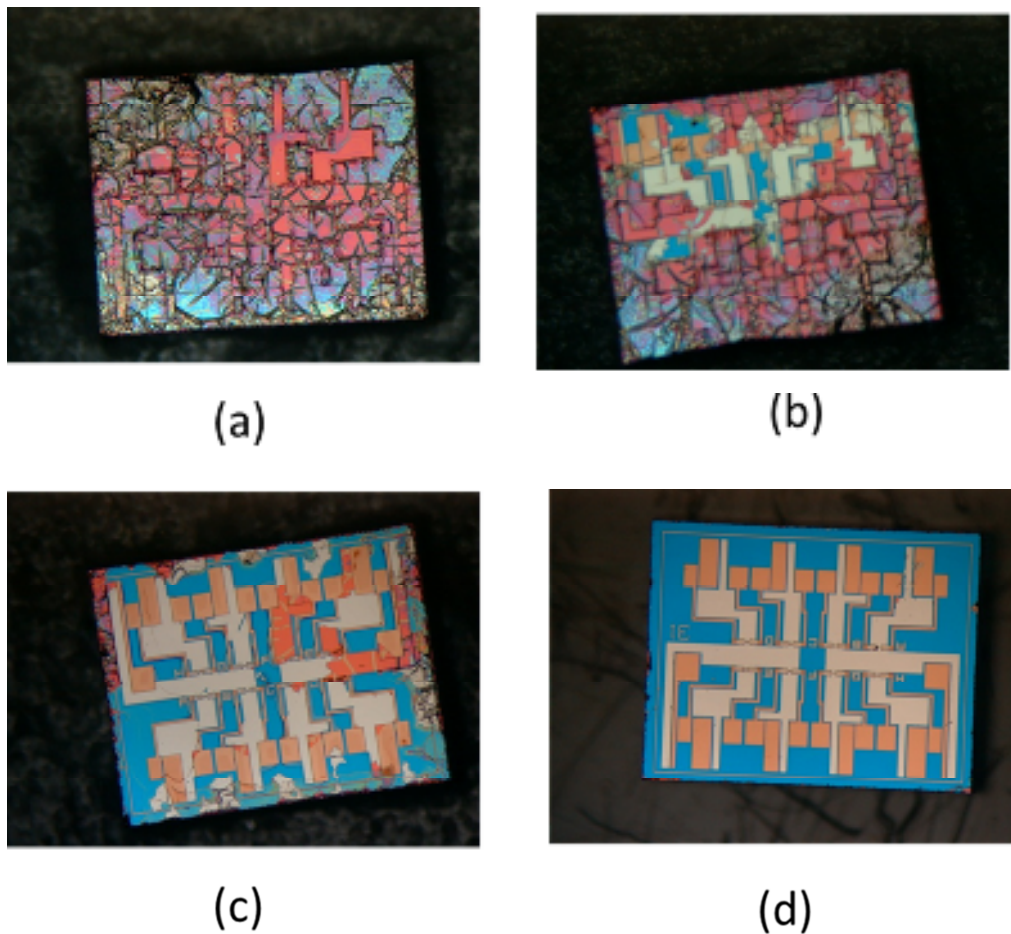

Fig. 5.10 Optical microscope images of a separate-heater PCM device at different time of lift-off process (a) 1 min (b) 2 min (c) 4 min (d) 5 min.
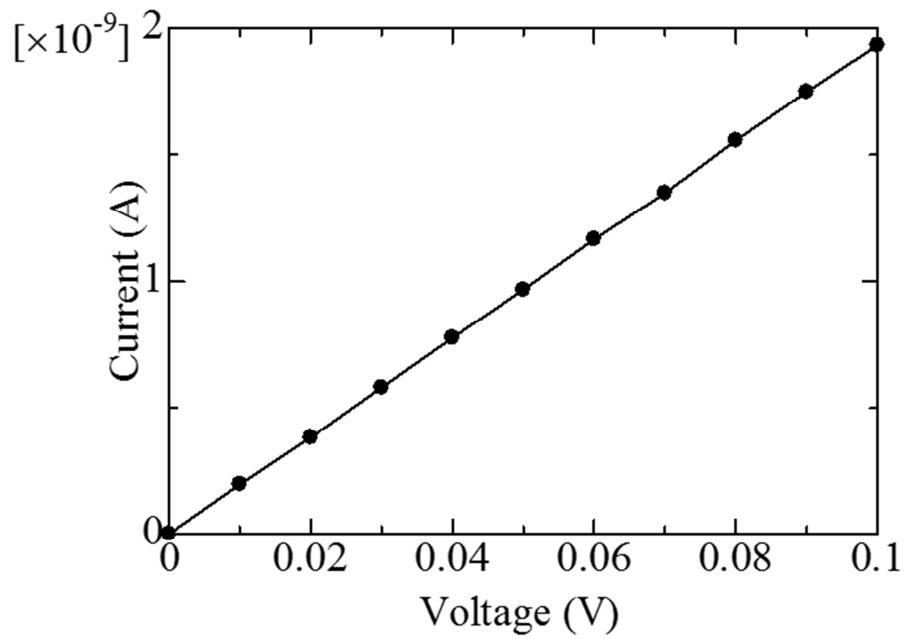
Fig. 5.11 I-V measurement of GST for separate-heater PCM device after 4 min of lift off process.
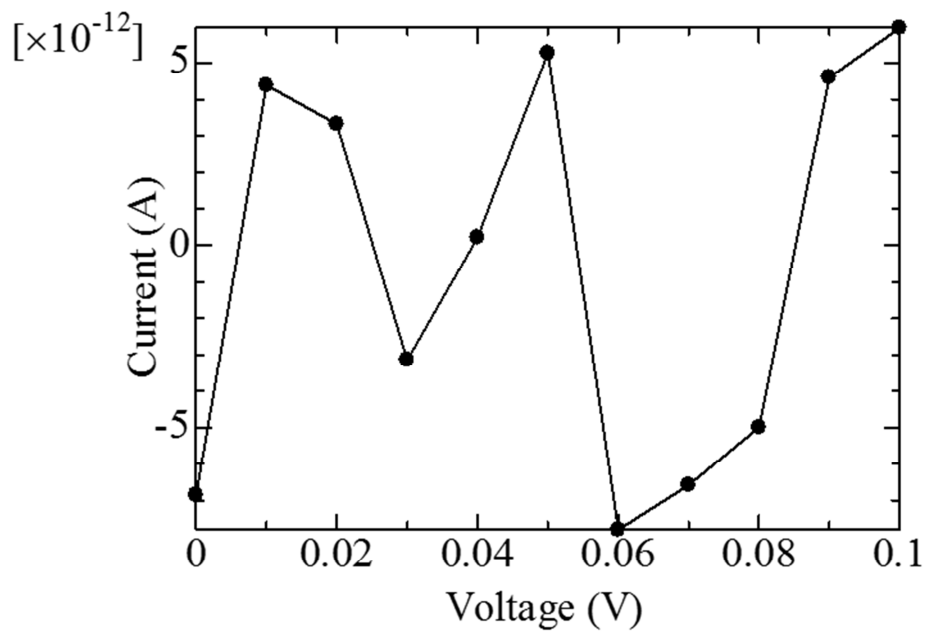

Fig. 5.12 I-V measurement of TiSi$_3$ for separate-heater PCM device after 4 min of lift off process.
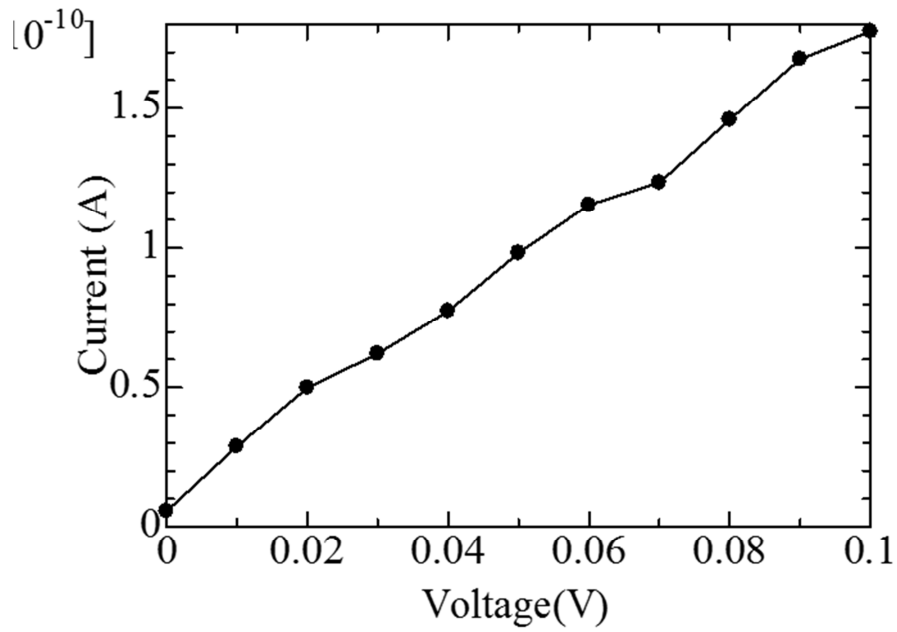
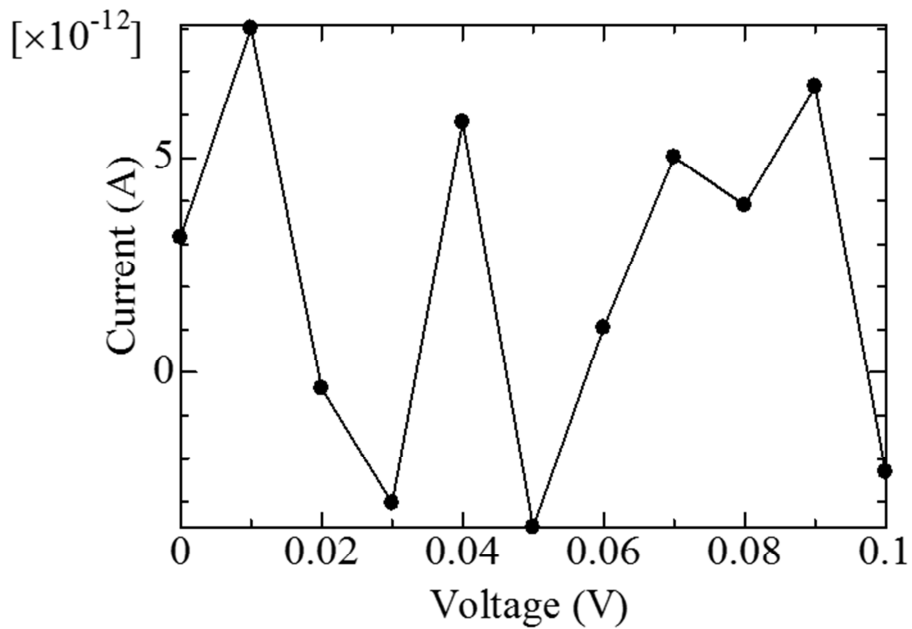Fig. 5.13 I-V measurement of GST for separate-heater PCM device after 5 min of lift off process.

Fig. 5.14 I-V measurement of $TiSi_3$ for separate-heater PCM device after 5 min of lift off process.

Next, I studied the second lift-off condition, which were cleaning the sample in PGMEA solution using an ultrasonic vibration. Fig. 5.15 shows optical images for the second condition. The sample was lift-off in a PGMEA solution using an ultrasonic vibration for 1, 2, 4 and 5 minute. From the figure, it shows that the resist layer surface started to peel off after 2 min time, and after 5 min, it had peeled the resist layer off cleanly from the sample surface, as shown in Figs. 5. 15(b) and 5. 15(d), respectively. The I-V measurement was done to check the existence of the 3 layers that was sputtered on the substrate.
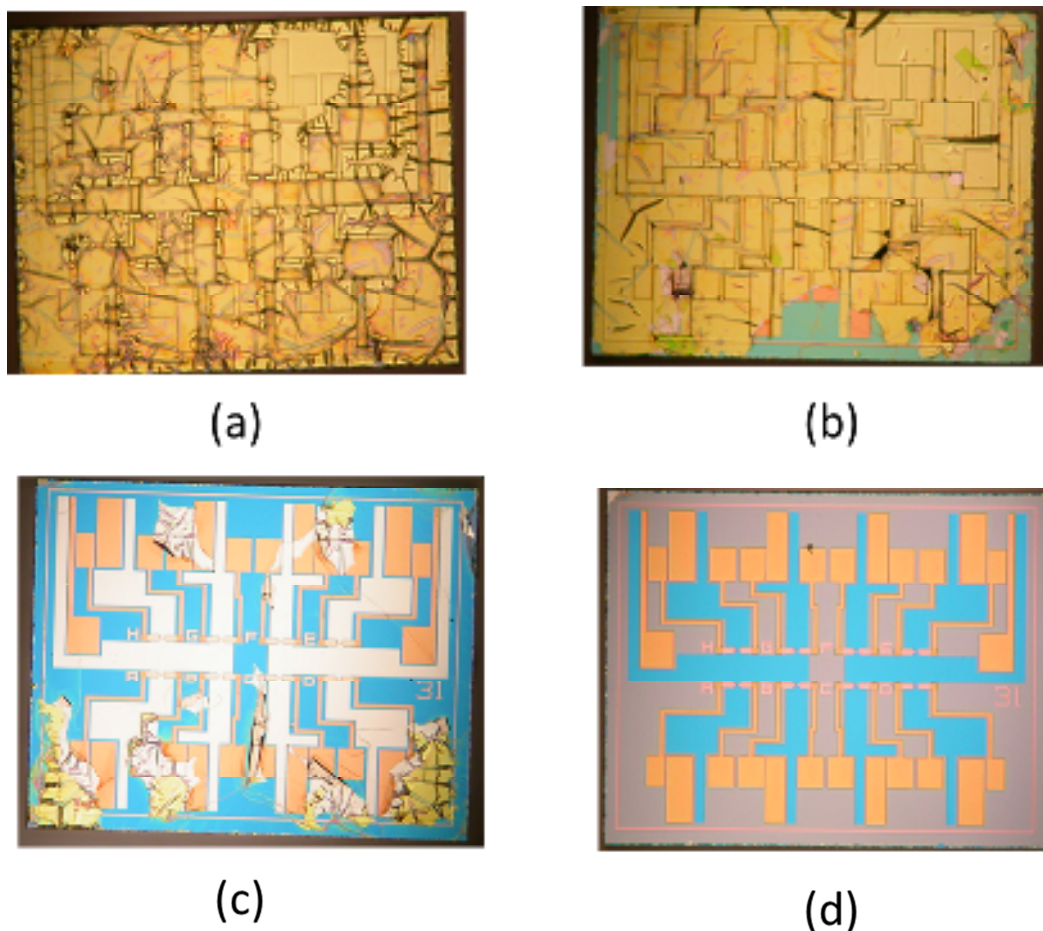

Fig. 5.15 Optical microscope images of a separate-heater PCM device at different time of lift-off process. (a) 1 min (b) 2 min (c) 4 min (d) 5 min
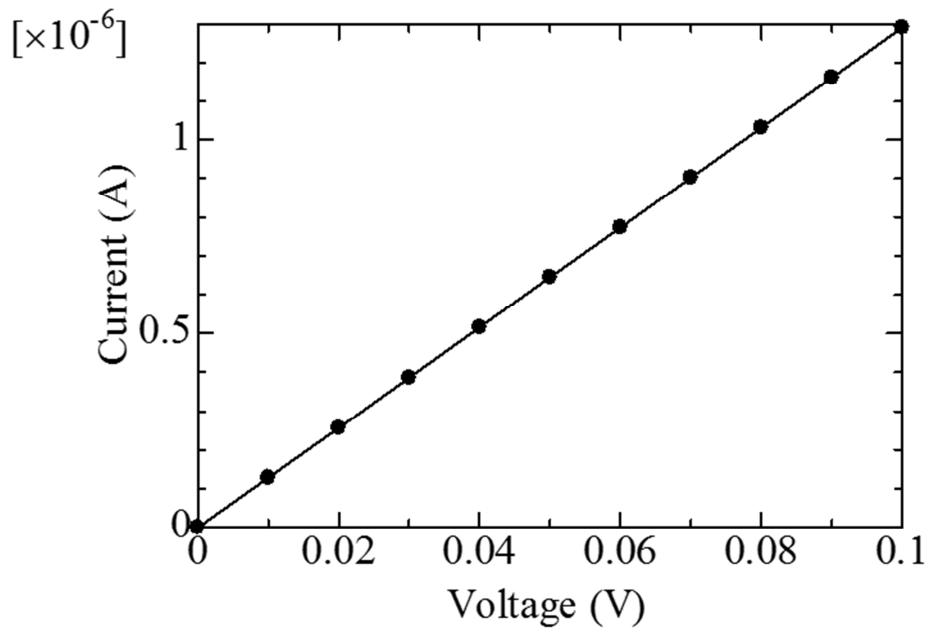
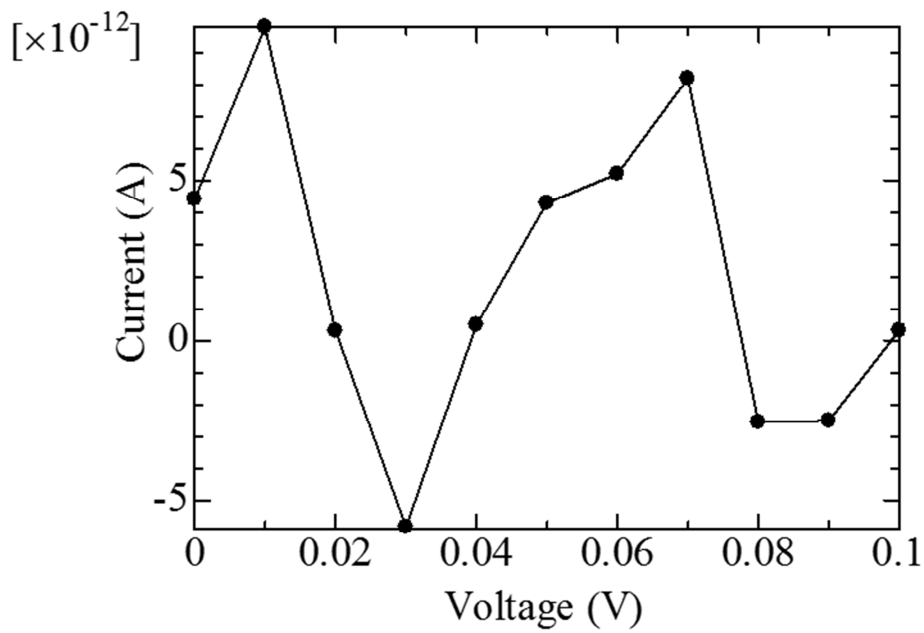Fig. 5.16 I-V measurement of GST for separate-heater PCM device after 4 min of lift off process.

Fig. 5.17 I-V measurement of TiSi$_3$ for separate-heater PCM device after 4 min of lift off process.

Fig. 5.16 and Fig. 5. 17 show the I-V measurements of GST and TiSi$_3$ layers after 4 min of lift-off process using an ultrasonic vibration. For the GST layer, the resistance was 71 kΩ, which was a little bit lower than the resistance that have been calculated in chapter 6.

For the TiSi$_3$, the I-V graph was almost zero not to be linear, as same as in Fig. 5. 11 for 4 min in lift-off process. The I-V measurement for the 5 min lift-off process using ultrasonic vibration could not be done due to some problem in the sample. From these results, it also can be concluded that lift-off process using the ultrasonic vibration was not good choice either.

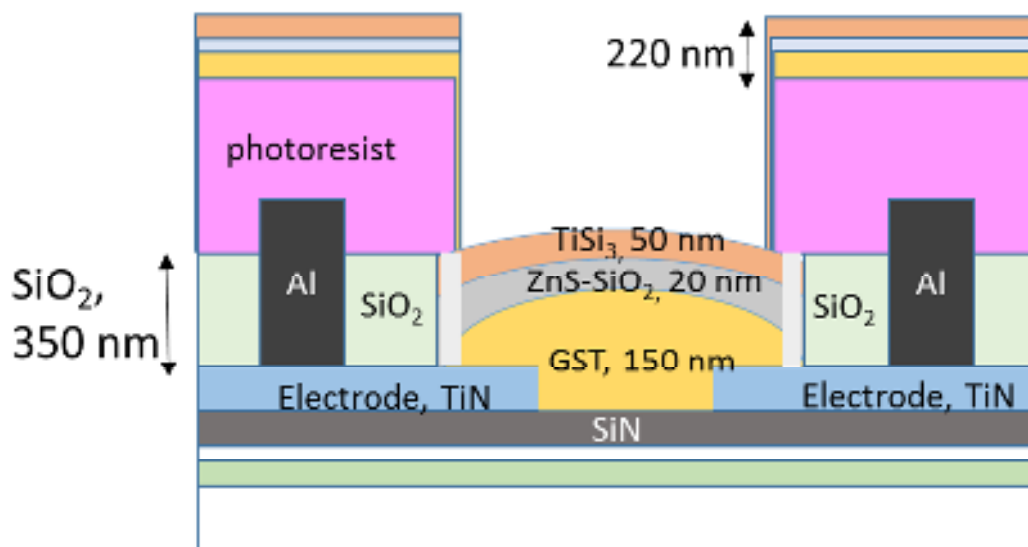Fig. 5.18 Schematic diagram for the first prototype of a separate-heater PCM.

For the first prototype of PCM cell, it was design to have the thickness of SiO$_2$ for about 350 nm, as shown in Fig. 5.18. The total sputtered thickness was 220 nm, making the differences between these two thickness was 130 nm. Since it was in nanometer range, the differences was very small. It can have the possibility for the TiSi$_3$ to be

connected to the photoresist layer on top of the SiO_2 layer. When the device undergo the lift off process, problem will occurred because the $TiSi_3$ will peel off together with the photoresist and might be leaving some of the GST layer on the SiN substrate. This explains why the resistance value for the above I-V measurements were not stable or cannot be read.

In order to overcome this problem, the SiO_2 layer was design to be thicker than the first prototype. The thickness of the SiO_2 layer was made to be 500 nm, making the differences level between the sputtered layer and the photoresist became 280 nm. With this thickness, it can help to prevent the $TiSi_3$ layer from being connected to the photoresist layer and being peel off together with the photoresist during the lift off process.
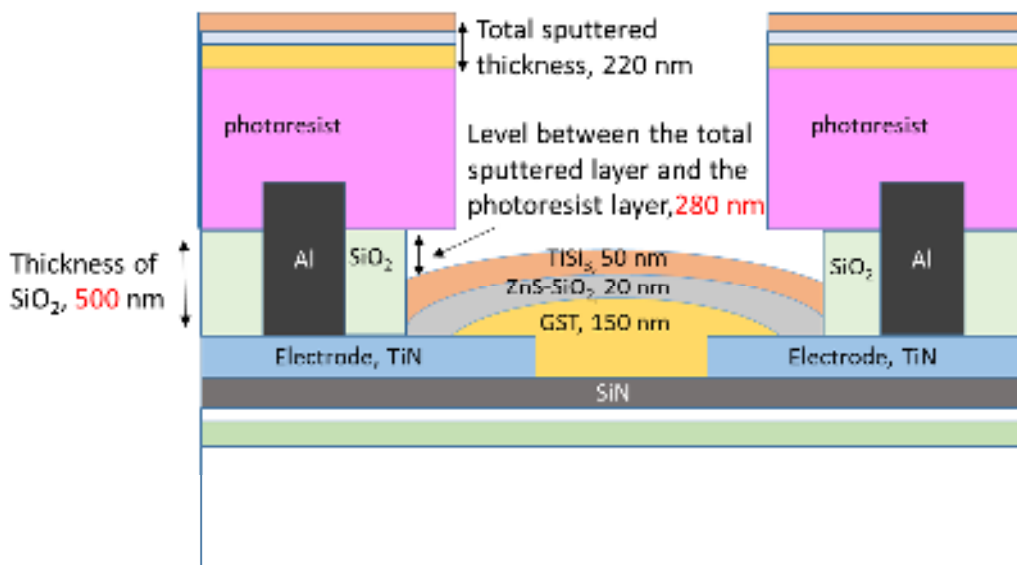

Fig. 5.19 Schematic diagram for the separate-heater PCM after increasing the thickness of SiO_2 layer for better lift-off process.

After making some amendments on the substrate structure to allow easier lift-off process without effecting the memory layer and the separate-heater layer, the optimum time of lift-off process need to be investigate once again. The resist that was attached on top of the Al electrode need to be removed to form the separate-heater and the memory channel unit. The process started with sputtering the GST layer (150 nm), followed by ZnS-SiO$_2$ layer (20 nm) and lastly TiSi$_3$ layer (50 nm) as the separate-heater layer.

The substrate was then cleaned using the ultrasonic vibration soaked in the PGMEA solution for various time, which was 0, 0.5, 1 and 2 minutes. After this process, the substrate was observed under an optical microscope.

Fig. 5.20 shows the I-V measurement GST layer of the separate-heater PCM device after 2 min of lift-off process. The resistance value was 66 MΩ, slightly bigger than the value calculated from the resistance equation in chapter 6.0, which was 9.3 MΩ. Fig. 5.21 shows the I-V measurement TiSi$_3$ layer after 2 min of lift-off process. The resistance value of the heater layer was 1 kΩ, which was closed to the value calculated from the equation, 0.9 kΩ. From these I-V measurement result, it can be concluded that the lift-off process was successful, allowing good current flow in the device.
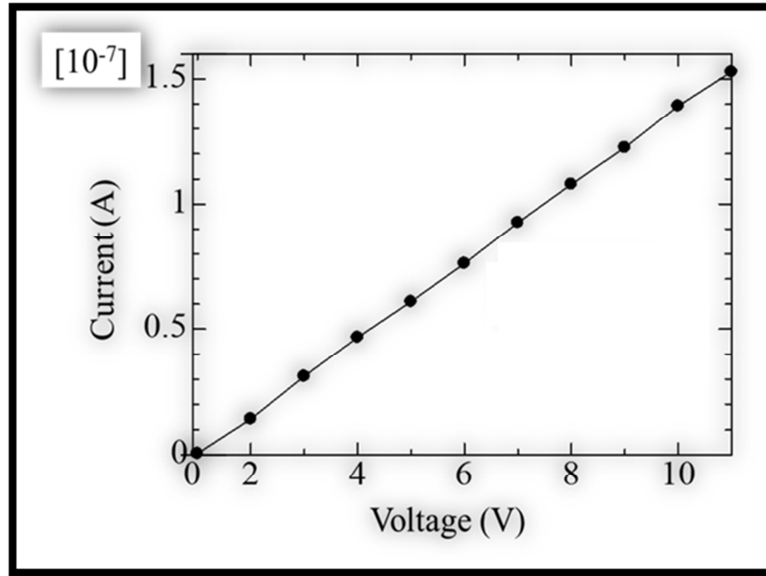
Fig. 5.20 I-V measurement of GST for separate-heater PCM device after 2 min of lift off process (after amendments).
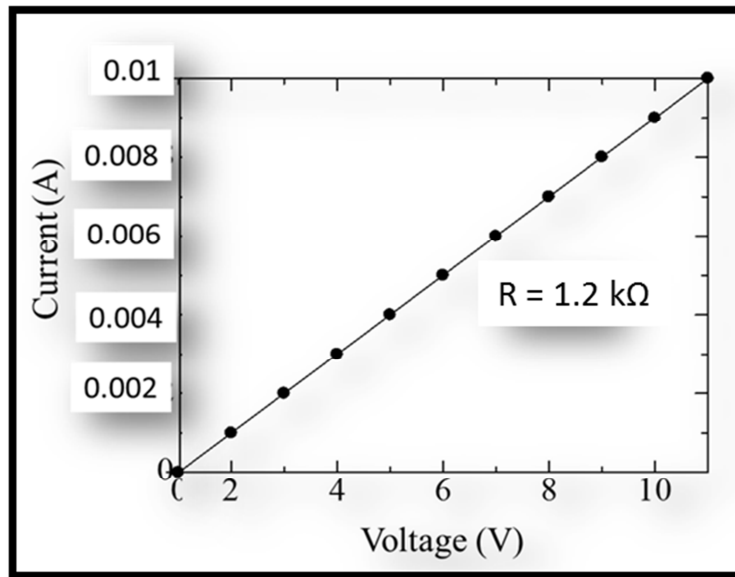

Fig. 5.21 I-V measurement of TiSi$_3$ for separate-heater PCM device after 4 min of lift off process (after amendments).

5.2 Conclusions

There are 3 important process that are needed in order to fabricate the separate-heater PCM device. The process consist of wet etching process, sputtering process and lift off process. For the wet etching process HF/NH$_4$F and the thickness of the SiO$_2$ layer was observed using AFM. After the wet etching process, the device will undergo the sputtering process to sputter the GST/ZnS-SiO$_2$/TiSi$_3$ into the channel. Lastly, lift-off process was done to peel-off the photoresist layer using the ultrasonic vibrator. Below are the conclusions that can be made from these three process.

(a) Wet etching process

1. The optimum for wet etching process was 8 min. This was confirmed by using the AFM by investigating the step level of the thickness of the SiO$_2$ layer in between the TiN electrodes.

(b) Sputtering process

1. The GST/ZnS-SiO$_2$/TiSi$_3$ layer were deposited using a RF sputtering machine by ULVAC.

2. Reverse sputtering before moving the substrate to the sputtering chamber was essential to ensure that the materials were beautifully sputtered onto the substrate, enabling a good current flow for the resistance measurement,

(c) Lift-off process

1. For the first prototype, problems occurred causing the current flow through the channel bad.

2. The heater layer was stripped off together with the CH photoresist at 2 min of lift-off process with or without an ultrasonic vibration for the first prototype of the separate-heater PCM device..

3. For the second prototype, which the SiO_2 layer was thicker than the first prototype at 500 nm, the optimum time for the lift-off process was 2 min using an ultrasonic buffer.

Chapter 6 Phase-change Experimental

In this chapter, the experimental work was done using the prototyped separate-heater PCM. For the first part, SET pulse voltage was induced to the $TiSi_3$ to investigate the possibility of crystallization in the GST by the separate-heater. Then, for the second part of the experiment, RESET pulse voltage was given directly to the GST layer through the Al electrode to bring it back to its initial state which was the amorphous state. Then, I checked whether two experiments were repeated to see the write/read cycle of this separate-heater PCM. The possibility of multi storage was also investigated.
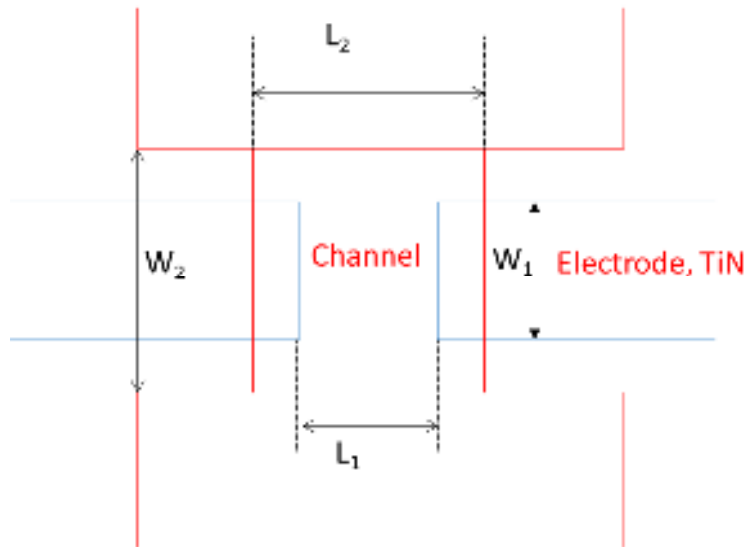
Fig. 6. 1 Schematic diagram of a separate-heater PCM device showing a superimpose of the GST channel and the separate-heater (red).

Fig. 6. 1 shows the schematic diagram of the separate-heater PCM. The blue part is the TiN electrode and the red part is an area of deposited GST/ZnS-$SiO_2/TiSi_3$ layer. The bottom layer of the GST was connected to the TiN electrodes, while the separate-heater was not connected to them and applied by the pulse from large pads in the top layer (red area).

In this prototyped device, the channel of the separate-heater PCM was a 0.8 μm wide (W_1) and 0.4 μm long (L_1). The resistances of as-depo GST which was the amorphous state, the crystalline GST and TiSi$_3$ were estimated using Eq. 1. The R is the resistance, ρ is the resistivity, L is the length and A is the area of cross section. These resistances are shown in Table 6. 1 (a), (b) and (c).

$$R = \frac{\rho L}{A} \qquad (1)$$

The resistivities of the amorphous GST, crystalline GST and TiSi$_3$ were 2.801, 0.001 and 5.7×10^{-5} Ωm, respectively.

Table 6.1 (a) Resistance value of amorphous GST.

L_1(μm)	W_1(μm)	R(Ω)
0.8	0.8	18.6×10^6
0.4	0.8	9.3×10^6

Table 6.1 (b) Resistance value of crystalline GST.

L_1(μm)	W_1(μm)	R(Ω)
0.8	0.8	6.67×10^3
0.4	0.8	3.35×10^3

Table 6.1 (c) Resistance value of TiSi$_3$.

L_2(μm)	W_2(μm)	R(Ω)
1.6	1.4	1.3×10^3
1.2	1.4	0.9×10^3

6.1 Resistance control experiment for multilevel storage

A typical PCM device is schematically illustrated in Fig.6. 1. The GST, ZnS-SiO$_2$ were deposited using RF sputtering equipment (ULVAC MNS-3000-RF) with a thickness of 150 nm and 20 nm, respectively. The background pressure of the sputtering machine was below 5×10^{-5} Pa, the sputtering pressure was 0.2 Pa and the power was 100 W. A waveform generator (Model 2571, Tabor Electronics, Ltd.) was used to apply SET pulse voltage ranging from 0 V to 2 V with a pulse width of 100 ns directly to the GST layer. Device resistance R was measured at a low pulse voltage.
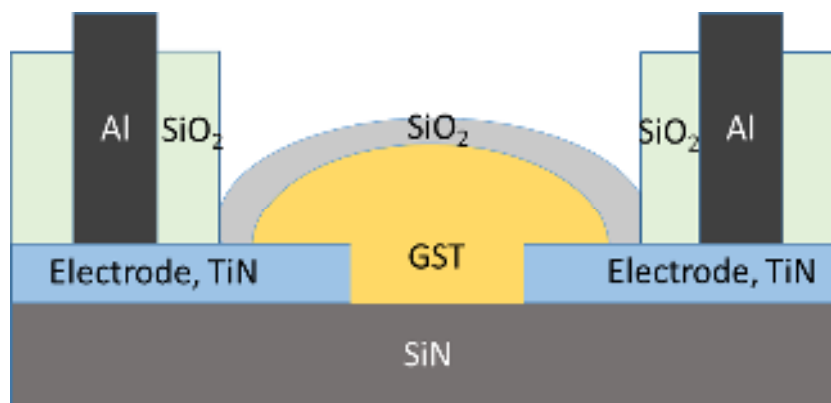

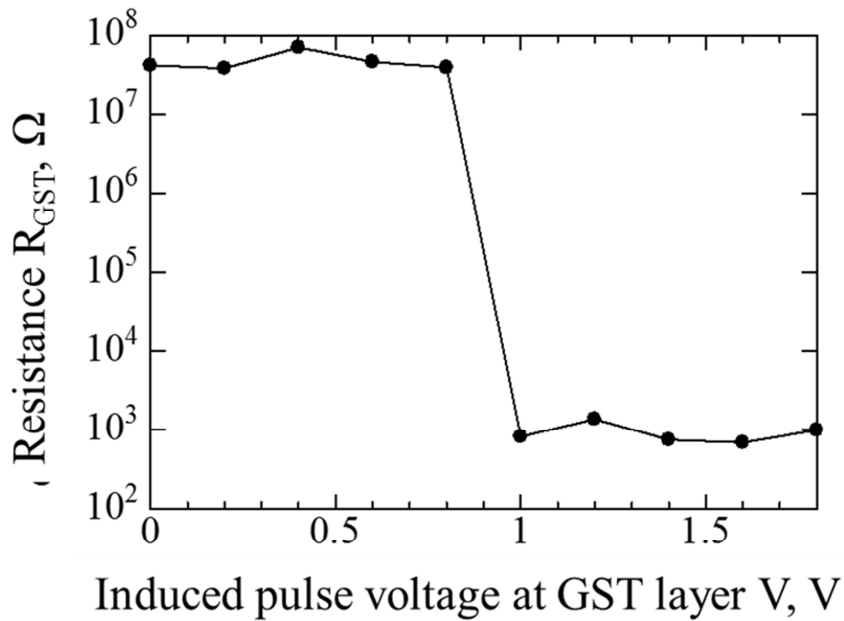Fig. 6.1 Schematic diagram of a typical PCM device

Fig. 6.2 Resistance drop in the GST layer due to an increasing SET pulse voltage for a typical PCM device.

Fig. 6. 2 shows a resistance drop in the GST layer due to the increasing pulse voltage. It shows a sudden drop of R_{GST} when a SET pulse is applied directly to the GST layer. The as-depo resistance of the GST layer was about 5×10^7 Ω and dropped directly to 7×10^2 Ω at 1 V pulse without any intermediate resistance levels. This indicates that it is difficult to control the crystallization process in order to obtain an intermediate resistance level for multilevel storage in typical PCM device. In order to overcome this problem, a separate-heater was added in the PCM device. An experimental work has been done and discussed in next section.

6.2 Resistance control experiment using separate-heater PCM device
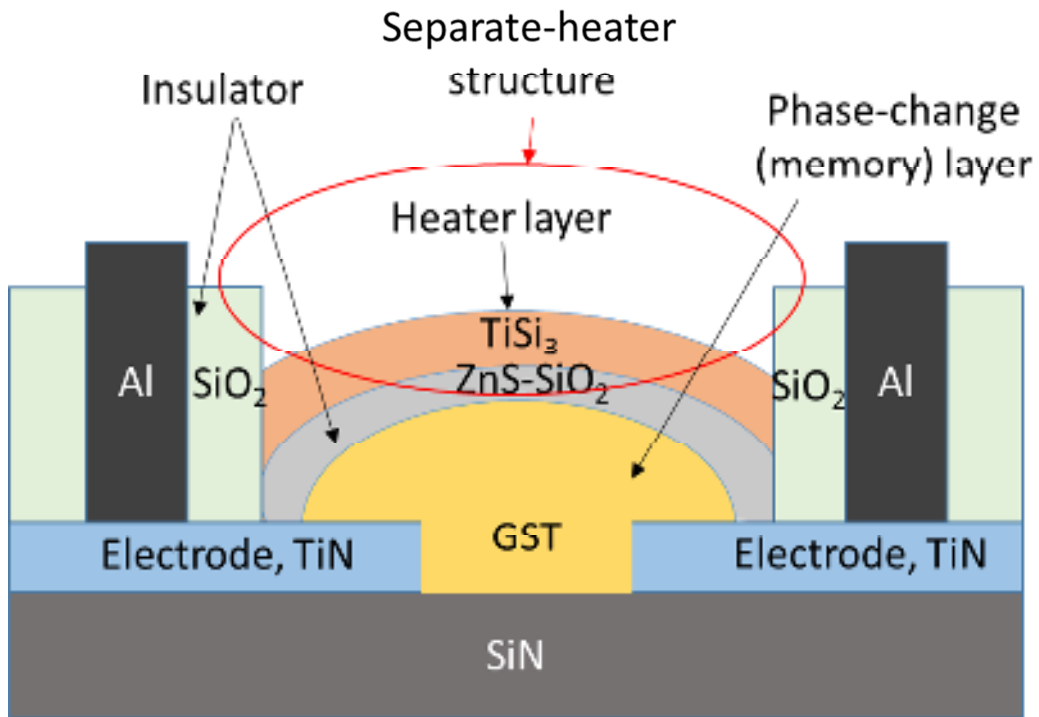
Fig. 6.3 Schematic diagram of a separate-heater PCM device.

Fig. 6.2 shows the schematic diagram of a separate-heater PCM device. The part in the circle is the separate-heater structure. It was not electrically connected to the GST layer since it was separated by the insulator layers which are SiO_2 on both sides and $ZnS-SiO_2$ on the bottom. As the $TiSi_3$ resistance value was constant, a controlled power can be transferred to the GST layer for the crystallization process since it can be controlled by the pulse amplitude V_{SET}. Possibility to achieve multilevel storage with this structure can be considered to be high.

6. 2. 1 SET experiment

Phase change experiment by the crystallization process was carried out using the prototype device. The schematic diagram of the device is shown in Fig. 6.4. The possibility of multi-level storage was investigated from this experiment.
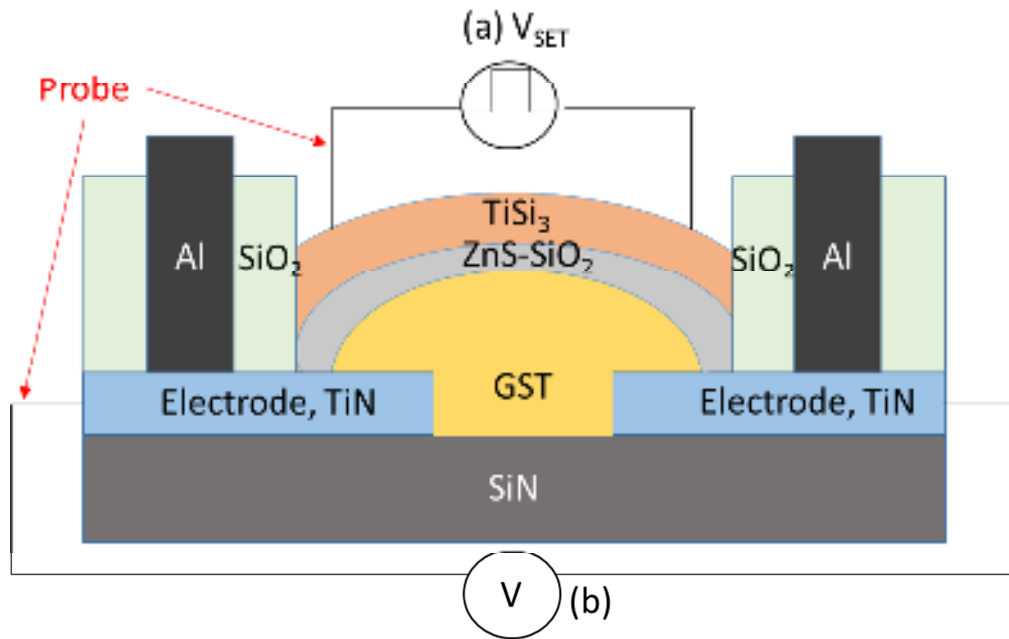

Fig. 6.4 Schematic diagram of separate-heater PCM device and pulse application

The GST, ZnS-SiO$_2$ and TiSi$_3$ layers were deposited using RF sputtering equipment (ULVAC, MNS-3000-RF) with a thickness of 150 nm, 20 nm and 50 nm, respectively. The sputtering condition was the same as previous condition. A waveform generator (Model 2571, Tabor Electronics, Ltd.) was used to apply SET pulse voltage to the GST, ranging from 0 V to 3 V with various widths of 100, 10 and 1 μs. The phase change resistance R was measured at a low pulse voltage.

At first, the electric probes were directly touched to the heater layer TiSi$_3$ as shown in Fig. 6. 3. The SET pulse voltage applying from the pulse generator was input to the

heater layer for phase-changing of the GST layer, The GST being heated as well through Joule heating. Since the resistance of the heater layer was constant, the power dissipated to the GST layer can be easily controlled. After applying of the SET pulse voltage to the heater layer, the resistance of the GST layer was read out. Here, the 2 probes were touched to the TiN electrodes that were directly connected to the GST layer. This sequence was done repeatedly with increasing the SET pulse voltage applying to the heater layer.

6.2.2 Crystallization due to the separate-heater PCM using electric probe.
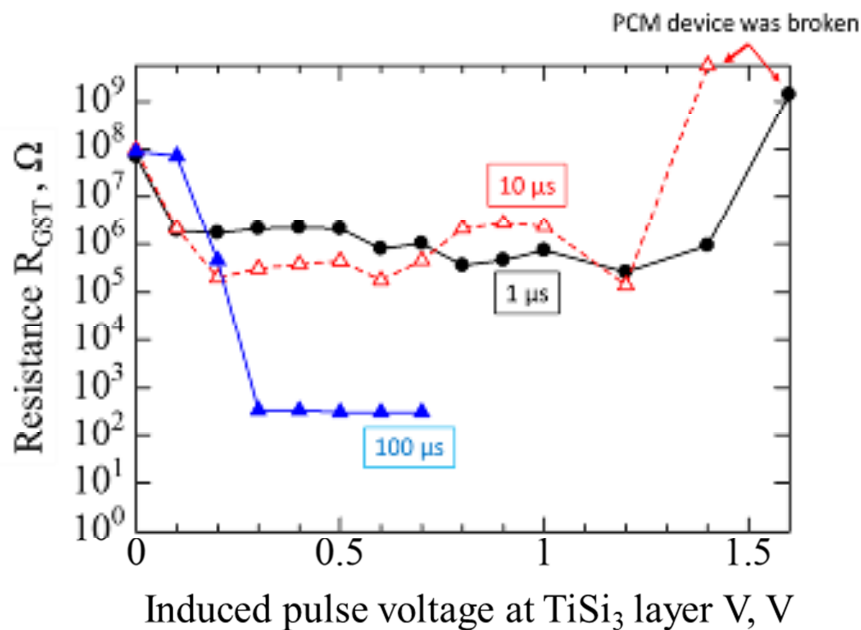

Fig.6.5 Resistance drop at GST layer with an increasing SET pulse voltage at TiSi$_3$ layer.

Fig. 6. 5 shows the resistance drop of the GST layer due to the increasing SET pulse voltage applying to the TiSi$_3$ layer. The as-deposited resistance of the GST layer was about 9×10^7 Ω and dropped directly to 5×10^2 Ω at an application of 0.3-V-pulse with a

width of 100 μs. For the drop, it is very difficult to control intermediate resistance levels by the pulse voltage. On the other hand, the resistance of the GST layer dropped to about 3×10^6 Ω and 3×10^5 Ω at applications of 0.3-V-pulse voltage with a width of 10 μs and 1 μs, respectively. The resistance of the GST layer of these two PCM devices also became constant at 0.2 V. At 1.3 V and 1.6 V the resistance of the GST layer suddenly increased to more than 9×10^7 Ω, for 10 μs and 1 μs, respectively. In other words, it can be thought that the PCM device was broken at these applications.

It also shows that the resistance of the GST layer changes by a factor of 10^5 when the SET pulse voltage with 100 μs was input. Since the objective of this work was to control the crystallization of the GST layer with the constant resistance of the heater layer at low SET pulse voltage, and to gain many intermediate resistance levels, applying 100-μs-pulse was considered not to be good choice.

Next, the 2 probes were directly touched to the heater layer of $TiSi_3$ to control the crystallization of the GST layer. This is because it was assumed that the probes have accidently connected to the GST layer in previous experiments. In other words, the sputtered layer of GST/ZnS-SiO_2/$TiSi_3$ was sputtered with a thickness in nanometer range. This means that the thickness was very thin so that it is difficult to control the probes only to the separate-heater without connecting to the GST layer as well (Fig.6. 6). This consideration explains well the experimental results (Fig. 6. 5) that the resistance of the GST layer dropped immediately without any intermediate resistance levels at 100, 10 and 1 μs of SET pulse voltage.

TiSi$_3$/ZnS-SiO$_2$ layer was sputtered at nanometer layer. The possibility of the probe to penetrate deep was high

V$_{SET}$

probe

TiSi$_3$

ZnS-SiO$_2$

SiO$_2$ Al

SiO$_2$ Al

Electrode, TiN

GST

Electrode, TiN

SiN
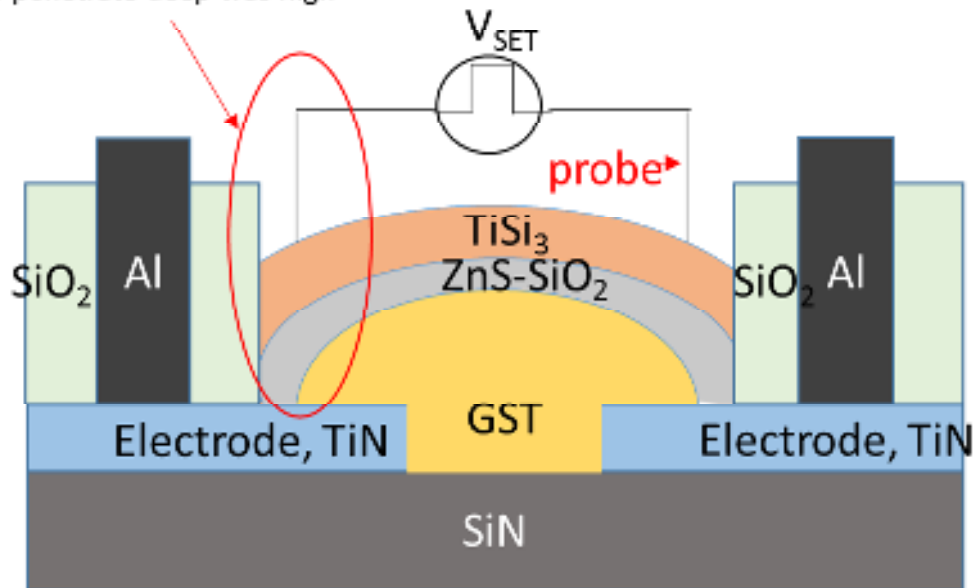
Fig. 6.6 Schematic diagram of separate-heater PCM device.

To overcome this problem, wire bonder was used. The PCM device was placed in the middle of a circuit board that has lots of electrodes. Then, the Al electrode and the TiSi$_3$ layer were connected to the electrodes on the circuit board by the wire bonder. The figure of the PCM device connected to the circuit board by the wire bonder is shown in Fig.6. 7.

Fig. 6.7 Optical microscope images of the device on the circuit board connected with the wire bonder.

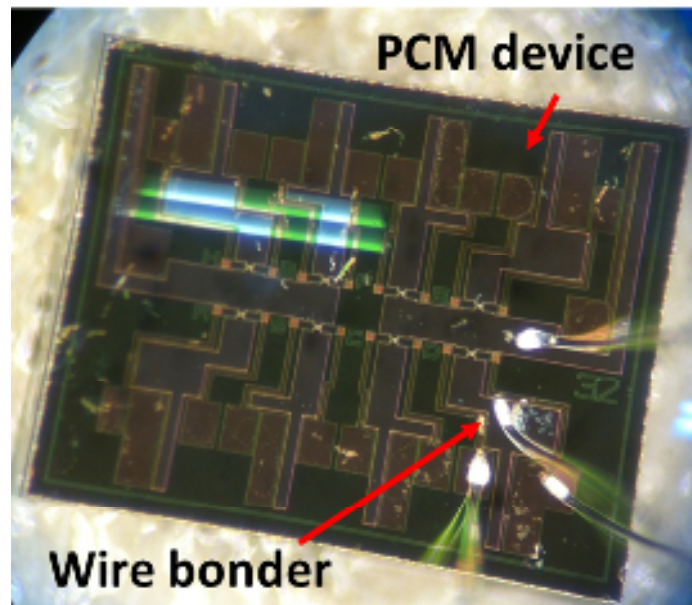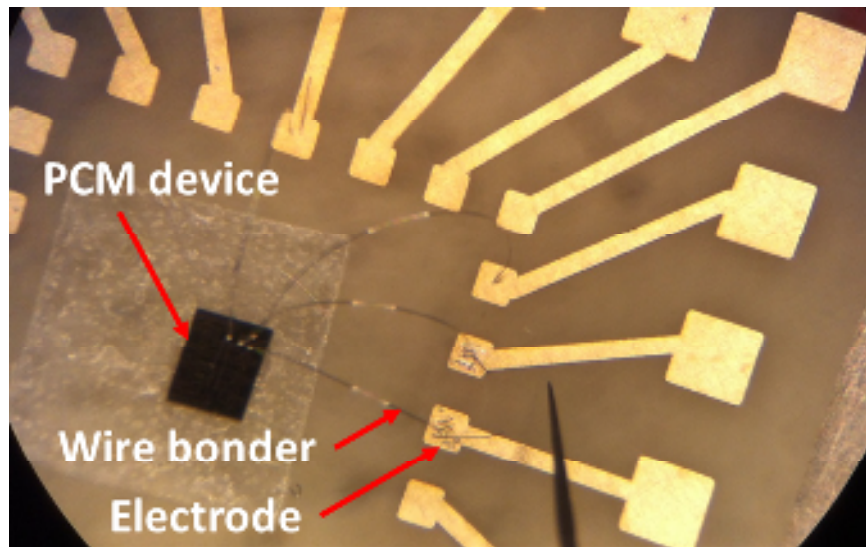## 6.2.3 Crystallization due to the separate-heater using bonded wiring

The SET experiment was done again after solving above problem by connecting the electrode with the wire bonder. A waveform generator (Model 2571, Tabor Electronics, Ltd.) was used to apply SET pulse voltage ranging from 0 V to 3 V with a width of 100, 50 and 20 ns. The GST resistance R was read at low pulse voltage. The concept of reading the resistance changes in GST layer was the same as described in previous section.

The probes were touched to the electrodes on the circuit board that was directly connected to the heater layer $TiSi_3$ as shown in Fig.6. 6. The SET pulse was applied from the pulse generator to the heater layer, making the GST layer heated as well through Joule heating.

The resistance of the GST layer was read out. The 2 probes were touched to the TiN electrode that was directly connected to the memory GST layer. This sequence was repeatedly done by increasing the SET pulse voltage applied to the heater layer.

Fig. 6. 8 shows a resistance drop of the GST layer as increasing the pulse voltage with a width of 200, 100, 50 and 20 ns. The as-deposited resistance of the GST layer was about 7×10^7 Ω. When a pulse voltage was applied for 200 ns, the resistance of the GST layer dropped a little by little until it saturated at an application of 2-V-pulse. The total of the resistance drop was about the factor of 10^2 and controllable intermediate resistance was achieved. For 100-ns-pulse, the resistance of the GST layer dropped from 10^7 to 10^4 Ω. This means that it is easy to control about 10 values of intermediate resistance by controlling of the pulse voltage. On the other hand, there were no changes of the GST resistance when applying 50- and 20-ns-pulse. From these results, it can be concluded

that crystallization of the GST layer was controlled successfully with the separate-heater when applying 100-ns-pulse.
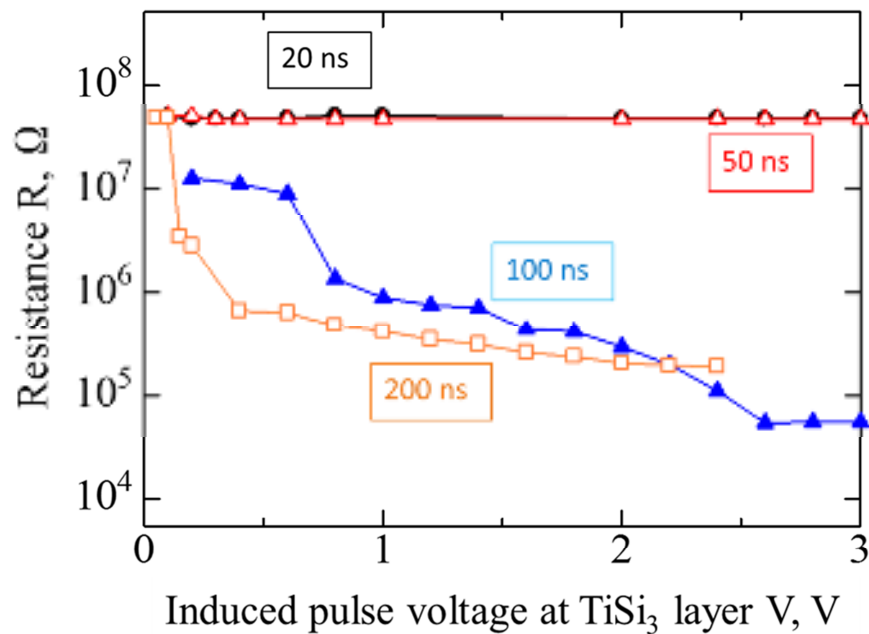

Fig. 6.8 Resistance drop at GST layer with an increasing SET pulse voltage at TiSi$_3$ layer.

Next, I will compare the experimental result with the simulation result described in Chapter 4.

Fig. 6. 9 shows gradual decrease of the GST resistance with increasing SET pulse amplitude for experimental work (red line) compared with the simulation result (black line). SET voltage pulse at 100 ns was applied to the heater layer and the resistance changes in the memory layer were investigated.

The figure shows that the resistance of GST layer started to drop at 0.6-V-pulse application, indicating that the temperature of the GST layer has reached to the crystallization temperature. In a range of pulse voltage from 1 V to 2.5 V, the resistance decreases gradually by a factor of about 10, showing the possibility to control many

intermediate resistance levels. This demonstrates that multilevel storage can be obtained successfully by controlling the crystallization using a separate-heater. Above 2.5 V, the resistance becomes constant. This experimental results agrees well with the simulation results described above.

In other words, with a separate-heater structure, crystallization process of the GST memory can be well controlled, allowing many intermediate resistance levels for multilevel storage.
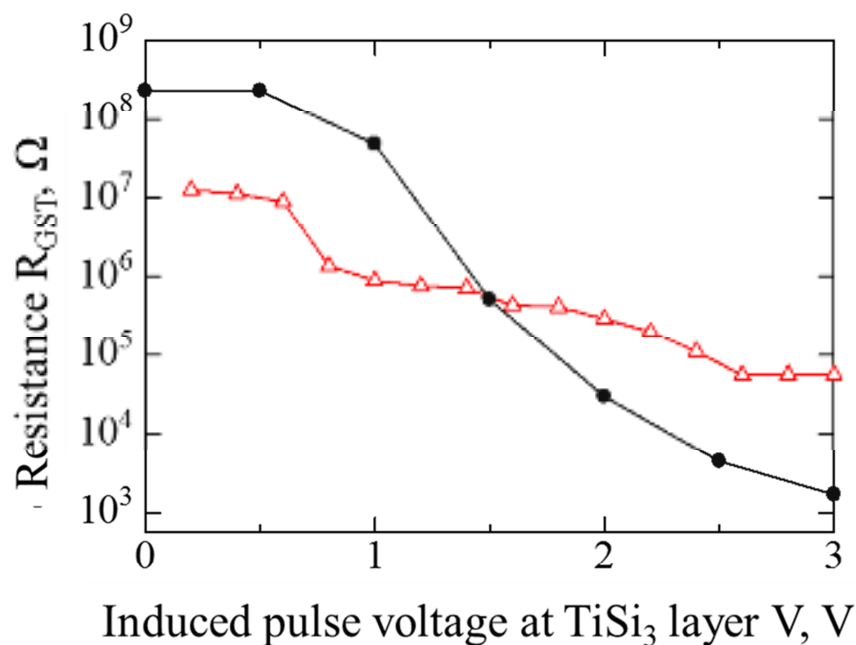
Fig. 6.9 Resistance drop at GST layer with an increasing SET pulse voltage at TiSi$_3$ layer for simulation and experimental results.

6.3 RESET experiment of the separate-heater PCM

After investigating the SET operation of the separate-heater PCM device in previous section, RESET operation must be investigated as well. This is important to know the read/write cycle of the device. The experiment started with applying SET pulse to the

TiSi$_3$ layer to heat up the GST layer. The SET pulse voltage was increased slowly until the crystallization of the GST layer completed. Before the next program pulse, the cell is brought again in the initial reference RESET state, which was an amorphous state, using a proper voltage pulse. Here, the read/write cycle of the separate-heater PCM was investigated.

A waveform generator (Model 2571, Tabor Electronics, Ltd.) was used to apply SET pulse voltage to the TiSi$_3$ layer, ranging from 0 V to 3 V for 100 ns in pulse width. The GST resistance R was read at a low pulse voltage. Then, after the GST resistance became constant, or in other words, has completely changed to crystal state, the RESET pulse was applied directly to the GST layer until it reached to the initial amorphous state. These steps were repeated after the PCM device reached to the initial state.

Fig. 6. 10 shows gradual resistance drop of the GST layer with increasing pulse voltage applied to the heater layer, ranging from 0 V to 3 V at 100 ns. For the first cycle (1st SET operation), the resistance of the as-deposited GST layer was around 1×10^7 Ω in the amorphous phase. The resistance decreased to 1×10^6 Ω at an application of 0.8 V. This was when the amorphous phase began to change to a crystalline phase. Then, the resistance drop was gradually starting at 1 V and became constant at approximately at 2.5 V.
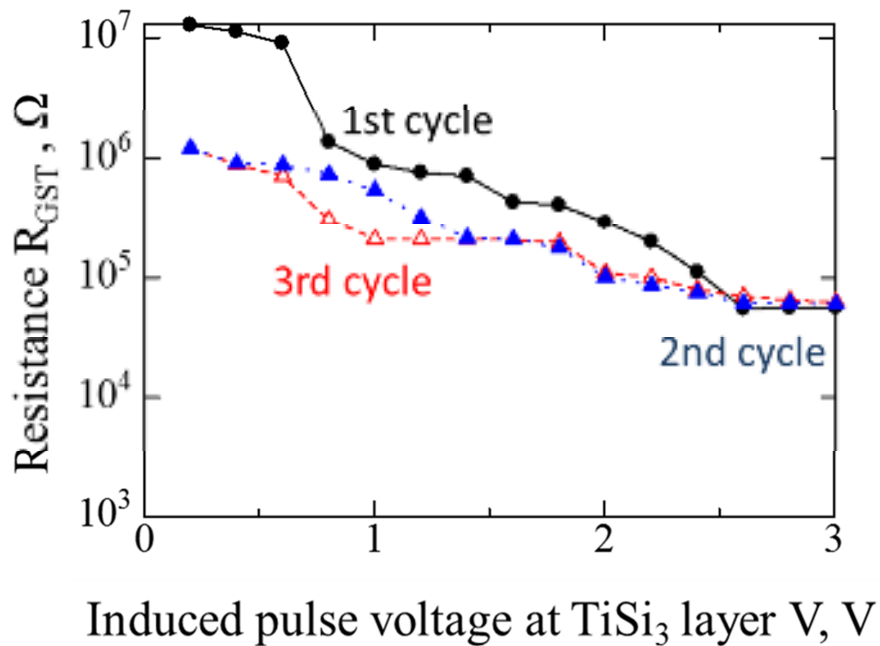
Fig. 6.10 Gradual resistance drop in GST layer with increasing SET pulse voltage to the heater layer.

Next, a RESET pulse at 100 ns was applied directly to the GST layer to make it become amorphous again. For the first cycle (to RESET state) as shown in Fig. 6. 10, the GST changed to partially amorphous phase at 3 V and the resistance value of the GST was up to about $1.2 \times 10^6 \, \Omega$.

Then, the SET pulse was applied once again for the 2nd cycle to the heater layer to investigate the reproducibility of the device operation. The resistance gradually dropped to $5 \times 10^3 \, \Omega$ and becomes to saturation at 2.5 V. A RESET pulse was applied for a third time and the amorphous resistance value was nearly the same as the previous cycle. This indicates that the PCM devices with the separate-heater was stable and was reproducible for more than two cycles.
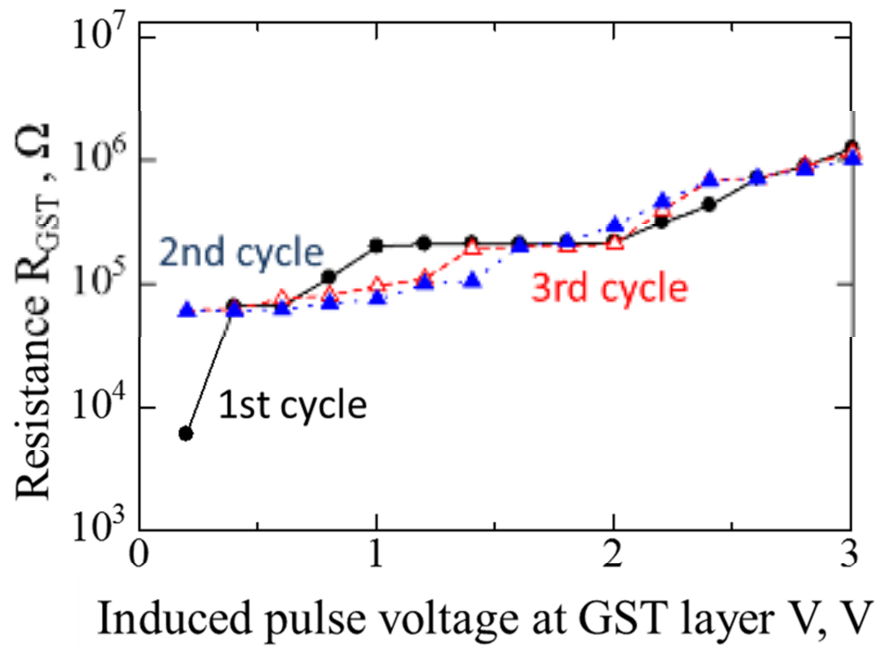
Fig. 6.11 Gradual resistance increament in GST layer with increasing RESET pulse voltage to the GST layer.

6.4 Conclusions

The experimental work was done using the prototyped separate-heater PCM. SET pulse voltage was induced to the $TiSi_3$ to investigate the possibility of crystallization in the GST by the separate-heater. Then, RESET pulse voltage was given directly to the GST layer through the Al electrode to bring it back to its initial state which was the amorphous state. The write/read cycle of this separate-heater PCM. The possibility of multi storage was also investigated. As the result, I have made the conclusions as below,

1. From the calculation, the resistance value for the amorphous GST, crystalline GST, $TiSi_3$ was 65.3×10^6 Ω, 116×10^3 Ω and 2.0×10^3 Ω, respectively. The channel was 0.4 µm long and 0.8 wide µm.

2. In a typical PCM device in 6.1.1, a sudden changed of GST resistance occurred when a SET pulse voltage was applied. It dropped from 5×10^7 ohm to 7×10^2 Ω at 0.8 V pulse amplitude.

3. For the separate heater, at 100 micro sec, resistance of GST dropped from 9×10^7 directly to 5×10^2 Ω at 0.3 V pulse amplitude and became constant. There was no intermediate resistance level. This problem occurred due to the very thin thickness of the sputtered layer, so that it is difficult to control the probes only to the separate-heater without connecting to the GST layer as well. Therefore, wire bonder method was applied.

4. Using the wire bonder method to bond the TiS_3 layer to the electrode on the circuit board shows good and reliable results. At 200 ns, the resistance of GST dropped gradually until it saturated at 2 V of pulse amplitude. At 100 ns, the resistance dropped from 10^7 to 10^4 with about 10 values of intermediate resistance value.

5. RESET pulse voltage at 100 ns was applied directly to GST layer to bring it to the initial state. Separate heater PCM device was thought to be stable and was reproducible.

Chapter 7 Summary

Recently, data density of storage media has increased tremendously. Multilevel NVM is increasing to fulfill this demand. A multilevel NVM can be used to store data on more than two levels per memory cell. More data can be stored without increasing the cell size.Phase-change memory (PCM) has the potential for the next generation NVM. It exhibits many advantages compared to flash memory such as fast switching speed, high endurance, low programmable energy and high scability. PCM operations, are based on the reversible switching of phase-change materials between amorphous and crystalline phases. $Ge_2Sb_2Te_5$ is widely used as phase-change material because it has high thermal stability at room temperature, high crystallization rate and good reversibility between amorphous and crystalline phases.

In conventional PCM devices, a sharp change occurs when a SET pulse is induced on the memory layer, GST. This makes the crystallization process difficult to control an intermediate resistance level for multilevel storage is not likely to be obtained. To overcome these issues, a PCM device with a separate-heater structure is proposed. This structure has the potential to achieve controlled crystallization operation for multilevel storage.

In this work, it has two important part which are simulation part and experimental part. For the simulation, FEM was applied by using commercial software, COMSOL 3.0. From here, several important results are obtained;

1. The resistance decreased by a factor of 10^5 for the separate heater device with ZnS-SiO2 capping layer after application of a 2 V pulse.

2. The resistance of the PCM layer after applying a 1 V pulse decreased gradually by a factor of 10^3.

3. Intermediate resistance value can be easily obtained by simply changing the pulse amplitude from 0.5 V to 2.5 V. This enables the possibility to achieve multilevel storage for the separate-heater PCM.

For the experimental part, it is divided into two. The first part is focused on the fabrications of the separate-heater PCM device. It consist 3 important steps which are wet etching, sputtering and lift off process. The conclusions that can be made for the fabrication process are as follows;

1. The optimum for wet etching process was 8 min. This was confirmed by using the AFM by investigating the step level of the thickness of the SiO_2 layer in between the TiN electrodes.

2. The GST/ZnS-$SiO_2/TiSi_3$ layers were deposited using a RF sputtering machine by ULVAC.

3. Reverse sputtering before moving the substrate to the sputtering chamber was essential to ensure that the materials were beautifully sputtered onto the substrate, enabling a good current flow for the resistance measurement,

4. For the first prototype, problems occurred causing the current flow through the channel bad.

5. The heater layer was stripped off together with the CH photoresist at 2 min of lift-off process with or without an ultrasonic buffer.

6. For the second prototype, which the SiO_2 layer was thicker than the first prototype at 500 nm, the optimum time for the lift-off process was 2 min using an ultrasonic buffer.

In the other hand, the second part of the experimental is the SET-RESET experiment. This part is very essential to PCM device because the possibility of multilevel storage

can be investigated. The conclusions are as follows;

1. From the calculation, the resistance value for the amorphous GST, crystalline GST, TiSi$_3$ was 65.3×10^6 Ω, 116×10^3 Ω and 2.0×10^3 Ω, respectively. The channel was 0.4 μm long and 0.8 wide μm.

2. In a typical PCM device in 7.1.1, a sudden changed of GST resistance occurred when a SET pulse voltage was applied. It dropped from 5×10^7 ohm to 7×10^2 Ω at 0.8 V pulse amplitude.

3. For the separate heater, at 100 micro sec, resistance of GST dropped from 9×10^7 directly to 5×10^2 Ω at 0.3 V pulse amplitude and became constant. This was due to the layers in between the channel was sputtered at nanometer range, making the possibility of the probe to penetrate deep until the GST layer was high. Therefore, wire bonder method was applied.

4. Using the wire bonder method to bond the TiS$_3$ layer to the electrode on the circuit board shows good and reliable results. At 200 ns, the resistance of GST dropped gradually until it saturated at 2 V of pulse amplitude. At 100 ns, the resistance dropped from 10^7 to 10^4 with about 10 values of intermediate resistance value. This results, agrees with the simulation results done in 4.2.

5. RESET pulse voltage at 100 ns was applied directly to GST layer to bring it to the initial state. Separate heater PCM device was thought to be stable and was reproducible.

From the results above, it can be concluded that the proposed PCM structure has an extremely good outcome. It shows the ability to obtain multilevel storage, which is very essential to PCM technology.

List of Related Papers

1. Rosalena Irma Alip, Yuki Koshita, Zulfakri Mohamad, You Yin and Sumio Hosaka"Effect of a Separate Heater Structure for Crystallization in Multilevel Storage Phase-Change Memory" International Journal of Nanotechnology (2013) - **accepted**

2. R. Alip, Z. Mohamad, Y. Yin, and S. Hosaka "Controlled Crystallization Process of Phas-change Memory device by a Separate Heater Structure" Key Engineering Materials, Vol. 596, 107-110 (2014).

3. R. I. Alip, R. Kobayashi, Y. Zhang, Z. Mohamad, Y. Yin, and S. Hosaka "A novel phase-change memory with a separate heater characterized by constant resistance for multilevel storage" Key Engineering Materials, Vol. 534, 136-140 (2013).

List of Presentations

1. Rosalena Irma Alip, Yuki Koshita, Zulfakri Mohamad, You Yin and Sumio Hosaka "Effect of a Separate Heater Structure for Crystallization in Multilevel Storage Phase-Change Memory " Sixth International Conference on Advanced Materials and Nanotechnology (AMN-6) 2013, Auckland, New Zealand (Jan. 2013).

2. R. Alip, Z. Mohamad, Y. Yin, and S. Hosaka "Controlled Crystallization Process of Phas-change Memory device by a Separate Heater Structure"4th International Conference on Advanced Micro-Device Engineering (AMDE), Gunma, Japan (Dec. 2012).

3. R. I. Alip, R. Kobayashi, Y. Zhang, Y. Yin, S. Hosaka "A Novel Phase-Change Memory with a Separate Heater Characterized by a Constant Resistance for Multilevel Storage" 3rd International Conference on Advanced Micro-Device Engineering (AMDE), Gunma, Japan (Dec. 2011).