STUDY OF HIGH EFFICIENCY AND LOW INPUT VOLTAGE POWER CONVERSION CIRCUITS FOR ENERGY HARVESTING APPLICATIONS

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PhD Dissertation

Submitted in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

Division of Electronics and Informatics
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4 February 2014 – Version 1.6

Zachary Zehner NOSKER:
Study of High Efficiency and Low Input Voltage Power Conversion Circuits for Energy Harvesting Applications, PhD Dissertation, © 4 February 2014

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What the result of these investigations will be the future will tell; but whatever they may be, and to whatever this principle may lead, I shall be sufficiently recompensed if later it will be admitted that I have contributed a share, however small, to the advancement of science.

— Nikola TESLA

This dissertation is dedicated to my parents, Sue and Richard. I owe all my success to their unending love, encouragement and support.

ABSTRACT

This dissertation summarizes research into power electronics for energy harvesting and mobile device applications. In order to familiarize the reader with basic power electronics concepts, Chapter 2 gives a brief overview of power electronic circuits, from linear regulators to switching buck and boost regulators. These circuits are presented in a simplified form and it is hoped that anyone with a basic understanding of microelectronics will be able to follow the explanation. While there are manifold other power electronic circuits in use in the world, their large size and reliance on transformers make them impractical for mobile applications. To this end, Chapter 2 focuses only on Buck (*step–down*) and Boost (*step–up*) regulators. Subsequent chapters delve deeper into the world of power electronics for mobile applications.

Since it is a new and developing field, Chapter 3 gives a survey of energy harvesting technology, including typical applications and examples of transducers that can be used as input sources. This introduction includes transducers that function from vibration (Piezoelectric Transducers), temperature difference (Thermoelectric Generators (TEGs)) and ambient light (Photovoltaic Transducers).

Chapter 4 gives a detailed account of power conversion circuits that have been introduced previously for energy harvesting applications. This explanation includes circuits for Piezoelectric, Thermoelectric and Photovoltaic transducers, and explains the operation of each circuit as well as their shortcomings.

Chapter 5 introduces a small, low power bootstrapped boost regulator that can start up with an input voltage of 240 mV and achieve a maximum efficiency of 97%. The proposed circuit uses two separate control schemes for startup and steady-state operation. A fixed-frequency oscillator is used to initially start up the circuit and raise the output voltage. Once the output voltage has reached a level adequate to bias the internal circuitry, a constant-on-time style hysteretic control scheme is used to regulate the output voltage. This hysteretic control scheme helps increase system efficiency compared to using conventional Pulse-Width-Modulated control. While maintaining a high efficiency, the proposed circuit is implemented using only three external components: two capacitors (input and output) and an inductor. The effectiveness of this approach is shown through Spectre simulation results. Additionally, a test chip consisting of the startup charge pump was taped out and evaluated on the lab bench. Characterization shows that this subsystem functions correctly and that it will be able to power the drivers and output switches when the full chip is taped out together.

Finally, one chapter of the appendix contains ongoing investigations into the output impedance of a multi-phase buck converter. Since these investigations into this area are outside the scope of energy harvesting, and since the results have not yet reached a level of academic breakthrough, this discussion is placed in appendix Chapter A. As power requirements in portable devices increase, more attention is being paid to the load transient response of the power electronic circuit, and how quickly the system can react to a change in load current. Measurement of the output impedance of the converter over frequency shows how the circuit will react to a load transient at any frequency, and can guarantee that the undershoot or overshoot is less than a certain maximum value. This data was collected using a Frequency Response Analyzer and the DA9210 4-phase buck converter provided by Dialog Semiconductor.

PUBLICATIONS

Some ideas and figures have appeared previously in the following publications:

JOURNAL PAPERS

I **Zachary Nosker**, Yasunori Kobori, Haruo Kobayashi, Kiichi Niitsu, Nobukazu Takai, Takeshi Oomori, Takahiro Odaguchi, Isao Nakanishi, Kenji Nemoto, Jun-ichi Matsuda, *A Small, Low Power Boost Regulator Optimized for Energy Harvesting Applications*, Analog Integrated Circuits and Signal Processing **75**(2), pp.207-216 (May 2013).

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X Hong Gao, Lin Xing, Yasunori Kobori, Zhao Feng, Haruo Kobayashi, Shyunsuke Miwa, Atsushi Motozawa, **Zachary Nosker**, Kiichi Niitsu, Nobukazu Takai, Takahiro Odaguchi, Isao Nakanishi, Kenji Nemoto, Jun-ichi Matsuda, *DC-DC Converter with Continuous-Time Feed-Forward Sigma-Delta Modulator Control,* IEEE Asia Pacific Conference on Circuits and Systems, Kaohsiung, Taiwan (Dec. 2012).

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XIII **Zachary Nosker**, Haruo Kobayashi, Hidenori Kobayashi, *Output Impedance Analysis for Multiphase Buck Converters in Mobile Devices,* 5th International Conference on Advanced Micro-Device Engineering, Kiryu, Japan (Dec. 19, 2013).

XIV Yasunori Kobori, Murong Li, Qiulin Zhu, Feng Zhao, **Zachary Nosker**, Shu Wu, Shaiful N. Mohyar, Haruo Kobayashi, Nobukazu Takai, *Single-Inductor Dual-Output DC-DC Converter Design with Exclusive Control Design with Exclusive Control,* 5th International Conference on Advanced Micro-Device Engineering, Kiryu, Japan (Dec. 19, 2013).

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ACKNOWLEDGMENTS

I would like to express my deepest appreciation to all those who provided me the possibility to complete this report. I would especially like to thank my supervisor at Gunma University, Professor Haruo KOBAYASHI for his tutelage and encouragement. I would also like to thank professors Nobukazu TAKAI and Ki-ichi NIITSU for valuable discussions during my time at Gunma University and Mr. Nobuyoshi ISHIKAWA for his help in managing funding, procuring lab equipment and always answering my questions about Japanese language and culture. I would also like to thank my review committee members, professors Kenichi ONDA, Yasunori KOBORI, Sumio HOSAKA and Sadao ADACHI. Additionally, I would like to thank professor Toshiaki ENZAKA for his help in setting up lab experiments and understanding the results.

For their help during joint research activities, I would like to thank the Tokyo engineering staff of Dialog Semiconductor for their help, encouragement, and valuable technical discussions: Hidenori KOBAYASHI, Naoyuki UNNO, Seiichi OZAWA, Nobuyuki NEGISHI, Olinver VINLUAN, Shiho HIROSHIMA and Kazuki YAMAMOTO. Also the management and engineering staff of AKM corporation: Jun-ichi MATSUDA, Kenji NEMOTO, Takeshi OMORI, Takahiro ODAGUCHI, Isao NAKANISHI, Kimio UEDA, Tetsuji YAMAGUCHI, Eiji SHIKATA and Tsuyoshi KANEKO.

I would also like that thank Ahmad BAZZI who introduced me to LaTeX and saved me considerable time in creating reports and presentations, including this dissertation. Also two students from my laboratory, Junshan WANG and Masahiro MURAKAMI, for their help in translating sections of this dissertation into Japanese.

Furthermore I would like to thank the professor who first sparked my interest in analog electronics, professor emeritus Sergio FRANCO of San Francisco State University. If not for his teaching of physical insight and circuit inspection over convoluted mathematics, I would not have achieved so much in such a short time.

I would like to thank the Marubun Research Promotion Foundation which provided me a research grant in my final year of studies and greatly reduced my financial burden in completing my research.

Finally I would like to thank the people of Japan and the Japanese Ministry of Education, Culture, Sports, Science and Technology (MEXT) who graciously provided me a full-ride scholarship to complete my graduate studies in Japan.

SYMBOL CONVENTION

This manuscript uses the symbol convention popularized by the likes of professors Paul R. GRAY and Robert G. MEYER. Any DC or large-signal quantity is displayed as an upper-case symbol with an upper-case subscript, such as V_I. Small-signal or AC quantities on the other hand are shown like v_i, i.e. a lower-case symbol with a lower-case subscript. Finally, a symbol with both DC and AC (or large- and small-signal components) is shown as a lower-case symbol with an upper-case subscript, such as v_I. This symbol convention is widely used in the field of analog electronics.

ELECTRONIC FILE FEATURES

This document was typeset with LaTeX and uses PDF hyperlinks extensively; every figure, equation, acronym and cited reference contains a hyperlink to the relevant object. Additionally, color is used liberally to highlight salient parts of figures. While it is still possible to read this dissertation in black and white printed form, it is highly encouraged that the reader seek out and read an electronic PDF copy instead.

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ACRONYMS AND ABBREVIATIONS

BJT Bipolar Junction Transistor

CCM Continuous Conduction Mode

CMOS Complimentary Metal Oxide Semiconductor

CTAT Complimentary To Absolute Temperature

DCM Discontinuous Conduction Mode

DUT Device Under Test

ESD Electrostatic Discharge

FRA Frequency Response Analyzer

HD High Definition

LDO Low Dropout Regulator

MCU Micro-Controller Unit

MIMCAP Metal Insulator Metal Capacitor

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MPP Maximum Power Point

MPPT Maximum Power Point Tracking

NMOS n-type MOSFET

opamp Operational Amplifier

PFM Pulse Frequency Modulation

PMOS p-type MOSFET

PTAT Proportional To Absolute Temperature

PWM Pulse-Width Modulated

RMS Root Mean Square

SoC System on a Chip

SMPS Switch-Mode Power Supply

TEG Thermoelectric Generator

TSMC Taiwan Semiconductor Manufacturing Company

ZCS Zero Current Switching

Part I

INTRODUCTION

1 BACKGROUND

Over the last few decades, we have become obsessed with mobile devices. When the cell phone boom started in the 1990s, consumers were just starting to understand the value of *always–on* communication systems, but now we can't live without them. Parents need to keep in touch with their children, school kids need to keep in touch with their friends, and company employees need to receive urgent e–mails from their bosses at any hour of the day or night. We have to be connected at all times—even 1 second of downtime is unacceptable.

But mobile devices are complicated systems, and they keep adding new features and increasing processor speeds. Each time a new feature is added, or a faster processor is introduced, the power requirements of the system increase. Yet to cut out features is tantamount to corporate suicide—consumers can't live without High Definition (HD) video chatting, high-resolution 3D games, video recording and high-speed web browsing from their smartphones. And since the competition is adding all these features, every smartphone manufacturer feels the need to catch up or stay ahead.

These changing specs put increasing strain on power supply designers, who have to design their circuits to work with tighter transient specs, at lower voltage, with much higher load currents. Failure to keep a regulated power supply for the System on a Chip (SoC) in these devices can lead to bit flips, kernel panics, and random restarts that completely ruin the user experience.

To make matters worse, consumers constantly complain about the battery life of their mobile devices. Even though this technology didn't exist 10 years ago, a smartphone that won't last all day without requiring recharging is considered useless. To address this perceived low battery life, power supply designers must also maximize the efficiency of their circuits; any small power loss is seconds of application time the user can't utilize.

Because of the industry demands, and the ever-changing problems faced by the design of their circuits, I have dedicated my research to the study to power electronics for mobile devices. Within this field, energy harvesting is an up-and-coming area that shows great promise in raising our quality of life.

1.1 ENERGY HARVESTING

Energy harvesting offers a chance to change the way we think about energy. By using transducers that capture energy from "free" sources

in the ambient environment, slight amounts of energy can be harvested in order to power real systems.

There are many ways that micro-power transducers could be used in energy harvesting systems. A piezoelectric or vibrational transducer attached to a bridge could be used to power a sensor grid. Thermal or vibrational transducers in implanted medical devices could reduce the dependence on invasive surgeries used to change batteries. Additionally, micro solar cells could be used to power watches or add power to cell phones.

In all of these examples, energy harvesting offers a way to reduce our dependence on conventional energy sources. If they are added to mobile devices, these systems could add trickle-charge to batteries and increase the amount of time a device can be used between charging. While this effect will probably be transparent to the user, the increase in battery life can have a significant impact on the perceived quality of a mobile device.

2

SURVEY OF POWER MANAGEMENT CIRCUITS RELEVANT TO MOBILE APPLICATIONS

Power management circuits (or *power converters*) are centered around creating a steady output voltage from a varying input source. A simple example of a power management circuit is a microprocessor being driven by a single-cell lithium battery, as is the case in modern cell phones. A single-cell battery typically has a voltage of 2.4 V at minimum charge to 5.5 V at maximum. Unfortunately, since the processor runs at a voltage around 1.0 V and uses a fine Complimentary Metal Oxide Semiconductor (CMOS) process, powering this chip directly with a 5.5 V supply will destroy the chip. In order to address this limitation, some type of power conversion circuit must be added between the battery and the microprocessor that delivers a constant 1.0 V no matter what changes with the input voltage or load current.

2.1 LINEAR REGULATORS

One way of addressing this constant output voltage requirement is via a simple Operational Amplifier (opamp) and a large output transistor as shown in Fig. 2.1. Using the fact that $V_P = V_N$ in the opamp, the DC transfer function can be written as in (2.1).

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_{REF} \tag{2.1}$$

By selecting a suitable reference voltage and tuning the feedback resistors to a proper ratio, the output voltage can be adjusted to any value that is desired. Additionally, as long as the opamp can control the feedback loop and the system is stable, the output voltage will

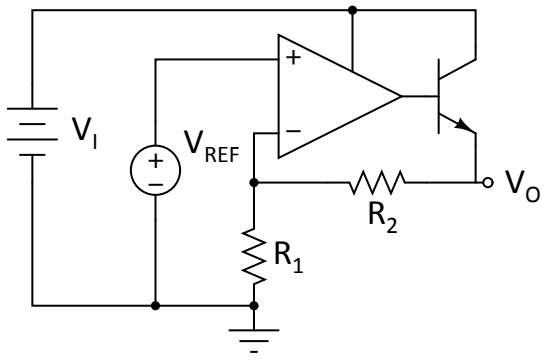


Figure 2.1: Simplified linear regulator schematic.

be well regulated at its set value. This type of power management circuit is known as a *linear regulator* due to the analog, linear control implemented using an operational amplifier.

Note that in this simple example, an NPN Bipolar Junction Transistor (BJT) is used at the output. This output transistor is commonly implemented with an n-type MOSFET (NMOS), though an NPN is shown for its relative simplicity. In general, this output transistor only acts as a unity-gain current buffer and should be a large enough size (and with a large enough heat-sink, if required) to handle the maximum load current of the system.

2.1.1 *Power Loss and Efficiency*

While the linear regulator shown in Fig. 2.1 is a simple circuit to implement, it generally suffers from high power loss and low efficiency. Consider the situation in Fig. 2.2 where the regulator is feeding a constant load I_O. In this case, the power delivered to the load is

$$P_O = V_O I_O. \tag{2.2}$$

Ignoring the quiescent power consumed by the opamp, the input power is

$$P_I \approx V_I I_O. \tag{2.3}$$

Thus, the efficiency of this circuit can be written as

$$\eta = \frac{P_O}{P_I} \approx \frac{V_O}{V_I}. \tag{2.4}$$

As an example, assume that the linear regulator is running from a 5 V input voltage, delivering 2 A of power to a 1.0 V load. In this case the efficiency is:

$$\eta \approx \frac{1V}{5V} = 20\%. \tag{2.5}$$

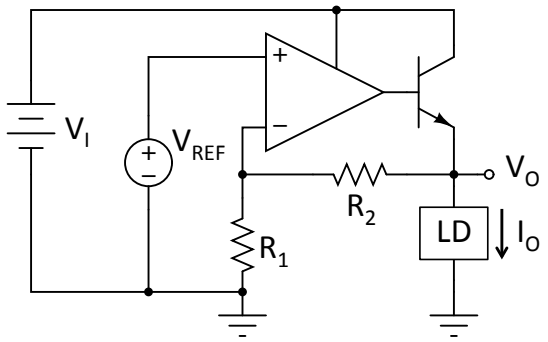


Figure 2.2: Linear regulator schematic with load.

While low efficiency is certainly an issue, another problem with this linear regulator is that the power loss (seen over the output transistor) is

$$P_{Loss} = (V_O - V_I)\, I_O = 4\ \text{V} \times 2\ \text{A} = 8\ \text{W}. \tag{2.6}$$

This power loss is converted to heat in the output transistor, and in a mobile application this would create too much heat which could not be properly dissipated.

2.1.2 *Low Dropout Regulators*

As mentioned in the previous section, the linear regulator of Fig. 2.1 will regulate nicely as long as the control loop (governed by the opamp) is stable. In order to maintain this stability, the output transistor must remain in the linear control region, hence (2.7) and (2.8) must be satisfied.

$V_{BE(ON)}$ is the Base-Emitter voltage when the BJT is ON

$$V_{BE} > V_{BE(ON)} \tag{2.7}$$

$V_{CE(sat)}$ is the Collector-Emitter voltage at which the BJT saturates

$$V_{CE} > V_{CE(sat)} \tag{2.8}$$

In order to accommodate these requirements, assuming that the operational amplifier can swing its output rail-to-rail, the maximum output voltage is

$$V_{O(max)} = V_I - V_{BE(ON)}. \tag{2.9}$$

Since $V_{BE(ON)}$ is usually around 0.7 V, even the maximum output voltage can lead to a significant power loss at higher currents. If the output voltage is set to less than $V_{O(max)}$, the power loss across the output transistor will be even higher.

One way to minimize this power loss (and improve efficiency) is to use a PNP output transistor as shown in Fig. 2.3. While this approach will still have a power loss across the output transistor, the maximum output voltage is now higher because

$$V_{O(max)} = V_I - V_{EC(sat)}. \tag{2.10}$$

Since the saturation voltage of the PNP BJT (labelled $V_{EC(sat)}$) is only on the order of 0.2 V, this lower voltage appearing across the output transistor also leads to a lower power loss. The minimum voltage allowed between the input and output voltage in a linear regulator is

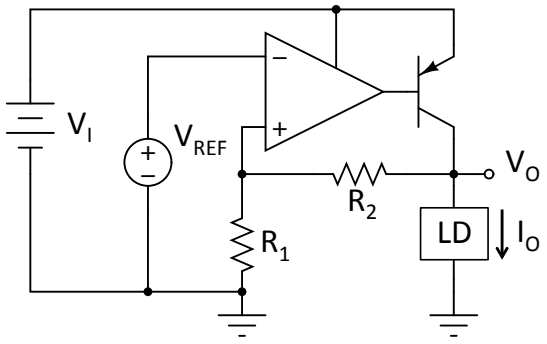


Figure 2.3: Low dropout regulator.

called the *dropout voltage*, and hence the circuit of Fig. 2.3 is called a Low Dropout Regulator (LDO).

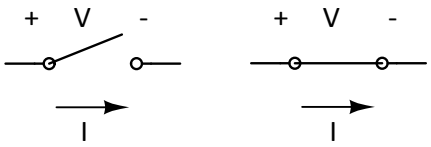
Note that switching the output transistor to a PNP also requires changing the inputs to the opamp since the PNP is operated as a common-emitter inverting amplifier. Additionally, by adding a final gain stage and the output transistor, the control loop varies considerably depending on the output load. Because of this issue, LDOs tend to be difficult to stabilize over a wide operating range, and careful attention needs to be paid to the opamp (control circuitry) and compensation network design.

Also like before, LDOs are commonly implemented using p-type MOSFET (PMOS) output transistors, but a PNP is used in this example because it is easier to estimate the on-voltage and saturation voltage of Bipolar Junction Transistors.

2.2 SWITCHING REGULATORS

While the linear regulators described in the previous section work well and are suitable for a variety of applications, higher efficiency can be achieved by using switches, inductors and capacitors to regulate an output voltage. The fundamental principle behind Switch-Mode Power Supply (SMPS) is that for an ideal switch, the power loss is always zero watts.

Fig. 2.4a and Fig. 2.4b show ideal open and closed switches, respectively. For an open switch, the voltage across the switch can be any value but the current through is zero. Similarly, for a closed switch,



(a) Open switch. (b) closed switch.

Figure 2.4: Ideal switches.

the current through the switch can be any value but the voltage across is zero. Because of this, an ideal switch will have no power loss because

$$P_{LOSS} = V \times I = 0 \text{ W}. \tag{2.11}$$

In practical regulators, non-ideal transistor switches are used, and as such there are a number of power losses related to non-ideal switches.

By utilizing switches, inductors and capacitors, high-efficiency converters can be created that step down the output voltage (buck converter), boost up the output voltage (boost converter) or both (buck-boost converter). A brief introduction to buck and boost converters will be presented in the next subsections.

2.2.1 *Buck Converter*

A buck converter is a step-down converter that creates an output voltage less than the input voltage. Due to its high efficiency, buck converters are widely used to power microprocessors, where a higher voltage like a battery or 12 V supply is stepped down to around 1.0 V to power the microprocessor.

Figure 2.5 shows a conceptual buck regulator schematic. The buck regulator requires that the output voltage is less than the input voltage, which can be seen by analyzing the circuit. Switch S is generally operated with a fixed period and a duty cycle D. Inspecting the circuit, we notice that the inductor L and capacitor C form a simple second-order low-pass circuit, and because of this, the output voltage is the average of the input voltage (as long as the inductor current stays positive).

For a more mathematical analysis of the buck converter, consider the timing chart in Fig. 2.6. Assuming the diode is ideal and the converter operates in Continuous Conduction Mode (CCM), i.e. the inductor current is always positive, steady-state operation means that the inductor current value does not change over one full cycle. Mathematically, this can be expressed as:

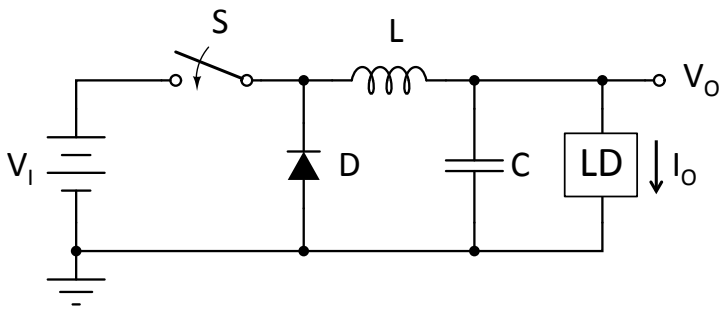


Figure 2.5: Conceptual buck regulator.

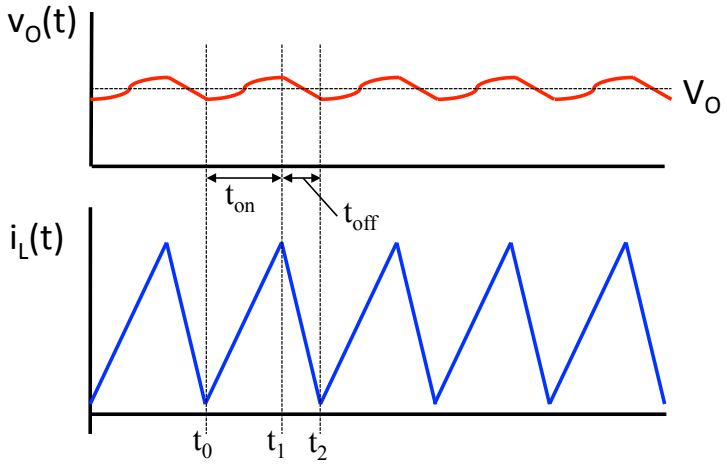


Figure 2.6: Buck regulator steady-state timing diagram.

$$i_L(t_0) = i_L(t_2) \tag{2.12}$$

Which implies that

$$\int_{t_0}^{t_1} i_L(t)\,\mathrm{d}t + \int_{t_1}^{t_2} i_L(t)\,\mathrm{d}t = 0. \tag{2.13}$$

At this time, it is convenient to note that, for an inductor charging with a constant voltage, we can use the relation

$$L\Delta I = V\Delta t. \tag{2.14}$$

Note that (2.14) is the inductor equivalent of the well-known $C\Delta V = I\Delta t$ used in analog circuit design to model a capacitor charged with a constant current. By inspecting the circuit and using the simplification of (2.14), we see that (2.13) can be re-written as

$$(V_I - V_O)\, L \times t_{on} + V_O L \times t_{off} = 0. \tag{2.15}$$

Equation (2.15) is known as the *inductor volt-second balance* equation, since the terms on the left and right consist of the voltage across the inductor multiplied by the amount of time the inductor charges (or discharges). This equation can be re-written in the more compact and well-known form

$$\frac{V_O}{V_I} = D \tag{2.16}$$

where D is the *Duty Cycle* of the Pulse-Width Modulated (PWM) signal applied to control the switch ($D = t_{on}/T$ and $T = t_{on} + t_{off}$). Thus, as suggested earlier, the buck regulator acts like a low-pass filter and the output voltage is the average of the switching waveform.

2.2.1.1 *Buck Converter Addendum*

There are a number of subtle points that should be elucidated for the Buck converter.

First, the buck converter can run at 100% duty cycle. In this situation $D = 1$ and hence the output voltage is equal to the input voltage. In practical applications, there are times when 100% duty cycle operation is useful. Leaving switch S ON will not cause the inductor current to saturate or cause any other undesired behavior, since the input and output voltages will be equal.

Second, since the buck converter's L and C act as a low-pass filter, the output voltage rises (slightly) during the switch ON time, but falls back down during the switch OFF time. This somewhat subtle effect is shown in Fig. 2.6.

2.2.2 *Boost Converter*

Another basic switching converter is the *boost converter* which creates an output voltage larger than the input voltage. The schematic of a basic boost converter is shown in Fig. 2.7.

Unlike the buck circuit, the boost converter is a bit more difficult to understand just by inspecting the circuit. The boost regulator works by charging the current in the inductor L during the on-time, then discharging this current into the output capacitor and load during the off-time. By completing the mathematical analysis, it can be seen that the output voltage will always be higher than the input voltage. In fact, if the switch is never commutated, the inductor can be modeled as a short circuit, and the output voltage will equal the input voltage (assuming the diode D is ideal).

By utilizing the *Inductor Volt-Second Balance* approach used to derive (2.15), a similar expression can be obtained for the boost converter.

$$V_I L \times t_{on} + (V_I - V_O)\, L \times t_{off} = 0 \tag{2.17}$$

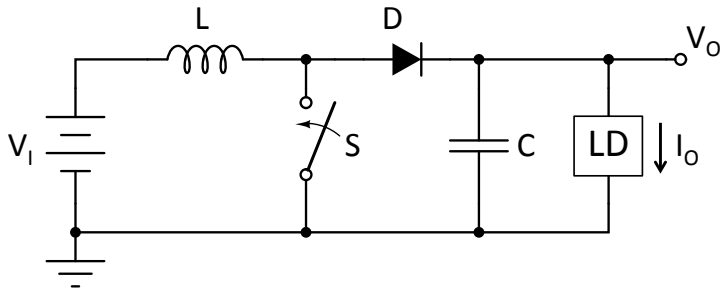


Figure 2.7: Conceptual boost regulator.

which can be rearranged as

$$\frac{V_O}{V_I} = \frac{1}{1-D}. \tag{2.18}$$

For a boost converter, (2.18) is the most common way to write the DC transfer function. This equation shows that when the circuit doesn't switch ($D = 0$), the output voltage will equal the input voltage, while at higher duty cycle the output voltage will increase.

2.2.2.1 *Boost Converter Addendum*

The preceding analysis of the boost converter shows that the output voltage is always higher than the input voltage, and will increase infinitely if the duty cycle reaches 100% ($D = 1$). Practically however, this is not the case. At 100% duty cycle, the boost converter's switch will always be ON, meaning that current will continually build up in the inductor. In a practical circuit, there is a limit to the maximum current that the switch and inductor can handle before failure, and hence 100% duty cycle is not feasible. Practically, the output voltage at 100% duty cycle will also decrease, and the transfer function will actually reach zero. Because of this fact, it is very important to ensure that the switch in a boost regulator always turns OFF for some amount of time, causing the output voltage to rise. Additionally, parasitic components in a boost regulator have a large impact on the DC transfer function and on the overall performance of the circuit.

Because of these two issues, even when performing a simple circuit simulation, parasitic resistances and practical components should be added whenever possible. Moreover, circuitry that guarantees that the switch turns OFF for some amount of time must also be implemented.

2.2.3 *Synchronous Switch Topology*

The buck and boost converter circuits shown previously are *asynchronous* circuits, i.e. they require a diode to function, and the inductor current will hit zero amperes if the load current is too low. In portable applications however, the *synchronous* topology is usually employed. With an asynchronous regulator, if the inductor current drops to zero for some time, the circuit operates in Discontinuous Conduction Mode (DCM). While this is useful in some applications, discontinuous conduction mode is not commonly used in portable applications. Instead, the synchronous switch topology utilizing a second switch (replacing the diode) is used. A simplified synchronous buck converter circuit is shown in Fig. 2.8.

By adding a second switch S_2, the inductor current can now flow in the negative direction, meaning that current flows up from ground, through S_2, and to the output capacitor/load. Because of this feature,

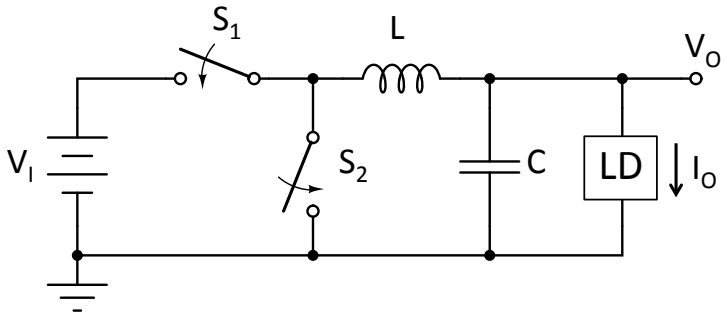


Figure 2.8: Conceptual synchronous buck regulator.

even when the load is 0A, the circuit will act as though it is still operating in continuous conduction mode, though now the inductor current can swing negative.

Similar to the synchronous buck converter, a simplified synchronous boost converter is shown in Fig. 2.9. Like the case of the buck converter, switch S_2 now takes the function of the diode in the asynchronous circuit. During the ON time, switch S_1 will be ON and charging the inductor current. During the off time, switch S_1 turns off and S_2 turns on, hence current built up in the inductor is transferred to the output capacitor and load through S_2.

2.2.3.1 *Synchronous Topology Advantages*

The previous discussion has assumed that diodes are ideal. Practically, in an asynchronous converter like the buck circuit in Fig 2.5, the inductor current will discharge through the diode D during the off-time. This discharge will also lead to a power loss of

$$P_{LOSS} = V_{D(on)} \times I \tag{2.19}$$

where I is the Root Mean Square (RMS) value of the current flowing through the diode during this time, and $V_{D(on)}$ is the *'on' voltage* of the diode. In applications where the current that flows through the diode is fairly small, this power loss is negligible. In mobile devices however, there is usually a large output current, hence using a diode would

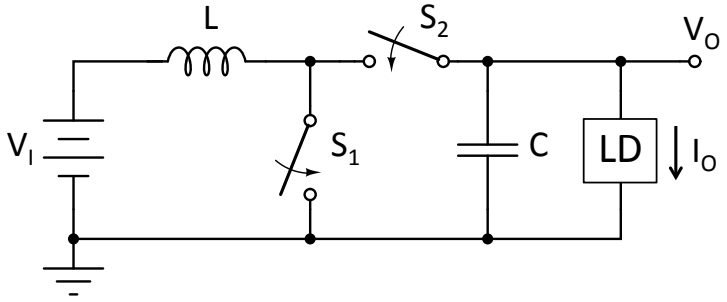


Figure 2.9: Conceptual synchronous boost regulator.

have a large effect on the efficiency of the system. Because of this, a synchronous topology is used in most portable power applications.

2.2.3.2 *Practical Implementation*

Since ideal switches and diodes don't exist in the real world, the switches shown in Fig. 2.8 are generally implemented with PMOS and NMOS transistors, as shown in Fig. 2.10.

To a decent approximation, a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) that is "OFF" is truly off, and no current flows through the channel. When a MOSFET is ON however, there is some conduction loss due to the fact that the channel has a finite resistance. Using the well-known triode MOSFET equation and approximating for V_{DS} being very small, an equation can be derived for this *on resistance* of the MOSFET.

$$r_{DS(on)} \approx \frac{1}{k' \frac{W}{L}(V_{GS} - V_t)} \tag{2.20}$$

Note that in (2.20), the variables W and L correspond to the gate width and length of the transistor, respectively. Hence, it can be seen that increasing the width of the MOSFET or increasing the gate-to-source voltage will reduce the on resistance. In a battery-powered application, the gate-source voltage of the MOSFET is usually fixed to the battery voltage, meaning that, practically, only the transistor width can be increased to lower the on-resistance.

The factor k' is known as the *process parameter* and is based on the type of process used to make these MOSFET transistors. While the full derivation of this variable is beyond the scope of this manuscript, it is interesting to note that for an NMOS, the value of k' is 2-3 times larger than that of a PMOS. Due to this discrepancy, the PMOS is generally designed with a width 2-3 times larger than its NMOS counterpart, ensuring that both NMOS and PMOS have identical (or nearly-identical) on-resistance.

This is due to the fact that electrons (n-ch) move faster than holes (p-ch)

While mathematically it seems that increasing the transistor width, or increasing the W/L ratio infinitely would be ideal, there are a number of other issues to consider. First, a larger transistor takes up more

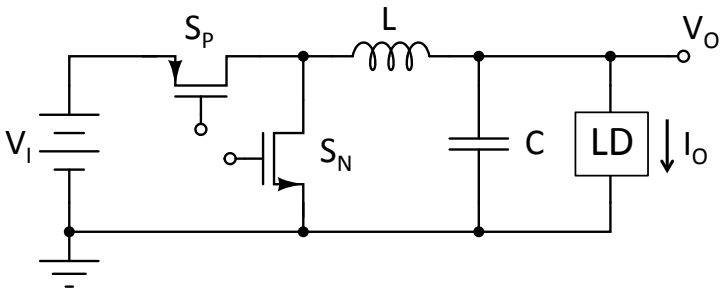


Figure 2.10: Practical implementation of a synchronous buck regulator.

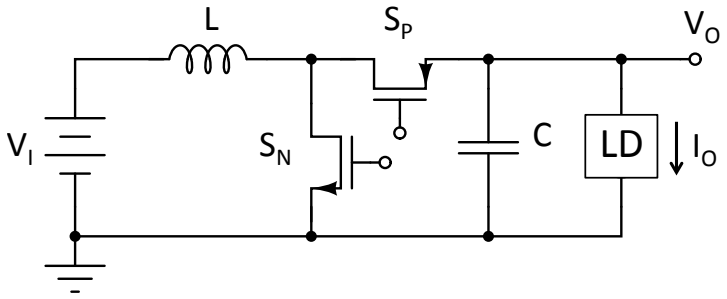


Figure 2.11: Practical implementation of a synchronous boost regulator.

chip area, which is especially problematic as die size shrinks smaller and smaller. Additionally, increasing the transistor size increases the gate capacitance, meaning that drivers must be made larger, while increasing the amount of dynamic switching losses from the transistors. In typical applications, there is a set size for power transistors or a minimum-allowable value of $r_{DS(on)}$ which engineers design around.

Similar to the buck converter, a synchronous boost converter can also be implemented using MOSFETs as shown in Fig. 2.11. While the MOSFETs themselves function similarly to the ideal switches shown in the previous boost regulator of Fig. 2.9, special attention should be paid to the gate driving voltage of these transistors. During the ON time, switch S_N is turned on, which can be accomplished by putting a large voltage (i.e. V_{IN}) at the gate of S_N. In order to keep S_P off during this time however, the source-to-drain voltage must be zero, hence the gate of S_N must be tied to the output voltage (which is higher than V_I). Notice that for the buck regulator this was not an issue—if the gates of both S_N and S_P switch between zero and V_{IN}, this is enough to turn the transistors ON or OFF.

While Metal Oxide Semiconductor (MOS) transistors aren't ideal switches (and will contribute to power loss in the system), they are good enough for many applications and have found wide adoption in power management circuits for mobile applications. As long as the process being used can tolerate an input voltage of about 5 V, almost any CMOS process can be used to implement power transistors. Of course, better processes will add mask layers to reduce $r_{DS(on)}$, reduce sensitivity to Electrostatic Discharge (ESD)/latchup or optimize other parameters that are important to power management circuits.

2.3 SUMMARY

This chapter has given a basic overview of power management circuits, including linear and switching regulators. Power management is a vast field where multiple textbooks are required to fully understand the principles and applications of all types of power converters. But for the purposes of this dissertation, it is hoped that the explana-

tions in this chapter give a decent introduction to power converters that are used in mobile applications.

Subsequent chapters introduce more complicated concepts in power management. In order to not overwhelm the reader, however, those explanations are written in their respective chapters.

Part II

TOPICS IN ENERGY HARVESTING

3

SURVEY OF ENERGY HARVESTING TRANSDUCERS

3.1 BACKGROUND

Energy harvesting represents a new way of thinking about energy. Instead of relying on power sources with limited supplies or severe drawbacks like gas or nuclear power plants, energy can be captured from ambient sources in our natural environment. There are a number of different types of energy harvesting transducers, and each could be used in different practical applications.

A piezoelectric or vibrational transducer attached to a bridge could be used to power a sensor grid. Micro solar cells could be used to power watches or add power to cell phone batteries, even when powered from relatively weak fluorescent lighting. Furthermore, thermal or vibrational transducers in implanted medical devices could reduce the dependence on invasive surgeries used to change batteries.

A typical system used in energy harvesting systems is shown in Fig. 3.1. The energy harvesting transducer is fed into some kind of battery management circuit (usually a boost converter) which stores harvested energy on some kind of energy storage component (battery, super-capacitor, etc). This stored energy can then be transferred to the system power supply (another power management circuit) which then drives a Micro-Controller Unit (MCU) and some kind of wireless interface circuit.

A good example of this energy harvesting system is a remote sensing network on a bridge. Natural vibrations of the bridge cause piezoelectric transducers to gather a small amount of energy, which helps

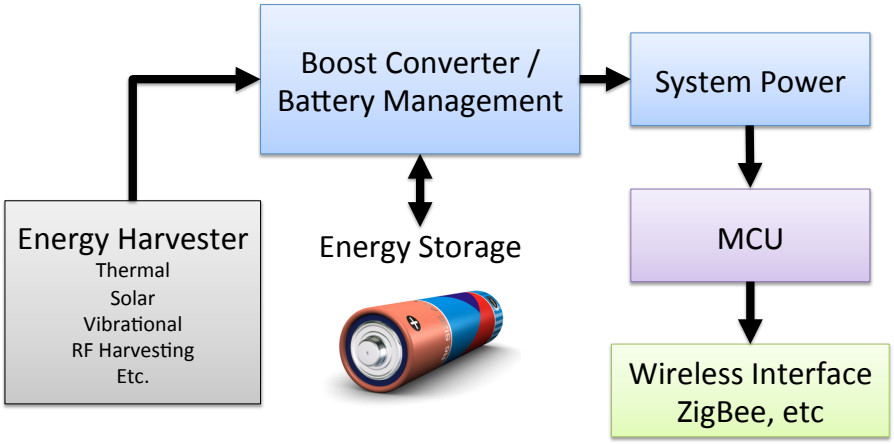


Figure 3.1: Conceptual energy harvesting system block diagram.

charge a battery. The energy stored in this battery can then be used to feed a low-power wireless network that reports the sensor readings periodically back to a main server. This wireless transmission can be performed with a *bursting* type of control, i.e. the transceiver is only active for a short amount of time (on the order of 1 ms per hour). This approach helps to lower the amount of power required by the system and ensures that the transceiver and MCU do not consume more power than the energy harvesting transducer can provide.

However, one drawback with conventional energy harvesting approaches is that they require a battery as a storage element. While battery chemistry gets better every year, there is still no battery that lasts forever, and in these systems the batteries would still need to be replaced at regular intervals.

3.2 TYPES OF ENERGY HARVESTING TRANSDUCERS

Focusing on the block diagram in Fig. 3.1, there are a number of different types of energy harvesting transducers that can be used. The most common of these are *Piezoelectric Transducers*, *Thermoelectric Generators* and *Photovoltaic Transducers*. Details about each of these three types of transducer are described in the following subsections.

3.2.1 *Piezoelectric Transducers*

Piezoelectric transducers generate electrical energy from vibrational energy. In practical applications, these transducers would be placed on some kind of structure that vibrates, like a bridge or a rotating piece of machinery. Vibrational transducers operate at a certain resonant frequency which can be changed by altering the effective length of the transducer or changing the position of a tuning mass.

One type of vibrational transducer is the LDT0-028K from Measurement Specialties [1] shown in Fig. 3.2. With this transducer, the large tuning mass shown on the left side can be altered in order to change the resonant frequency of the transducer. A larger tuning mass cor-

Figure 3.2: LDT0-028K piezoelectric transducer.

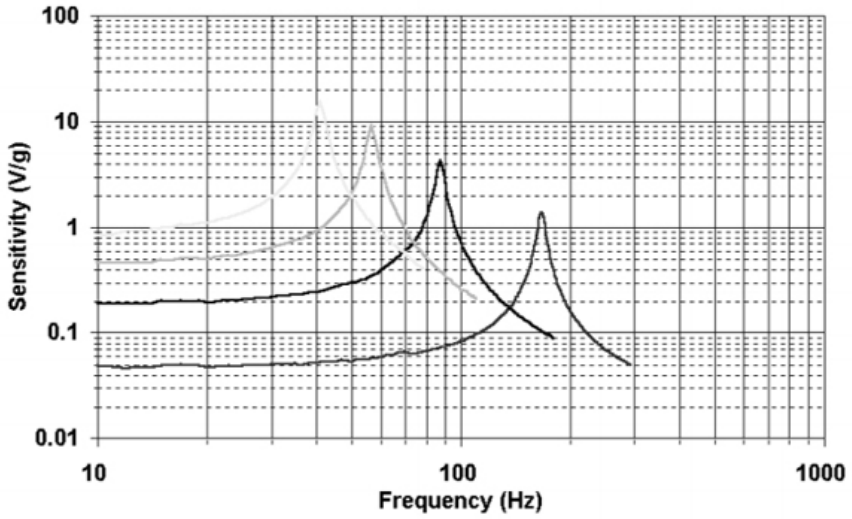


Figure 3.3: LDTo-028K piezoelectric transducer resonant frequency.

responds to a lower resonant frequency while no tuning mass corresponds to a resonant frequency of about 180 Hz, as shown in Fig. 3.3.

Since piezoelectric transducers are connected to some kind of vibrating source, the output of the transducer is an AC signal, and hence any power management circuits that convert this to a usable voltage will have to convert the AC signal into a DC signal. There are a number of prior works [2–5] that have investigated energy harvesting for piezoelectric systems. Details about each of these approaches will be presented in Section 4.2.

3.2.2 *Thermoelectric Generators*

A Thermoelectric Generator (TEG) is operated by exploiting the Seebeck effect, where an electrical signal is created if the junctions of two different conductors are held at different temperatures. Using this physical property, injecting current into a TEG can cause it to cool down, which is used in many industrial applications. Conversely, let-

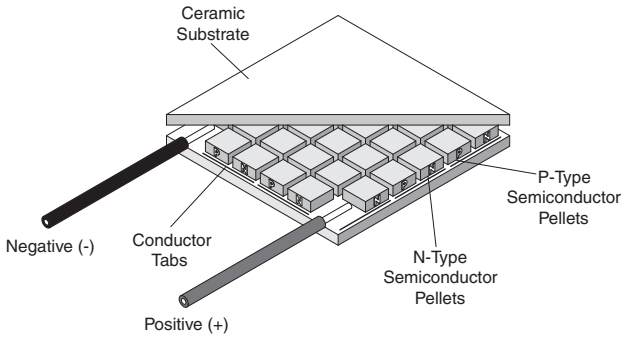


Figure 3.4: CUI CP85-series thermoelectric generator.

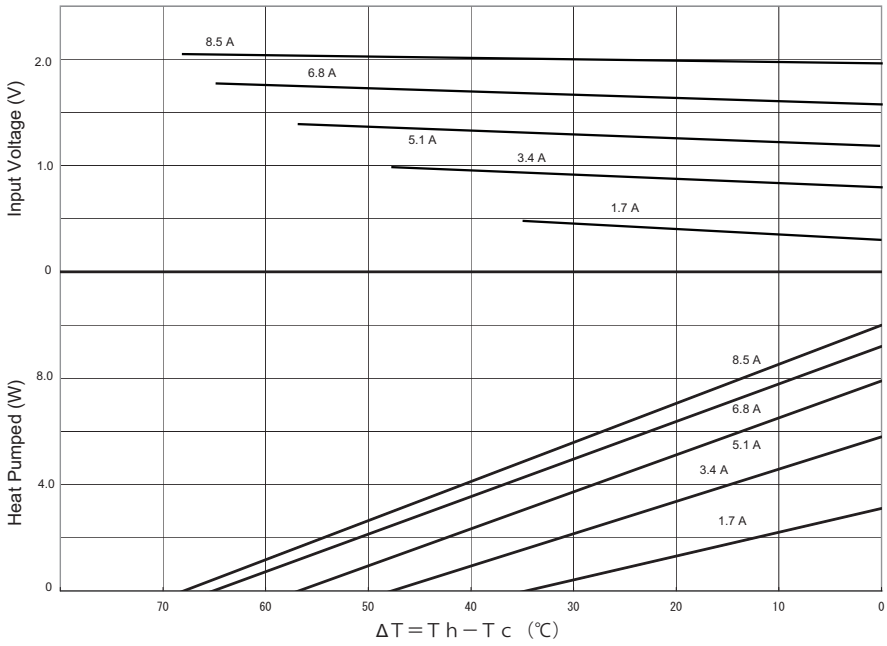


Figure 3.5: CUI CP85138 TEG performance.

ting both sides of the TEG reach different temperatures will create an electrical signal, which can be used with an energy harvesting circuit to power a useful system. In modern TEG design, n- and p-type silicon can be used to create electrical power from a temperature difference.

Fig. 3.4 shows the internals of the CP85-series thermoelectric generators from CUI [6]. Depending on the voltage and amount of current applied to the TEG, the temperature difference of the TEG can be controlled [7] as shown in Fig. 3.5. While this figure shows the situation when power is applied to the Peltier cooler in order to change the temperature, the opposite is also true and using the TEG as a power source will work as long as there is a temperature difference across both sensor terminals. Although the value is not shown explicitly in Fig. 3.5, operating the TEG with a small temperature difference is able to generate a small voltage (ca. 500 mV) with a fairly large current.

The output of a thermoelectric transducer is a DC voltage, which simplifies the design in creating power management circuits that are capable of driving a realistic and useful load. A number of prior works [8–11] , all of which aim to lower the minimum voltage at which the power converter can operate. A detailed description of each of these circuits will be presented in Section 4.3

The output voltage of a TEG seems to vary greatly based on the materials used and the number of devices (or semiconductor voltage generators) placed together in series or parallel. Some transducers have an output voltage in the range of 5 mV / °C [8], while others generate a voltage of several hundred millivolts even with a small

temperature difference [7]. In general, power converters that are designed to work from a TEG input are optimized to startup with the lowest voltage possible, and the minimum input voltage is an important figure of merit for the converter.

3.2.3 *Photovoltaic Transducers*

Photovoltaic transducers (commonly referred to as *solar cells* when used outdoors) are becoming widely used in higher-power applications such as residential power and solar-field power plants. But photovoltaics can also be used to scavenge the energy produced by indoor lighting, similar to solar-powered calculators.

Unfortunately, the output voltage of a photovoltaic transducer changes based on the output current as shown in Fig. 3.6. For a photovoltaic cell, there is a point where the power from the transducer is optimized. Modern approaches seek to find this Maximum Power Point (MPP) using a Maximum Power Point Tracking (MPPT) approach. MPPT attempts to disturb the input in some way and watch the reaction. By iterating this process over a range of conditions, the circuit can find the maximum power point. Additionally, since the sun doesn't always shine (and most indoor lights aren't always on), some type of energy storage device is required to store the captured energy.

There have been some recent advances in power converters that operate with a photovoltaic input [13]. A detailed description of this circuit will be presented in Section 4.4.

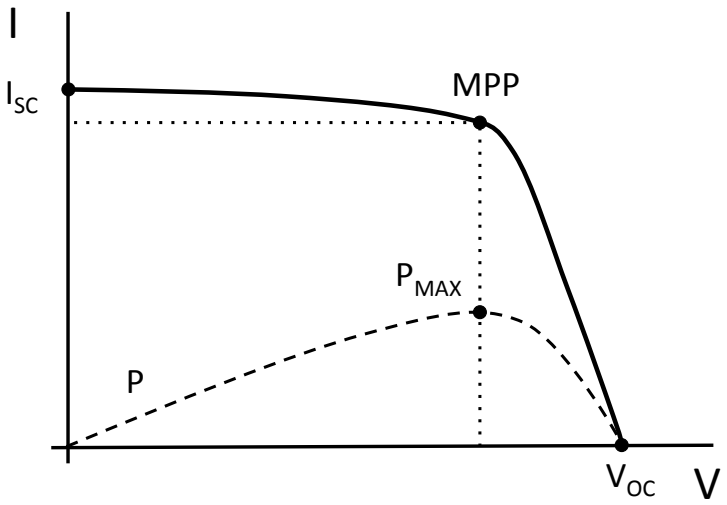


Figure 3.6: Typical photovoltaic cell I-V characteristic.

4

PREVIOUS WORKS RELATED TO ENERGY HARVESTING POWER CONVERSION

4.1 INTRODUCTION

The transducers introduced in Ch. 3 produce different kinds of signals at their outputs—piezoelectric generators produce AC signals, while TEGs and photovoltaic transducers produce DC signals. In all of these cases, the output from the transducer must be converted to a different voltage that will be useful for powering a low-power system or charging an energy storage device, like in Fig. 3.1.

The following sections introduce some previous approaches to power management circuits for energy harvesting technology. Since the topology of the power conversion circuit depends greatly on the type of input source, these explanations are separated by the type of input transducer.

4.2 POWER CONVERTERS FOR PIEZOELECTRIC GENERATORS

Since piezoelectric generators create an AC signal, most power management approaches rectify this signal to DC in order to charge a battery. The following sub-sections introduce some of the approaches taken by others with regards to piezoelectric transducers.

4.2.1 *Kwon, D., Rincon-Mora, G.* A single-inductor ac-dc piezoelectric energy-harvester/battery-charger ic converting $\pm$(0.35 to 1.2v) to (2.7 to 4.5v)

A block diagram of [2] in shown in Fig. 4.1. Since this circuit uses a piezoelectric input, the input signal is AC and and output signal is a DC battery that is charged from the small amount of power that is captured from the input vibrational source.

This circuit works by sensing the peak voltage of the input source to know when the piezoelectric transducer has stored a maximum amount of energy in equivalent capacitor C_{PZT}. This then causes the circuit to control switches S_I and S_N in order to transfer energy from the input transducer to the output inductor L_H. The circuit then waits for a variable yet programmed delay to ensure that the maximum amount of energy from the input source is stored in the output inductor L_H. Once the timer has ended, L_H is de-energized through a switch and an active diode: if the input signal is positive, the inductor is discharged through active diode M_{P1} and switch S_I, while if

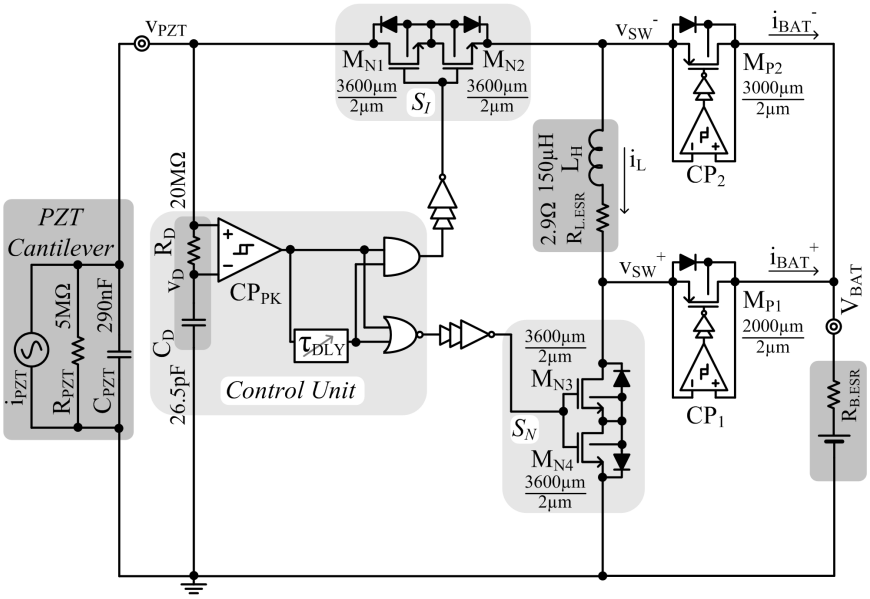


Figure 4.1: Block diagram of piezoelectric energy harvester in [2].

the input signal is negative, the inductor is discharged through active diode M_{P2} and switch S_N.

4.2.1.1 *Drawbacks*

While this paper shows an interesting way of harvesting energy from a vibrational transducer, there are a number of drawbacks:

1. Low efficiency (49.9% max)
2. Requires external 4 V source for bias
3. Requires external -2 V source for peak detection circuit

4.2.2 *Ramadass, Y., Chandrakasan, A.* An efficient piezoelectric energy-harvesting interface circuit using a bias-flip rectifier and shared inductor

The approach in [3] uses a bias-flip architecture to increase the amount of energy that can be harvested from the AC piezoelectric input. Fig. 4.2 shows the bias-flip rectifier used in this paper. Turning the inductor on when the transducer voltage crosses zero causes the voltage across the transducer V_{BF} to quickly jump to $\pm V_{RECT}$. This in turn makes it possible for the rectifier to transfer energy from the input source for a longer period of time compared to using a conventional rectifier (even if the diodes were ideal).

However, in order for this approach to work properly, the voltage V_{RECT} itself must be regulated in order for the circuit to function

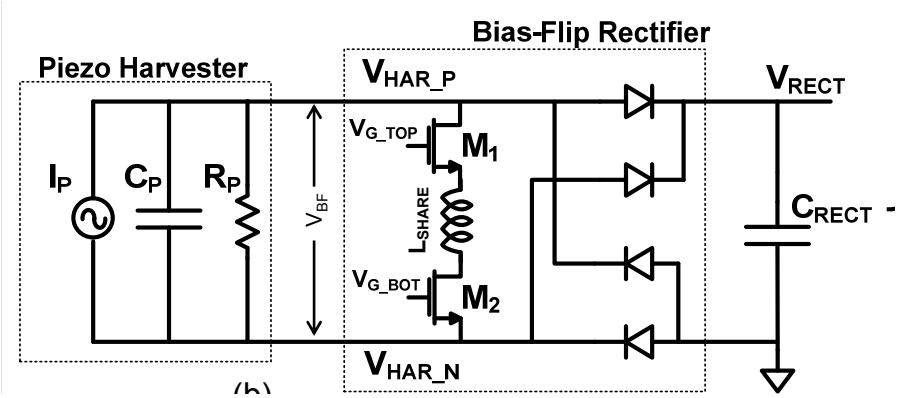


Figure 4.2: Bias-flip rectifier block diagram from [3].

properly. A block diagram of the entire system is shown in Fig. 4.3. A buck regulator is used to regulate V_{RECT} and to store the captured energy onto output storage capacitor C_{STO}. A boost converter is used to create a high voltage in order to power the switches of the bias-flip rectifier. Both the buck and boost converters require an inductor to operate, and a single inductor is shared between 3 blocks: the bias-flip rectifier, the buck converter and the boost converter. An intelligent control scheme is implemented in order to share the inductor current between these 3 blocks.

4.2.2.1 *Drawbacks*

While this paper shows an impressive way of increasing the amount of energy that can be harvested from an AC source by using the bias-flip rectifier technique, it still suffers from several drawbacks:

1. Maximum output power is very low (60 μW)
2. Requires storage device to hold bias voltage

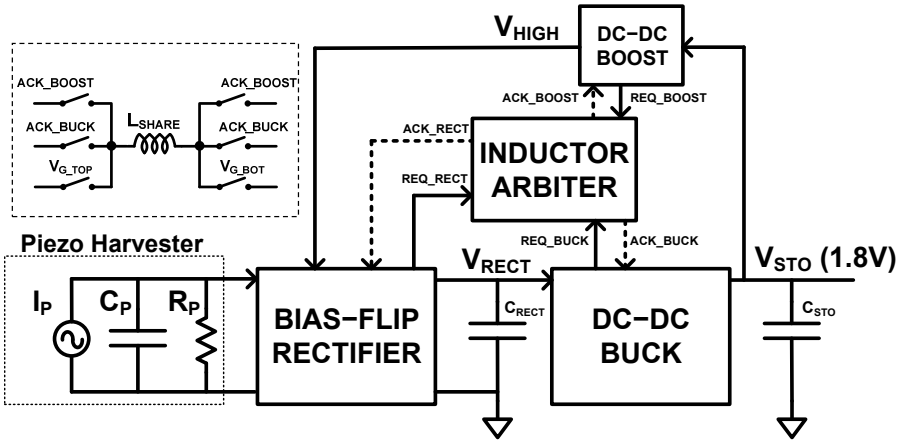


Figure 4.3: Full block diagram from [3].

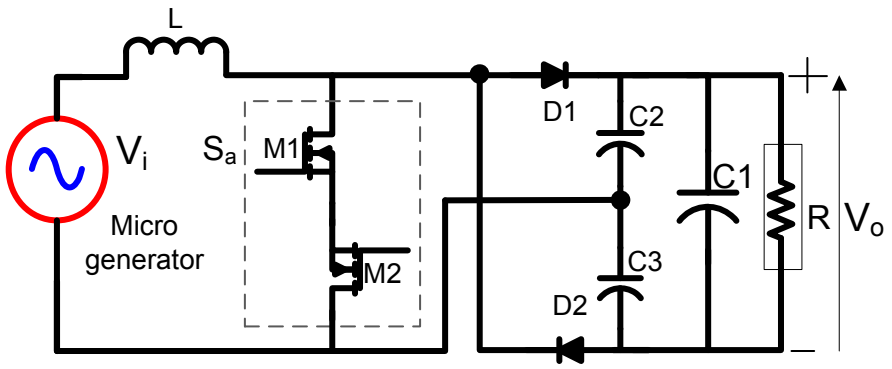


Figure 4.4: Split-capacitor based AC-DC converter from [4].

3. Complicated design with many switches

4.2.3 *Dayal, R., Parsa, L.* Low power implementation of maximum energy harvesting scheme for vibration-based electromagnetic microgenerators

While Maximum Power Point Tracking (MPPT) techniques are most commonly seen with photovoltaic transducers, [4] introduces a way to maximize the energy harvested from a piezoelectric transducer. A simple block diagram of the circuit is shown in Fig. 4.4.

The circuit uses a split-capacitor based AC to DC boost converter that converts the small AC input signal to a larger DC output voltage during both half-cycles. The converter is operated in DCM with a fixed duty cycle. While most MPPT approaches require a sophisticated algorithm to perturb the input and measure the output result, this paper uses the much simpler scheme shown in Fig. 4.5.

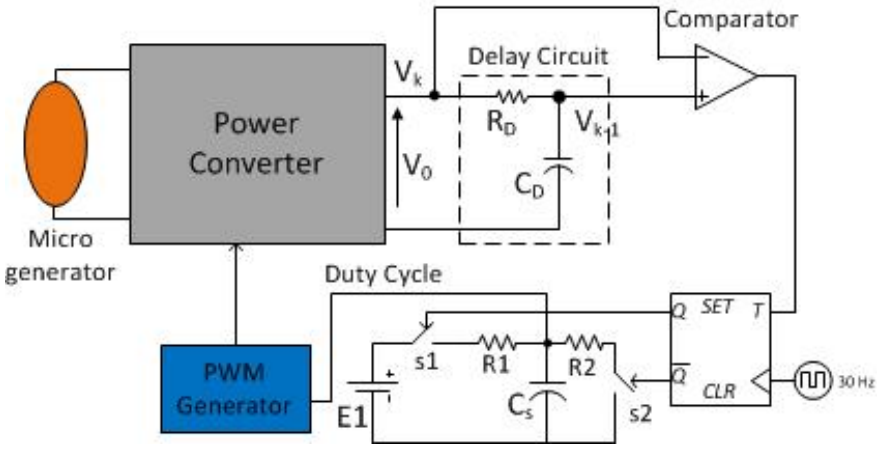


Figure 4.5: Maximum energy harvesting scheme from [4].

By changing the duty cycle of the DCM controller and observing the change in the output voltage, this circuit implements a poor man's MPPT type of control, without requiring sophisticated computations. This paper also explains that this technique could likely be adapted to other types of energy harvesting, but does not give details on how exactly they would be implemented.

4.2.3.1 *Drawbacks*

Since this paper's focus is mostly on maximizing the power that can be drawn from the input source, there are a number of drawbacks:

1. Maximum efficiency is not presented
2. Minimum input voltage is not presented
3. Requires a large number of external components

4.2.4 *Rao, Y., Arnold, D.* Input-powered energy harvesting interface circuits with zero standby power

While most energy harvesting circuits create a large output from a small input voltage and use this higher voltage to bias control circuitry, the circuit in [5] uses only the input voltage to bias control circuits. The argument is that if the output voltage is used, there will be some non-zero power draw as long as the circuit is active, even if the input source is too small to make the circuit operate. Since it is optimized for vibrational energy harvesting, this paper uses an AC/DC converter that connects to a DC/DC converter to regulate the output load. A block diagram of this circuit is shown in Fig. 4.6.

The AC/DC portion of the circuit is implemented using two stages—a full-wave rectifier and an active diode. The rectifier is implemented using a MOSFET H-bridge as shown in Fig. 4.7. The MOSFETs are implemented with a fairly large size (W/L ratio of 750 μm/1 μm) and this block is the rate-limiting step in terms of starting up the circuit.

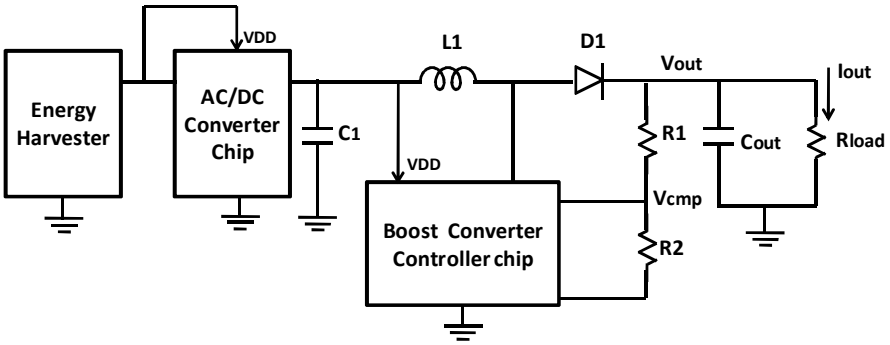


Figure 4.6: Complete energy harvesting interface circuit from [5].

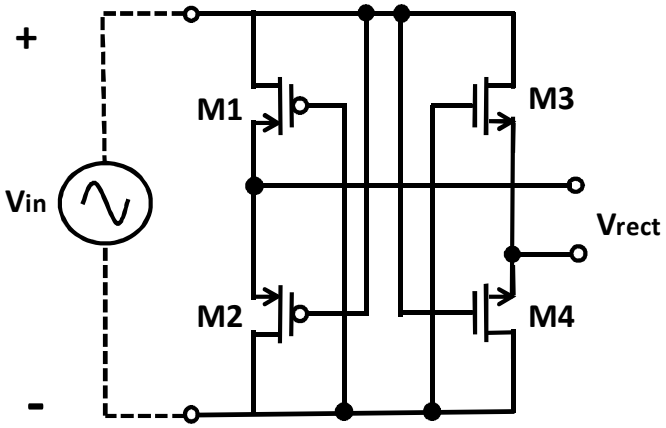


Figure 4.7: MOSFET full-wave rectifier in [5].

If the input voltage is higher than the transistor V_t (which is stated as 0.6 V), then the rectifier will operate and power can flow to the subsequent blocks.

The rectifier is then connected to the active diode, which is essentially a comparator connected to a very large PMOS (W/L ratio is 1500 μm/1 μm). The full wave rectifier and active diode complete the AC to DC conversion in this circuit. The DC output from these blocks is then fed to a simple asynchronous DC-DC Boost converter.

The DC-DC converter is a boost converter that is entirely driven from the input voltage, where the input voltage is the output from the AC/DC converter stage. This boost converter uses a hysteretic control scheme in order to save power, though the use of a diode instead of a synchronous switch likely accounts for the converter having such low efficiency.

4.2.4.1 *Drawbacks*

While the published paper shows an interesting way of converting an AC piezoelectric signal to a stable output voltage while only biasing from the input voltage, there are a number of drawbacks with this approach:

1. Low efficiency (60% max)
2. Low maximum load (3.9mW)
3. Minimum input voltage is very high
4. Many external components (Schottky diode, 2 output capacitors, 3 feedback resistors)

4.3 POWER CONVERTERS FOR THERMOELECTRIC GENERATORS

With a Thermoelectric Generator (TEG) as the input source, the input voltage is generally very low, but adding a number of transducers in parallel can greatly increase the amount of current that is available for harvesting. For example, the transducer introduced in [7] can create a current up to 8.5 A at 2.0 V, while the transducer used in [8] has an output voltage of about 5 mV / °C, and an output current in the μA range.

All power converters that use a TEG input require a large amount of gain to boost the DC input voltage to a usable output value (usually about 1 V DC). While inductor based boost converters are commonly used, voltage multiplying switched capacitor converters are also used in some works.

4.3.1 *Carlson, E., Strunz, K., Otis, B.* A 20 mv input boost converter with efficient digital control for thermoelectric energy harvesting

By using a fairly typical boost converter running in DCM, [8] proposes a converter that can take a TEG input down to a voltage of 20 mV while creating a 1 V output voltage. A block diagram of the circuit is shown in Fig. 4.8.

Exploiting the fact that a synchronous boost topology (like that shown in Fig. 2.11) will have lower power loss, this circuit uses a Pulse Frequency Modulation (PFM) (or hysteretic) type of control scheme to reduce power loss, enabling a voltage gain of 50 V/V. Since the control loop uses a variable-time one-shot and relies on the inductor current zero cross point, the control scheme is a kind of adaptive

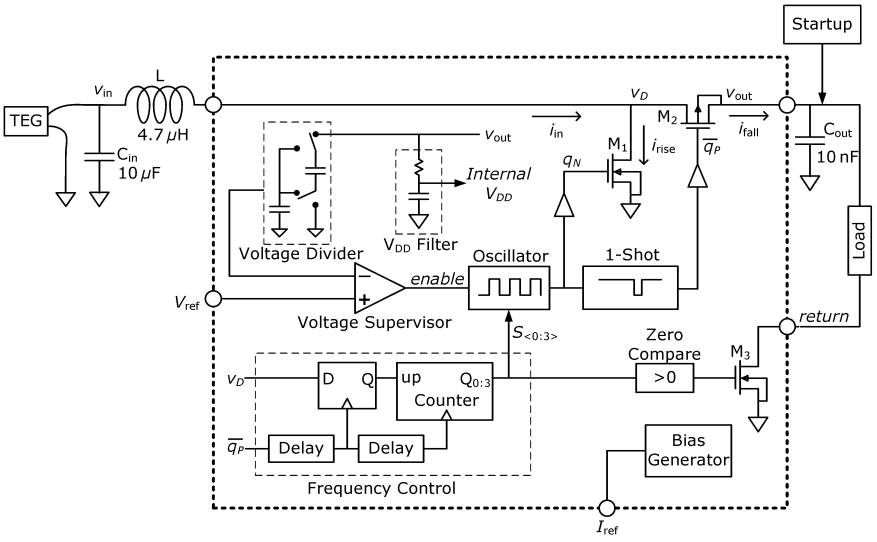


Figure 4.8: Block diagram of boost converter used in [8].

constant on time style hysteretic control scheme. The paper describes the design of the one-shot and inductor zero cross in great detail.

Closed-loop regulation is performed by using a scaled version of the output voltage which is then fed to the *Voltage Supervisor* comparator. In an effort to reduce power loss, output voltage scaling is performed by using a switched capacitor voltage divider—when this circuit is not switching, its static power loss is zero. The bias for this circuit is provided externally: both the reference voltage and an external bias current.

The startup mechanism for this circuit requires an external voltage source to charge the output capacitor. Internal circuitry cannot be properly biased, and hence the circuit will not operate unless the output voltage is pre-charged to at least 600 mV.

With an input voltage of 100 mV and an output voltage of 1.0 V (i.e. voltage gain of 10 V/V), this circuit can achieve a maximum efficiency of 75% and deliver a maximum load of 176 μW. The circuit was also tested with a real TEG input. With an input voltage of 34 mV, the converter was able to generate 34 μW at 1 V.

4.3.1.1 *Drawbacks*

While this circuit introduces an interesting way to convert the energy generated from a very low voltage TEG source, there are some significant drawbacks:

1. Low peak efficiency (75%)
2. Low maximum load (176 μW)
3. Requires external bias generator
4. Requires external reference voltage
5. Requires external 600 mV source for circuit startup

4.3.2 *Ramadass, Y., Chandrakasan, A.* A batteryless thermoelectric energy-harvesting interface circuit with 35mv startup voltage

With an eye on using a TEG that is worn on the body and only has a temperature difference of a few kelvins, [9] introduces a power converter that does not require a battery for energy storage. The block diagram of this circuit is shown in Fig. 4.9, which utilizes the startup circuit shown in Fig. 4.10 in creating an output voltage of 1.8 V.

The startup of this circuit relies on a mechanical switch, labelled S_1 in Fig. 4.10, and implemented using a MEMS device that responds to motion of the human body. By moving the MEMS device, switch S_1 will be turned on and off. Turning on this switch will build up energy in the startup inductor L_{START}, while turning off the switch

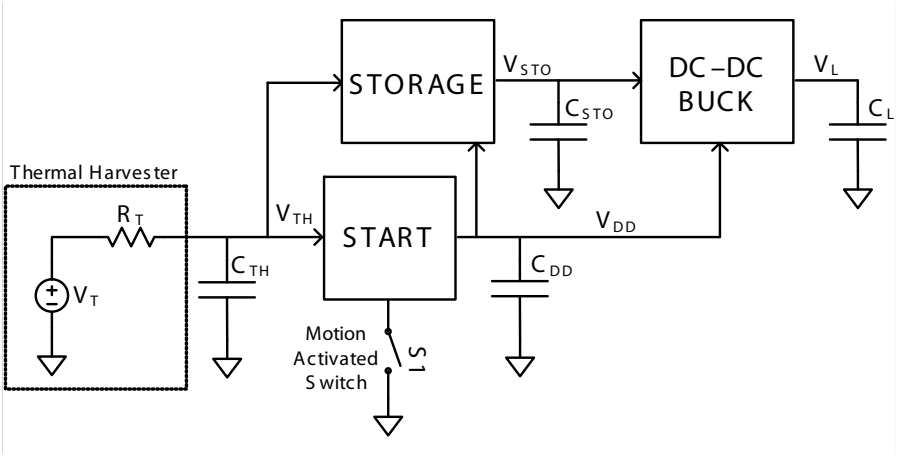


Figure 4.9: Block diagram of circuit used in [9].

will cause the stored energy to flow to the on-chip storage capacitor C_{DD} through the MOS diode M_1.

Since the startup circuit used in this paper is a basic boost converter, continuously commutating the mechanical switch will cause the output voltage stored on C_{DD} to continuously rise. Once this startup voltage, V_{DD} has risen to 1.0 V, the internal circuits can be properly biased and hence the closed-loop regulator can function. Once the regulator's clocks, reference voltage and other internal circuitry have finished start-up, the voltage stored on V_{DD} is then diverted to the

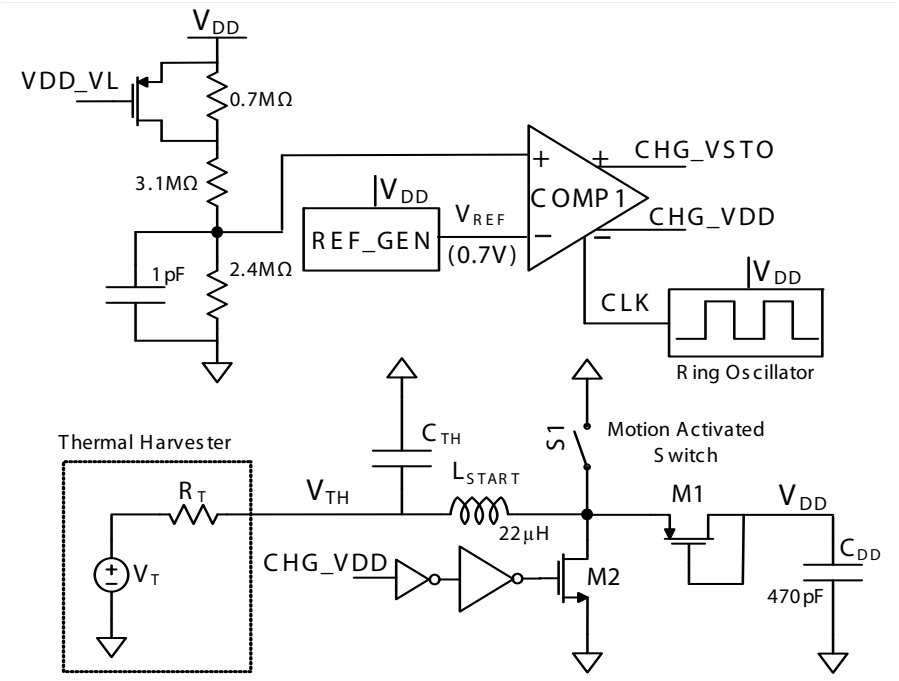


Figure 4.10: Startup circuit used in [9].

storage capacitor C_{STO}. When the voltage of V_{STO} is above 2.4 V, the DC-DC buck regulator is enabled to create a regulated output of 1.8 V.

The STORAGE block shown in Fig. 4.9 is a basic boost converter as shown in Fig. 4.11. By using a synchronous switch topology and Zero Current Switching (ZCS) control, this block can efficiently transfer energy harvested from the MEMS switch to the storage capacitor.

When the storage voltage is greater than 2.4 V, the DC-DC buck converter operates to regulate the output voltage at 1.8 V. This buck converter is a synchronous circuit with hysteretic control, both of which help to improve the efficiency of this block.

This paper mentions a system efficiency of 58%, with the maximum amount of power available to the load at a little less than 300 μW. The system was tested with a real TEG which provides a voltage of 25 mV / K based on the temperature difference.

4.3.2.1 *Drawbacks*

While this paper presents an interesting way to harvest energy from a TEG source, there are some inescapable drawbacks, chief among them the requirement of a mechanical switch:

1. Low efficiency (58%)
2. Low maximum load (<300 μW)
3. Requires a mechanical switch for startup
4. Requires a large number of external components: 3 inductors, storage capacitors, etc.
5. Complicated design with 3 switching regulators

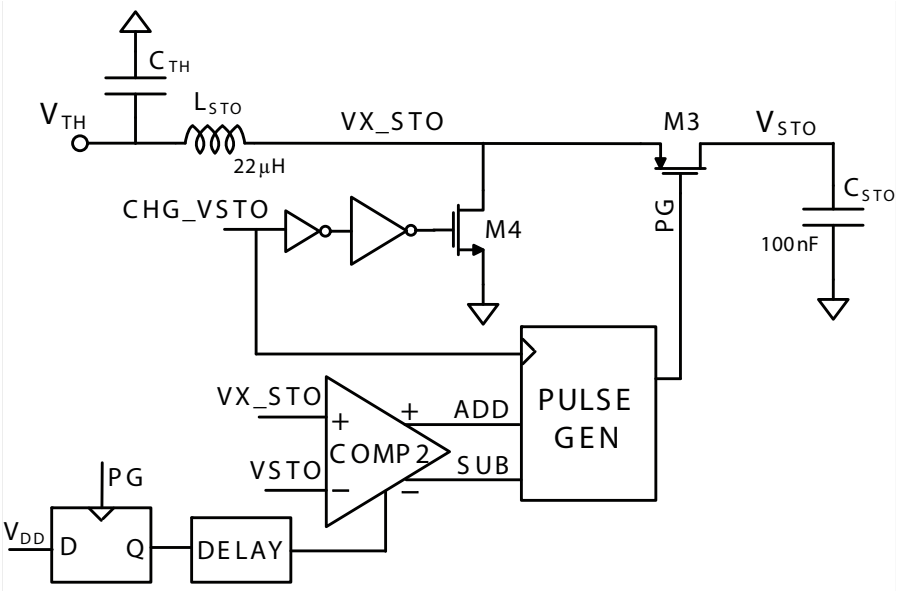


Figure 4.11: Energy storage circuit used in [9].

4.3.3 *Doms, I., Merken, P., Mertens, R., Van Hoof, C.* Integrated capacitive power-management circuit for thermal harvesters with output power 10 to 1000μW

Unlike other TEG approaches that use a magnetic switching converter topology (i. e. the converter uses an inductor), [10] uses a switched-capacitor architecture to boost up the voltage from a TEG input. A block diagram of the proposed circuit is shown in Fig. 4.12, where the shaded part of the figure is the power management circuit.

Based on the number of gain stages used in the switched-capacitor design, the output voltage will follow the characteristic of

$$V_{out} = (M+1)\,(V_{in} - V_d) - \frac{MI_{out}}{fC}, \tag{4.1}$$

where M is the number of charge pump stages, C is the switching capacitance size, V_d is the voltage drop across the switches and f is the switching frequency.

Similarly, the total system efficiency for this circuit was calculated as

$$\eta_{total} = \frac{4R_{TEG}V_{out}}{V_{open}^2} \frac{(M+1)V_{open} - (1+\alpha CfMR_{TEG})\,V_{out}}{(M+1)^2R_{TEG} + (1+\alpha CfMR_{TEG})\,\frac{M}{Cf}}. \tag{4.2}$$

In (4.2), α is the ratio of parasitic capacitances to switching capacitances (whose value is reported as 0.03 for the process used), R_{TEG} is the series resistance of the TEG and V_{open} is the voltage across the TEG.

For a switched-capacitor converter, the ratio of parasitic capacitors, number of gain stages, storage capacitor size and switching frequency

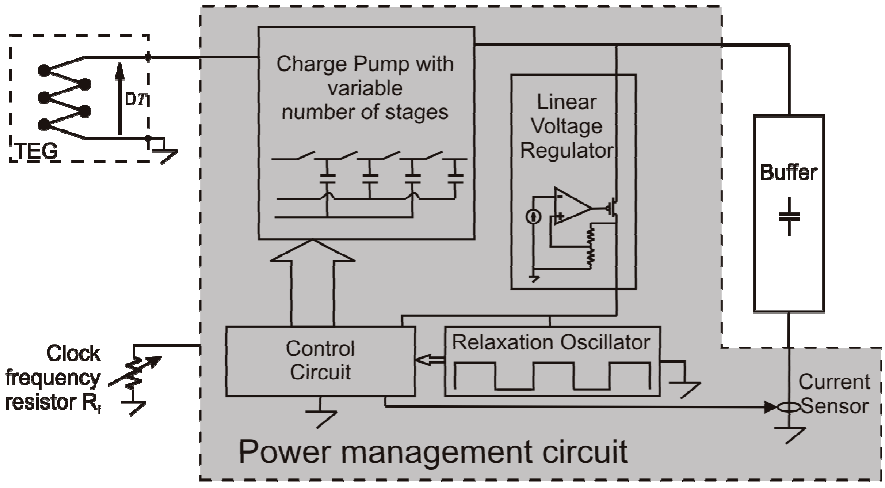


Figure 4.12: Block diagram of the circuit presented in [10].

have a large effect on the amount of power that the circuit can deliver to the load. Consequently, these parameters also have a large effect on the total circuit efficiency, as shown in (4.2).

Since the maximum deliverable power depends both on the number of gain stages and the switching frequency, this chip was designed to first fix the number of gain stages, then change the chip frequency to optimize the efficiency. This is accomplished by using an external resistance to change the switching frequency.

This chip was fabricated with very large on-chip Metal Insulator Metal Capacitors (MIMCAPs) ($C = 2.45$ nF) and was tested with a TEG with an impedance of $R_{TEG} = 11$ kΩ. With these values, this circuit reached a peak efficiency of 70% while being able to drive a load up to 1 mW.

4.3.3.1 *Drawbacks*

While this paper presents an interesting way to convert the power from a TEG using a switched-capacitor topology, there are a number of drawbacks to this design:

1. Low peak efficiency (70%)
2. Low maximum load (1 mW)
3. High minimum input voltage (600 mV)
4. Clock frequency controlled externally

4.3.4 *Linear Technology* Ultralow voltage step-up converter and power manager (LTC3108)

There are also some commercially available energy harvesting circuits on the market, like the LTC3108 circuit from Linear Technology Corporation [11]. While the LTC3108 is a general-purpose energy harvesting circuit, it is commonly used with a TEG input, as shown in the typical circuit setup in Fig. 4.13. In this application, a TEG with a voltage as low as 20 mV charges a supercapacitor ($C = 100$ mF), which then powers a low-power load (MCU, transceiver, RF link, etc). The load is assumed to be OFF for a certain amount of time, so that the harvesting source can store charge on the storage capacitor when the load current is low, then transfer stored charge from the storage capacitor to the output load when the load circuitry is active.

The LTC3108 circuit uses a step-up transformer with a high turns ratio (typically 1:100) that helps boost up the input voltage. The inductance of the transformer secondary winding resonates with capacitor C_2 to create an AC signal at the secondary side of the transformer. This AC signal then goes through charge pump capacitor C_1 and an internal rectifier to create a stable DC voltage inside the chip. A block

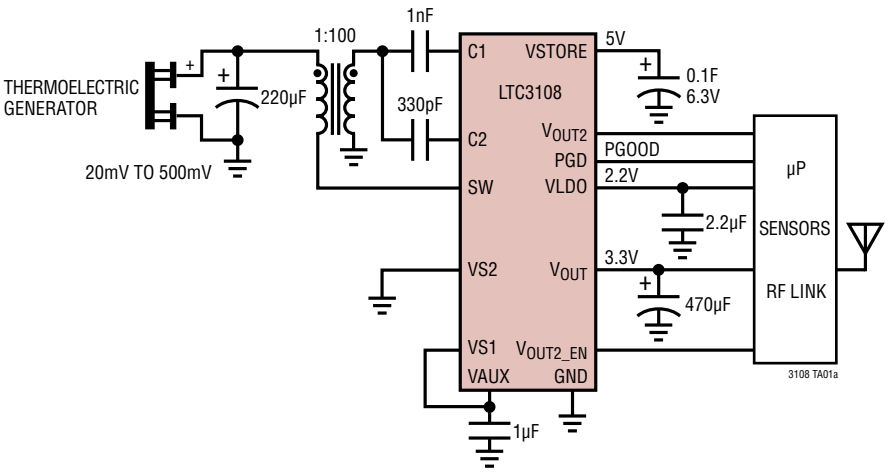


Figure 4.13: Block diagram of LTC3108 energy harvester in a TEG application.

diagram of the internal circuitry used in the LTC3108 is shown in Fig. 4.14.

The signal rectified from the AC input is stored at node VAUX, which is a DC voltage and is used to bias the internal circuitry. The value of the voltage VAUX determines whether the converter begins functioning—once VAUX exceeds 2 V, the synchronous rectifiers inside the chip begin to function and the AC to DC conversion is greatly improved, effectively raising the value of VAUX. Since VAUX is used

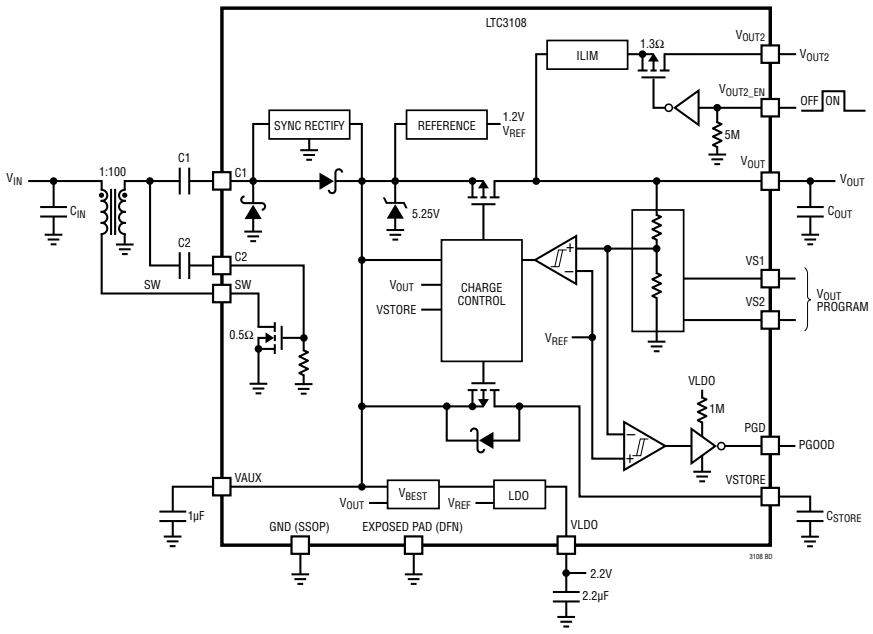


Figure 4.14: Internal circuitry of the LTC3108 energy harvester.

to bias the internal control circuitry, its value is clamped to 5.25 V using a shunt reference.

Output regulation for the LTC3108 is implemented using a programmable linear regulator, using VAUX as the input voltage. Depending on the settings on pins VS1 and VS2, the output voltage can be set to a constant voltage between 2.35 V and 5 V. Internal feedback resistors connect to an opamp that modulates the gate of a large PMOS transistor in order to keep the output voltage stable.

Like most commercial parts, the LTC3108 chip includes a number of additional features (power good signal, separate internal LDO, etc) but their details are beyond the scope of this manuscript.

4.3.4.1 *Drawbacks*

While the LTC3108 introduces an interesting way of boosting a DC input voltage to a larger AC signal, rectifying back to DC and conditioning through a linear regulator, there are a number of drawbacks with this approach:

1. Low peak efficiency (65%)
2. Large number of external components (transformer, capacitors)
3. Best performance with a huge storage capacitor and large transformer

4.3.5 *Chen, P.H., Ishida, K., Zhang, X., Okuma, Y., Ryu, Y., Takamiya, M., Sakurai, T.* 0.18-v input charge pump with forward body biasing in startup circuit using 65nm cmos

A hybrid approach to energy harvesting, using both a switched-capacitor charge pump for startup and a switching regulator for high-efficiency regulation is introduced in [12]. This circuit uses a 3-stage Dickson charge pump like the conceptual circuit shown in Fig. 4.15. Although this circuit works fine when all components are ideal, the body effect

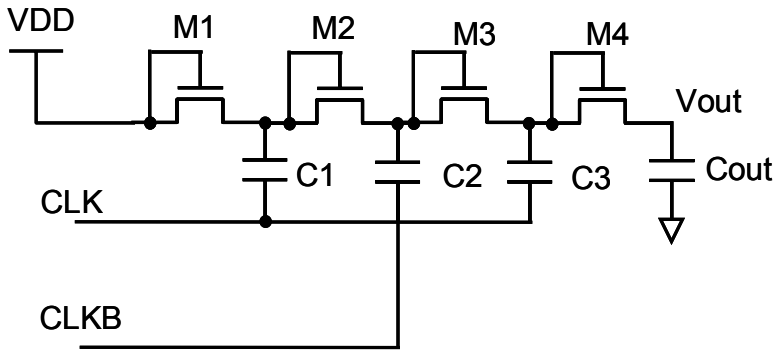


Figure 4.15: Three-stage Dickson type charge pump.

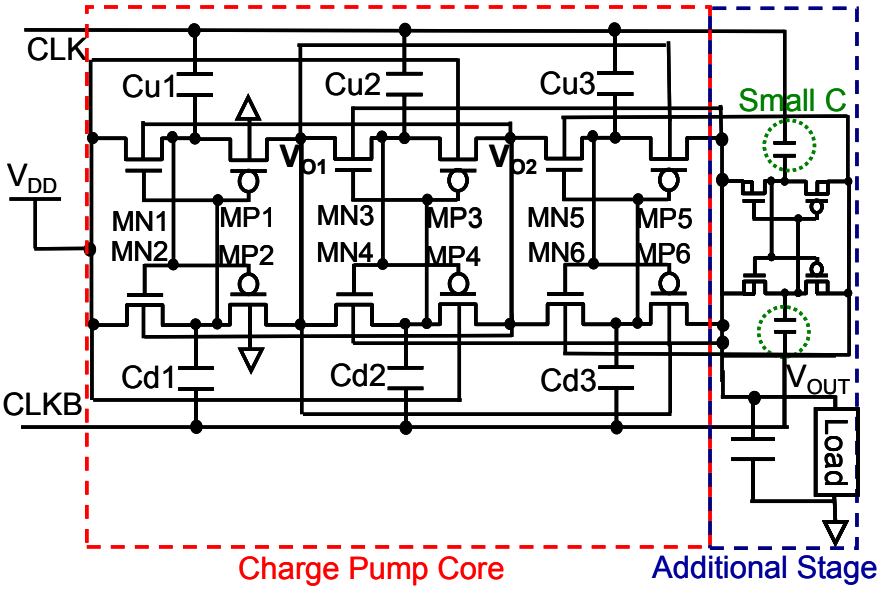


Figure 4.16: Charge pump with forward body bias from [12].

of the NMOS transistors can cause the threshold to increase on each diode-connected device, thereby lowering the gain of the circuit.

In order to address this body effect limitation, the body of each NMOS is biased from the output of the previous charge pump stage as shown in Fig. 4.16. This approach lowers the effective threshold voltage of each NMOS, thereby increasing the gain and reducing the minimum input voltage for this charge pump circuit. Note that this approach requires isolated deep n-well NMOS devices, which are not always available in standard CMOS processes.

The output of the charge pump circuit then connects into a clock generator and high duty-cycle generating circuit, which finally connects to a boost regulator, as shown in Fig. 4.17. By using this hybrid approach, a very low input voltage will start up the charge pump which can then be used to bootstrap the startup of a boost regulator. Since the boost regulator will likely have a higher efficiency than a switched-capacitor circuit, this approach can realize both the advantages of low input voltage and high efficiency.

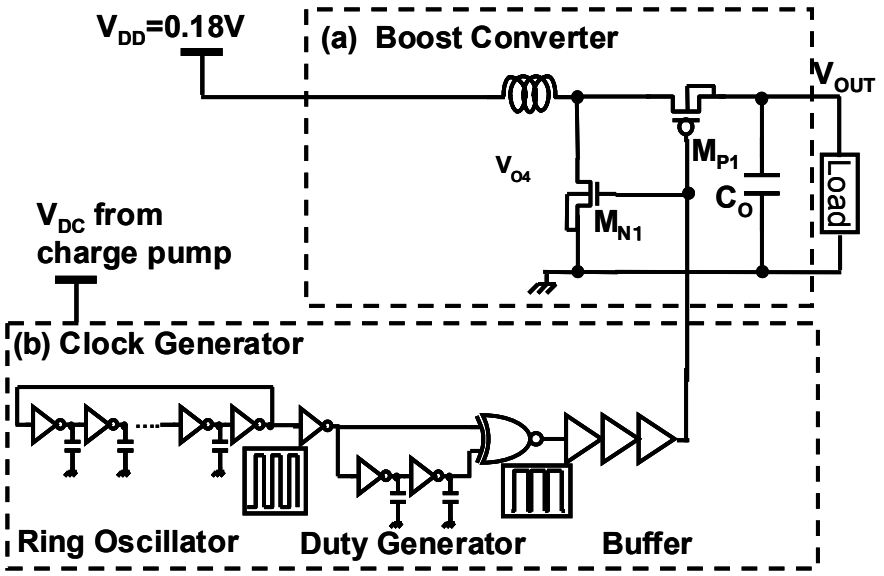


Figure 4.17: Block diagram of the boost regulator in [12].

4.3.5.1 *Drawbacks*

Although this paper presents an interesting hybrid switched capacitor and boost regulator approach to regulating an energy harvesting input, there are a few drawbacks:

1. Efficiency is not presented
2. Requires deep n-well isolated NMOS transistors
3. Requires external clock generator for charge pump
4. Boost regulator output is unregulated (fixed duty cycle)

4.4 POWER CONVERTERS FOR PHOTOVOLTAIC TRANSDUCERS

4.4.1 *Chew, K.W.R., Sun, Z., Tang, H., Siek, L.* A 400nW single-inductor dual-input-tri-output DC-DC buck-boost converter with maximum power point tracking for indoor photovoltaic energy harvesting

Recall from Sec. 3.2.3 that a photovoltaic transducer has a maximum power point, and a good design will track this point to maximize the energy collected from the photovoltaic input. Additionally, the input energy source is not always present (i.e. the sun doesn't always shine, indoor lights aren't always on, etc.), hence some type of energy storage device is necessary to store the harvested energy.

The circuit in [13] shows a unique approach of addressing these problems. The target application is an image sensor with a voltage of

1.8 V, but 1.0 V is also generated to power the internal digital circuitry, citing that using a lower voltage for digital circuitry will save power. Additionally, the input can be either the photovoltaic scavenger or the battery voltage. The system block diagram of this approach is shown in Fig. 4.18.

In order to supply the 1.0 V and 1.8 V output voltages, this circuit uses a single inductor with a buck-boost converter and converts the outputs using both pulse-skipping modulation and constant-on time PFM control. A sophisticated digital control scheme requiring only a signal comparator is implemented in order to drive the appropriate output at the appropriate time.

To save power, the control circuits are disabled most of the time. A very low frequency clock (312 Hz, labelled SYS_CLK) wakes up the circuit. Once the bandgap voltage has stabilized, the input and two output voltages are evaluated with the comparator. Based on this calculation, the system can tell if the input source is large enough, and power can flow to the outputs that need it.

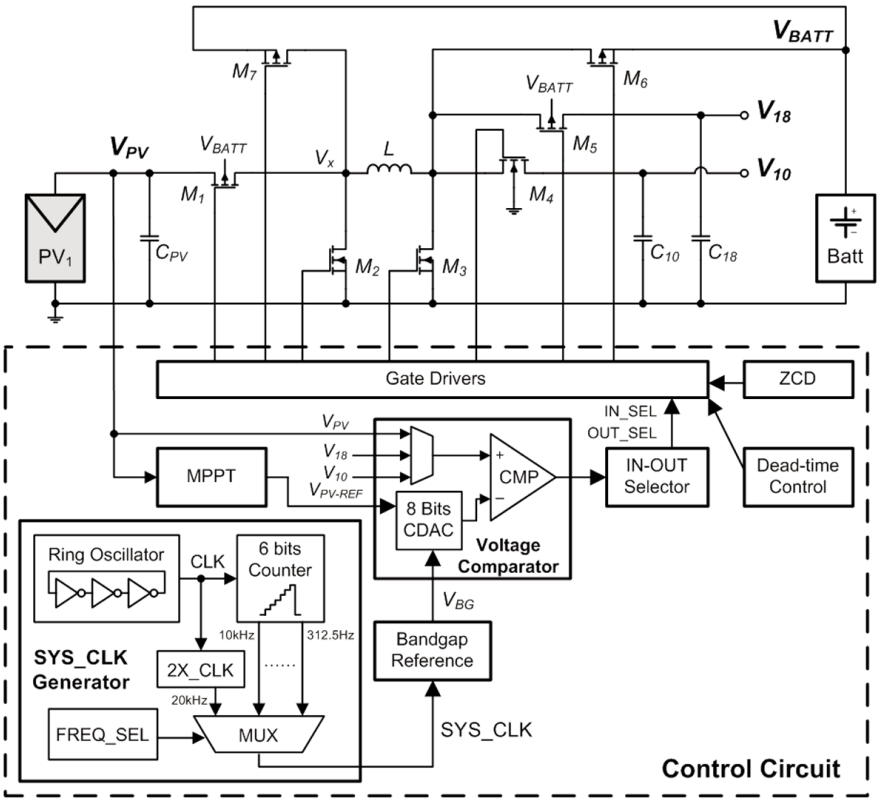


Figure 4.18: Photovoltaic energy harvesting block diagram from [13].

4.4.1.1 *Drawbacks*

While this paper introduces an interesting way to harvest energy from micro-solar sources, there are some drawbacks to this approach:

1. Requires battery for energy storage
2. Low peak efficiency (83%)
3. Switching in the audio range (<20 kHz) which likely produces audible noise

4.5 FUTURE PROSPECTS FOR ENERGY HARVESTING POWER MANAGEMENT CIRCUITS

This chapter introduced some approaches others have made in the area of energy harvesting power management. Even as transducers and power management circuits advance, the greatest challenge for energy harvesting is in the adoption of energy harvesting systems into commercial products.

While there are an increasing number of commercial chips on the market, it has been difficult to convince companies that energy harvesting can save money or replace other powering systems in their current devices. In some systems, the amount of energy that can be harvested from a transducer is much too small to adequately power the system (or charge the necessary energy storage components). In other cases, the prospect of removing a battery doesn't justify the cost or complexity of moving to an energy harvesting solution.

Because of these drawbacks, companies and researchers need to work more closely with companies that could use energy harvesting electronics—both understanding the power requirements for their systems and the cost/complexity of the system they could handle. Initial reports are that the power generated from energy harvesting transducers are too low to ever power useful systems like smartphones or embedded medical devices. But there are other systems like remote sensor networks that should be able to function from an extremely low power input source.

By targeting customers directly and understanding their specific needs and expectations, energy harvesting will have a better chance to grow and improve in the future. Unfortunately in the current environment, there is no *killer app* for energy harvesting circuits. Thus, while research will continue inside the ivory tower of academia, there will not be widespread use of energy harvesting products until customers are shown exactly how they can be used in a simple, cost-effective manner.

5

A FULLY INTEGRATED SINGLE SUPPLY BOOTSTRAPPED BOOST REGULATOR FOR ENERGY HARVESTING APPLICATIONS

5.1 INTRODUCTION

As introduced in Ch. 4, there have been great advances in the realm of Energy Harvesting. Using vibrational, thermal and solar transducers, small amounts of power can be captured by latent energy sources [2–5, 8–12]. While previous works have shown that capturing power from these micro-power sources is feasible, each approach has drawbacks. Some approaches require an external battery [2] or a storage capacitor [3] with a voltage of several volts to bias the control circuitry. Others have designed their circuits with external bias circuitry [8] or require a mechanical switch in order to start up the converter [9]. Furthermore, previous works also are not suitable to drive realistic loads, as their maximum load capability is in the μW range [2–4, 8–10]. In real-world applications, where energy harvesters are used in hard-to-reach places, it would be impractical to replace the batteries used in these systems. Additionally, since a typical low-power microcontroller requires several mW of power to operate, conventional circuits are unsuitable for real-world applications.

In order to address these issues, I have created a low-power boost converter that is only operational when its input source is large enough to bootstrap the system. My circuit is also optimized to provide several mW of power, which would be suitable to drive a low-power MCU. Additionally, as previous papers only briefly mention total system efficiency, my circuit is designed to maximize efficiency, which, in a real-world application, would increase the maximum amount of energy that is available to the load. While there are a number of boost regulators on the market that can start up with a low input voltage [11, 14], these parts have very low efficiency (<40%) in the 1 mW output load range and some require a large number of external components [11]. Since energy harvesting inputs like thermal transducers only output a small amount of power, it is critical to optimize energy harvesting power electronics at a lower load range.

This chapter introduces a regulator that is able to start up with an input voltage of 240 mV, and can supply up to 6.2 mW of power with a maximum efficiency of 97%. With my approach, these results are achieved with only 3 external components—an input capacitor, an output capacitor, and an inductor. The feasibility of my approach is

shown both from Spectre simulation results and a test chip used to verify the operation of the internal charge pump circuit.

5.2 PROPOSED CIRCUIT TOPOLOGY

5.2.1 *Comparison to Previous Works*

The previous works related to energy harvesting power conversion in Chapter 4 [2–5, 8–13] all have drawbacks from a practical implementation perspective. These drawbacks are reiterated below:

- Low or unknown peak efficiency [2, 4, 5, 8–13]
- Low maximum load range [3, 5, 8–10]
- Minimum input voltage >300 mV [4, 5, 10]
- Require external bias voltage(s) [2, 8]
- Require many external components [4, 5, 9, 11]
- Require a mechanical switch for startup [9]
- Complicated design [3, 9]
- Clock frequency controlled externally [10]
- Require very large external components for best performance [11]
- Require deep n-well isolated NMOS transistors [12]
- Require clock generated externally [12]
- Unregulated output voltage [12]
- Require a battery for external storage [3, 13]
- Switching in the audio range (<20 kHz), generating audible noise [13]

5.2.2 *Design Methodology*

With the drawbacks of previous circuits in mind, my circuit is designed with the following design targets:

1. High peak efficiency (>90%)
2. Maximum load >5 mW
3. Minimum input voltage <300 mV
4. Only 3 external components (2 capacitors, 1 inductor)

5. Output voltage 1.0 V and well regulated
6. Does not require energy storage (battery, super-capacitor)
7. None of the following *research paper tricks*:
    - Additional external voltages
    - External back-gate bias
    - External clock source
    - Clock frequency, bias, etc. controlled externally
    - Exotic devices not in standard CMOS process (isolated NMOS, vertical NPN, etc)

In order to achieve both high efficiency and a low input voltage, the proposed circuit uses a novel combination of commonly-used circuits to achieve a low input voltage, a high efficiency, and a load range that is realistic for energy harvesting systems. This approach also requires two control schemes for startup and steady-state operation, respectively:

1. A charge pump circuit is used to create a voltage high enough to begin switching the main power transistors during the initial startup phase (Sec. 5.3).
2. A constant-on time hysteretic control mode is used after startup completes to regulate the output voltage while maintaining a high efficiency (Sec. 5.4).

Both of these control modes are implemented while using only a single input voltage supply and with only 3 external components—an input capacitor, an output capacitor and an inductor. All individual circuit blocks have been optimized to lower the minimum required input voltage and increase the system efficiency, offering exceptional performance at load ranges suitable for energy harvesting applications (on the order of 1 mW).

5.2.3 *Synchronous Boost Topology*

The proposed circuit was designed using a synchronous boost topology using standard NMOS and PMOS transistors for the 2 switches, similar to the circuit shown in Fig. 2.11 of the survey on power management circuits (Sec. 2.2.3.2). All circuits were designed at the transistor level, including the drivers for the power transistors and all internal control circuitry. Because of this approach, the simulation results include all internal circuit parasitics and give a more accurate representation of how the practical circuit operates.

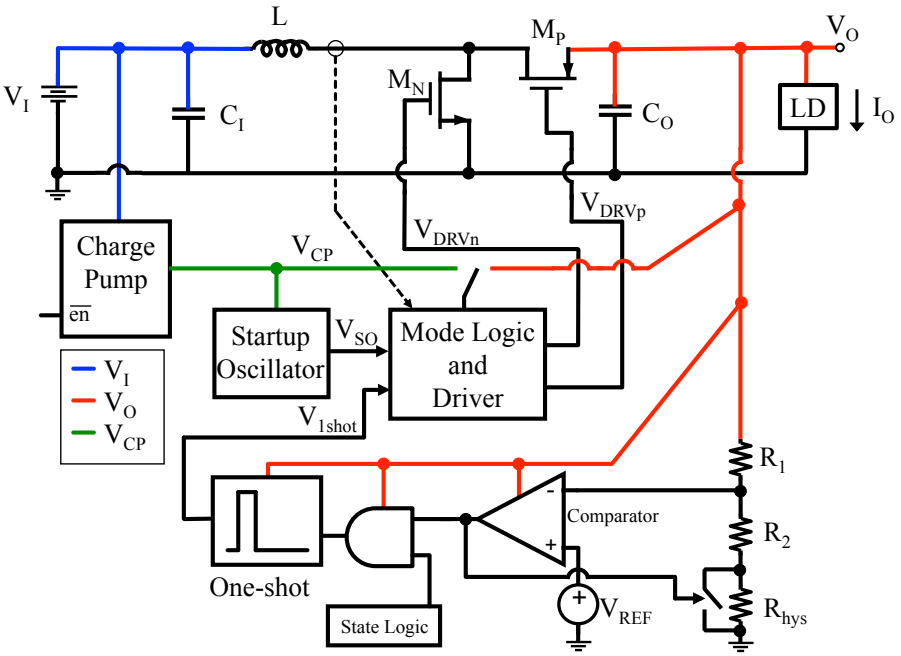


Figure 5.1: Bootstrapped boost converter block diagram.

5.2.4 *Design Methodology*

The proposed circuit uses a novel combination of commonly-used circuits to achieve a low input voltage, a high efficiency, and a load range that is realistic for energy harvesting systems. During startup, a charge pump circuit (Sec. 5.3) is used to create a voltage high enough to begin switching the main power transistors. Once the output voltage has risen to an acceptable value, the system changes to a constant-on time hysteretic control mode (Sec. 5.4.1) to regulate the output voltage while maintaining a high efficiency. This is accomplished by using only a single input voltage supply (i.e. there is no extra gate biasing) and with only 3 external components—an input capacitor, an output capacitor and an inductor.

All individual circuit blocks have been optimized to lower the minimum input voltage and increase the system efficiency, offering exceptional performance at load ranges suitable for energy harvesting applications ($\approx$ 1 mW).

5.2.5 *Block Diagram*

A block diagram of the proposed circuit is shown in Fig. 5.1. The components L, M_N, M_P and C_O form the core of a basic boost converter, similar to that in Fig. 2.11. Since the output voltage V_O will be well regulated and larger than the input, it is suitable for supplying power to the internal control circuitry: namely the voltage loop comparator, one shot and voltage reference. In order to initially raise

the output voltage however, I am using a charge pump circuit that can operate from a very low input voltage, which will be described in Sec. 5.3.1. The output of this charge pump is then fed to a fixed-frequency startup oscillator and to the main drivers that commutate the switches and raise the output voltage to bias the internal circuitry.

Once the output voltage has reached an acceptable level, the charge pump and startup oscillator are stopped, and the driver power source switches to the output voltage. When this handoff is complete, the circuit begins running in a constant-on-time hysteretic mode, as described in Sec. 5.4.1. The input voltage V_I, output voltage V_O and charge pump output voltage V_{CP} are highlighted in different colors to help easily understand the voltage domains present in the proposed circuit.

5.3 STARTUP

The following subsections introduce the bootstrapped startup scheme for this circuit, and how the startup charge pump is able to begin switching the main drivers and output switches.

5.3.1 *Startup Charge Pump*

The proposed circuit is designed in a 0.18 μm CMOS process that supports NMOS native–V_t and low–V_t transistors (threshold voltages for all available 1.8 V transistors are shown in Table 5.1). In order to reduce leakage current however, nominal V_t devices are used as the output drivers and switches. Because the threshold voltage of the nominal devices is greater than 400 mV, an on-chip charge pump is used to ensure that the system can operate with V_I less than the switch threshold voltage. Fig. 5.2 shows the oscillator used to operate the charge pump circuit. By using low-Vt transistors and an 8 fF capacitor, this circuit operates at 80 MHz with an input voltage of 300 mV.

Since the charge pump is only used during the initial startup mode of the circuit, this oscillator needs to be disabled when the constant-

Table 5.1: Transistor threshold voltage V_{t0}

Transistor Type	Model V_{t0}
Native NMOS	−0.02 V
Low–V_t PMOS	−0.13 V
Low–V_t NMOS	0.27 V
Nominal–V_t PMOS	−0.44 V
Nominal–V_t NMOS	0.44 V

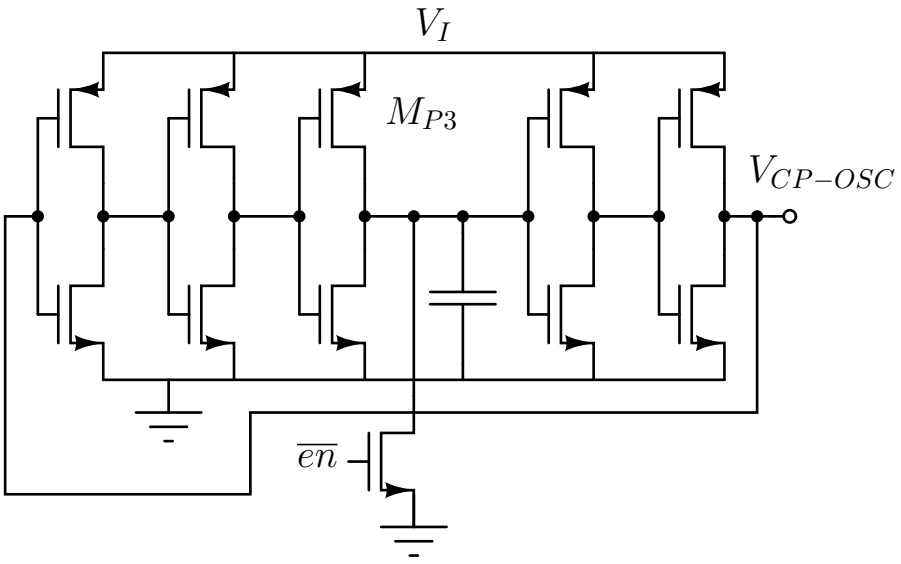


Figure 5.2: Startup charge pump oscillator.

on-time loop takes over. To this end, the final PMOS M_{P3} in the oscillator of Fig. 5.2 is designed with a W/L size of 2 μm / 5 μm in order to minimize current consumed when this cell is disabled. The other PMOS transistors are 5 μm / 250 nm and the NMOS transistors are 2 μm / 300 nm, where 250 nm and 300 nm are the minimum channel length for low–V_t PMOS and NMOS transistors, respectively.

It should be noted that this circuit is the limiting step in terms of minimum startup voltage. As long as the charge pump oscillator operates, the charge pump will create a high enough output voltage to operate the main switches and operate the circuit (as described later). Current data shows that the minimum input voltage required to start up the charge pump oscillator, and hence the full circuit, is 240 mV.

Fig. 5.3 shows the complete charge pump schematic. The oscillator from Fig. 5.2 is fed through a buffer before connecting to a diode-connected native–V_t NMOS charge pump, similar to the approach in [15]. Unlike the previous work, our system relies on an oscillator signal generated on-chip and is connected to the output switch drivers, which require a large amount of power to operate. Because of these drawbacks, while using a 10 stage design, our charge pump achieves a peak voltage of only 950 mV from a 300 mV source. In my implementation of this charge pump, all native-V_t NMOS transistors are designed with a size of 40 μm / 500 nm. Capacitors C_1 are 5 pF MIMCAPs and C_2 are 40 pF NMOS gate capacitors. Optimization simulations showed that this mix of capacitors yields the best performance for this circuit. Note that in the CMOS process I used, 500 nm is the minimum channel length for native–V_t NMOS transistors.

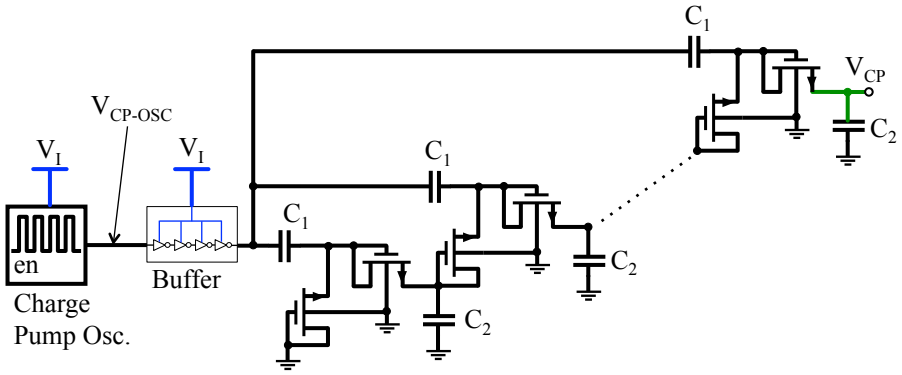


Figure 5.3: Full charge pump schematic.

5.3.2 *Startup Oscillator and Driver*

In order to raise the output voltage to an appreciable value to bias the hysteretic control circuitry, a high duty cycle oscillator is applied to the gate driver circuitry for the switch transistors, powered by the charge pump described in Section 5.3.1. Using an oscillator similar to that in Fig. 5.2, but running at a frequency of 100 kHz, this low-frequency clock is modified to run at a very high duty cycle (83%). Fig. 5.4 shows the high duty cycle transformation circuit. As long as either of the inputs to the NAND gate are low, the output of this circuit will be high. Since the input comes from a clock running at about 50% duty cycle, the output is only low during the delay when the oscillator goes from LO to HI. During this time, the output V_{SO} will be low until the input signal propagates through the three inverter, two capacitor delay cell. As was described in Sec. 2.2.2.1, the duty cycle of the converter must be less than 100% to ensure that current from the inductor is transferred to the output capacitor, and hence the output voltage can rise. The schematic of this high-duty-cycle system connected to the drivers and output switches is shown in Fig. 5.5.

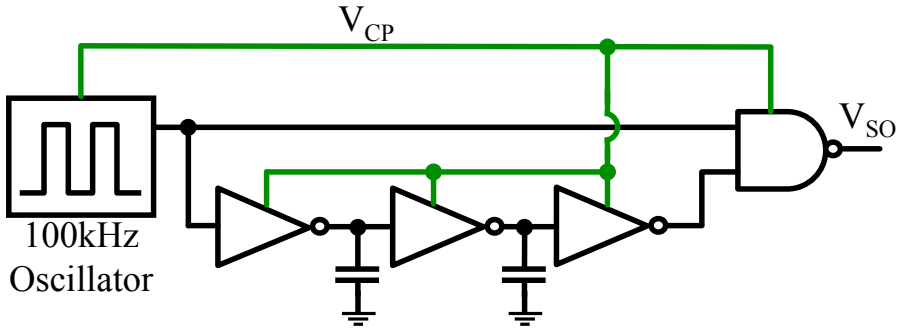


Figure 5.4: Startup oscillator and high duty cycle circuitry.

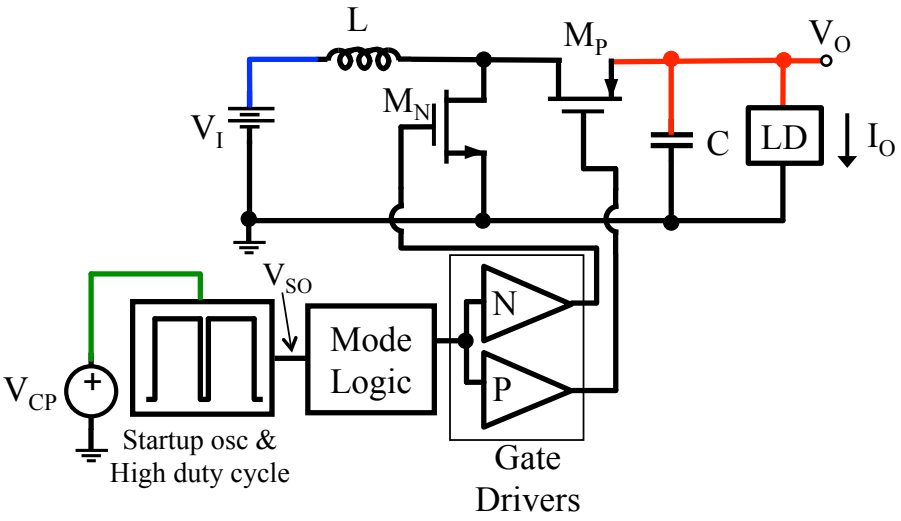


Figure 5.5: Startup circuitry connected to drivers and output switches.

5.4 STEADY-STATE OPERATION

The following subsections introduce the steady-state constant-on-time hysteretic control scheme that is used to accurately and efficiently regulate the output voltage.

5.4.1 *Hysteretic Control*

The main control loop for the proposed circuit is implemented using the constant-on-time control scheme shown in Fig. 5.6 and similar to what is described in [18]. If the feedback voltage is below the reference voltage, the one-shot circuit will trigger, causing the NMOS switch to turn on for a fixed period of time. At the same time, the switch across R_{hys} will close, effectively setting the voltage threshold to a higher level and adding a predictable amount of positive hysteresis. Once the one-shot times out, the NMOS turns off and the PMOS turns on, until the current through the inductor reaches zero.

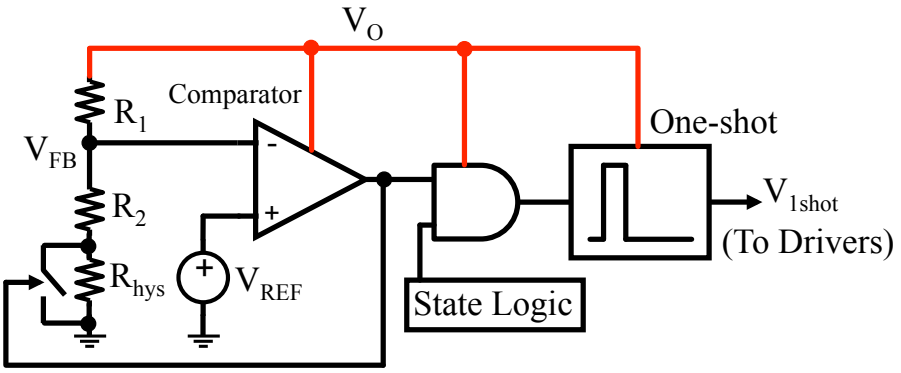


Figure 5.6: Hysteretic control schematic.

At this point, the same process repeats until V_O reaches the comparator threshold, at which point the circuit goes into a low-power coasting mode and the R_{hys} switch turns off, returning the circuit to its lower threshold as it waits for the output voltage to fall again.

The block labeled "State Logic" in Fig. 5.6 controls when the circuit enters coasting mode (i.e. the one shot is disabled and both switches are OFF) as well as resetting the one-shot after every zero current detect when the NMOS is OFF. A state diagram of the proposed control scheme is shown in Fig. 5.7.

5.4.2 *Output Voltage Ripple*

By examining Fig. 5.8 and assuming the output current I_O is zero, a closed-form expression can be developed for the output voltage ripple, Δv_O. Note that Fig. 5.8b shows the on-time system while the NMOS and PMOS are commutating ON and OFF, hence here is no "Coasting" time. In the zero-load condition, the output voltage of the constant-on-time regulator only increases when the inductor is discharging, and hence, transferring its energy to the output capacitor. During this time (t_1 to t_2), switch S_1 is OFF while S_2 is ON as shown in Fig. 5.8a. The current in the inductor over an entire switching period is shown in (5.1).

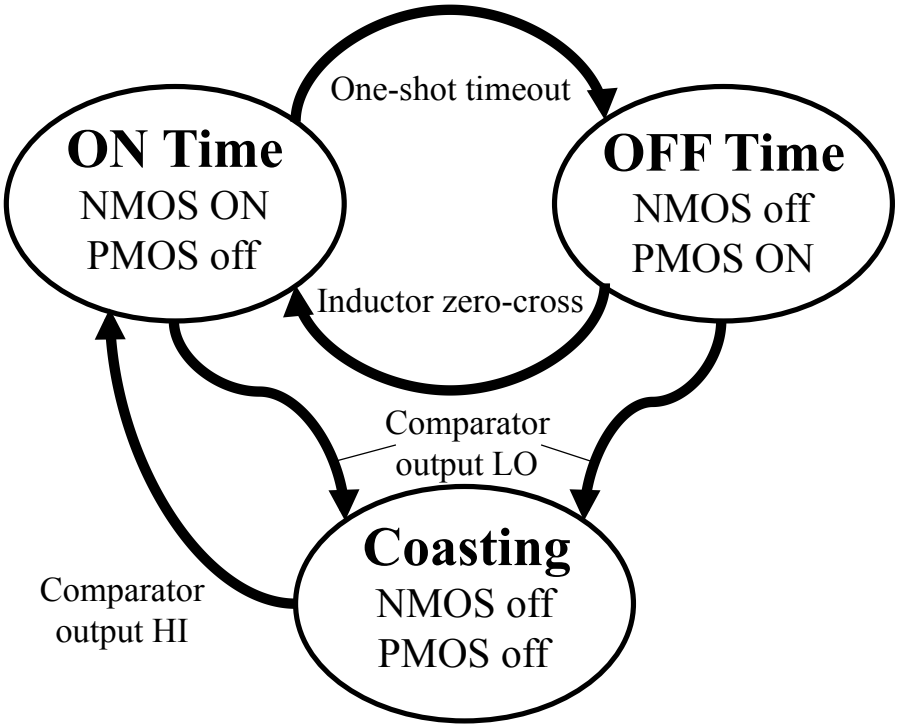


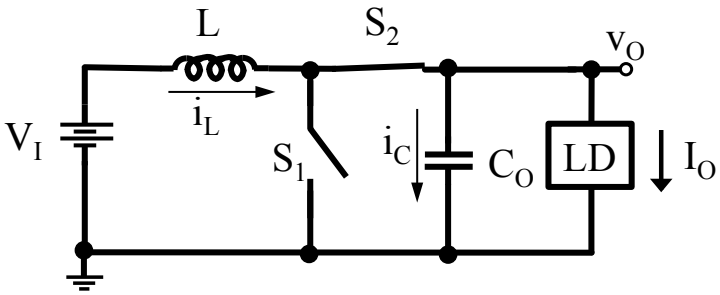
Figure 5.7: Hysteretic control state diagram.

$$i_L(t) = \begin{cases} \frac{V_I}{L}t, & t_0 < t \leq t_1 \quad (5.1a) \\ I_P - \frac{V_O - V_I}{L}(t - t_1), & t_1 < t \leq t_2 \quad (5.1b) \end{cases}$$

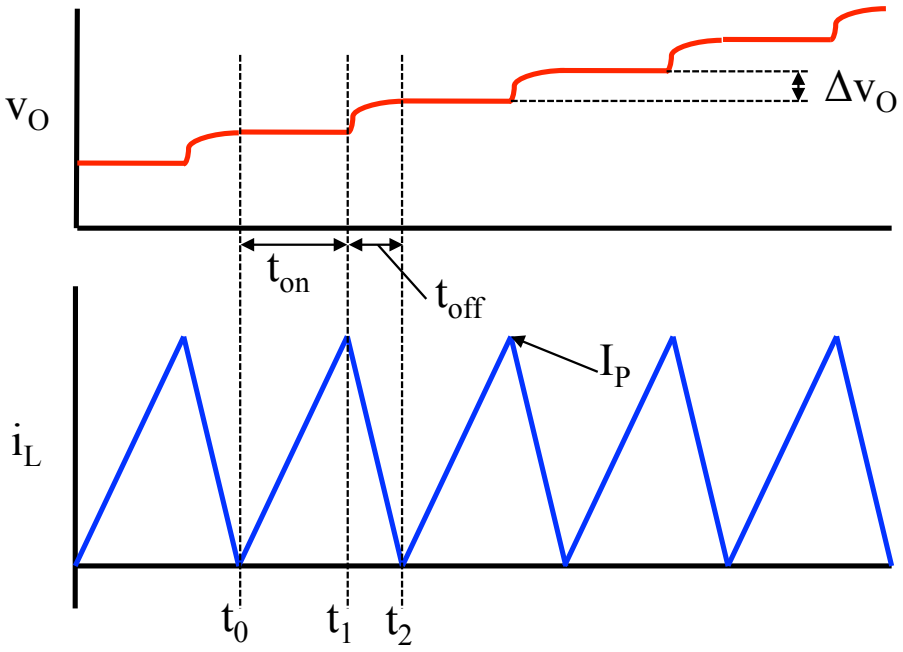
And hence,

$$t_{off} = t_2 - t_1 = \frac{I_P L}{V_O - V_I}. \quad (5.2)$$

During t_{off}, when the current from the inductor flows to the output capacitor and load, the output voltage will increase for each cycle. Assuming the load current, I_O is zero, This change in output voltage, Δv_O, can be derived as shown in (5.3).



(a) Off-time schematic.



(b) Switching inductor current and output voltage.

Figure 5.8: Constant-on-time voltage ripple analysis.

$$\begin{aligned}\Delta v_O &= \frac{1}{C_O}\int i_L(t)\,\mathrm{d}t = \frac{1}{C_O}\int_{t_1}^{t_2}\left[I_P - \frac{V_O - V_I}{L}(t - t_1)\right]\mathrm{d}t \\ &= \frac{I_P^2 L}{2C_O(V_O - V_I)} \end{aligned} \tag{5.3}$$

From (5.1a), it can be shown that I_P=$V_I\ t_{on}/L$, and thus (5.3) can be simplified to the more readable expression shown in (5.4).

$$\Delta v_O = t_{on}^2 \frac{V_I^2}{2LC_O(V_O - V_I)} \tag{5.4}$$

5.4.3 *Maximum Load Current*

Using the superposition principle, the output voltage ripple including effects from the load current I_O can be written as:

$$\Delta v_O = t_{on}^2 \frac{V_I^2}{2LC_O(V_O - V_I)} - \frac{I_O\left(t_{on} + t_{off}\right)}{C_O}. \tag{5.5}$$

Since the output voltage ripple will be zero at the maximum load current (i.e. the output voltage cannot increase), the maximum load current is as shown in (5.6). Note that the result from (2.18) was substituted in order to make this result more compact.

$$I_{O(max)} = t_{on}\frac{V_I^2}{2LV_O}. \tag{5.6}$$

While increasing the on time or reducing the value of the inductor increases the available load, the peak inductor current also increases. While this is not a problem in the ideal mathematical case, larger peak currents are a problem in the practical circuit, where the switch resistance $r_{DS(on)}$ is fairly high. Because of this limitation, simulations have shown that a peak inductor current of I_P = 45 mA provides a good balance of high maximum load current with low power loss (high efficiency).

5.4.4 *Voltage Hysteresis Value*

By analyzing the circuit of Fig. 5.6, and ignoring non-idealities in the comparator, it can easily be shown that the value of the voltage hysteresis, ΔV_O is

$$\Delta V_O = V_{REF}\frac{R_1}{R_2 + R_{hys}}\frac{R_{hys}}{R_2}. \tag{5.7}$$

5.4.5 *Voltage Reference*

Since the proposed circuit operates with an output voltage around 1.0 V which is used to drive the control circuitry, the reference voltage (labelled V_{REF} in Fig. 5.1) must also run from a very low input voltage. Due to its low input voltage requirement and the ability to create a reference voltage less than a typical 1.2 V bandgap, I have modified the Banba bandgap voltage reference described in [16]. In order to save space, I incorporated an area mismatch of $8\times$ to $1\times$ between the two PNP BJTs; this has an added benefit that the transistors can be easily laid out in a 3×3 grid.

Additionally, I adjusted the reference voltage output to 250 mV, which is better suited to the application. However, since these parameters have been changed, the values of the pertinent resistors must also be changed, as explained in the next subsection.

5.4.5.1 *Voltage Reference Design Equations*

Like any bandgap voltage reference, the Banba bandgap operates by adding a voltage component that is Complimentary To Absolute Temperature (CTAT) to a voltage component that is Proportional To Absolute Temperature (PTAT). In the circuit of Fig. 5.9, the two substrate-collector PNP devices and the output resistor R_3 share the same current

$$I_1 = v_T \frac{\ln(A)}{R_1} + \frac{V_{BE}}{R_2}, \tag{5.8}$$

where V_{BE} is the emitter-base voltage of the 1x transistor, $v_T = kT/q$ is the *thermal voltage* of silicon (which is directly proportional to temperature T) and A is the area ratio between the two PNP transistors.

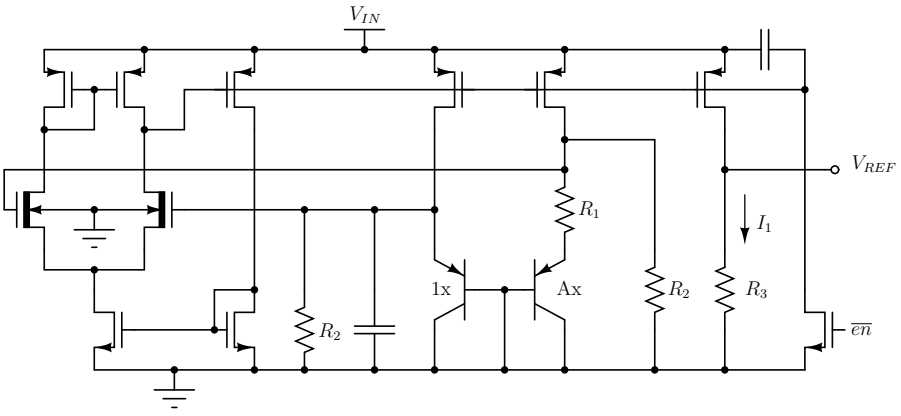


Figure 5.9: Banba bandgap voltage reference.

Since $V_{OUT} = I_1 R_3$,

$$V_{REF} = \frac{R_3}{R_1} v_T \ln(A) + \frac{R_3}{R_2} V_{BE}. \tag{5.9}$$

(5.9) shows that the reference voltage is a function of a PTAT component and a CTAT component, hence the resistor ratios and area ratio A can be adjusted to ensure that the reference voltage remains constant over temperature.

As described in [17], the base-emitter voltage of a BJT can be written as:

$$V_{BE} = E_{GE} - H(E_{GE} - V_{BEN}) + v_{TN} H \ln(I_C / I_N) - \eta v_{TN} H \ln(H), \tag{5.10}$$

where E_{GE} is the bandgap voltage of silicon, H is the "hotness" factor ($H = T/T_N$), T_N is a normalizing temperature, V_{BEN} is the value of V_{BE} at a normalized point, I_C/I_N is the BJT collector current divided by the normalized current, v_{TN} is the value of the *thermal voltage* at nominal temperature ($v_{TN} = kT_N/q$), and η is a curvature factor. Assuming that the collector current of the transistor remains constant, V_{REF} can be rewritten as:

$$V_{REF} = \frac{R_3}{R_1} H v_{TN} \ln(A) + \frac{R_3}{R_2} \left[E_{GE} - H(E_{GE} - V_{BEN}) - \eta V_{TN} H \ln(H) \right]. \tag{5.11}$$

In order to make V_{REF} a proper reference voltage, it should remain constant over temperature, hence

$$\frac{\partial V_{REF}}{\partial H} = 0. \tag{5.12}$$

Substituting (5.11) into (5.12) and expanding, an expression can be developed for which V_{REF} does not change with temperature:

$$\frac{R_1}{R_2} = \frac{v_T \ln(A)}{E_{GE} - V_{BEN} + \eta V_{TN}}. \tag{5.13}$$

As long as the condition in (5.13) is met, a closed form expression can be gained for V_{REF} that does not change with temperature:

$$V_{REF} = v_T \ln(A) \frac{R_3}{R_1} \left(1 + \frac{V_{BEN}}{E_{GE} - V_{BEN}} \right). \tag{5.14}$$

In order to finalize the values for the resistors, start by setting the area mismatch between the two PNP transistors to 8:1 ($A = 8$).

Since the difference in the two V_{BE} voltages will appear across resistor R_1, and setting the current in each PNP to 300 nA, we have $R_1 =$ 54 mV / 300 nA $=$ 180 kΩ. By using the result of (5.14) then (5.13) and setting $V_{REF} =$ 250 mV, it follows that $R_3 =$ 371 kΩ and $R_2 =$ 2.07 MΩ.

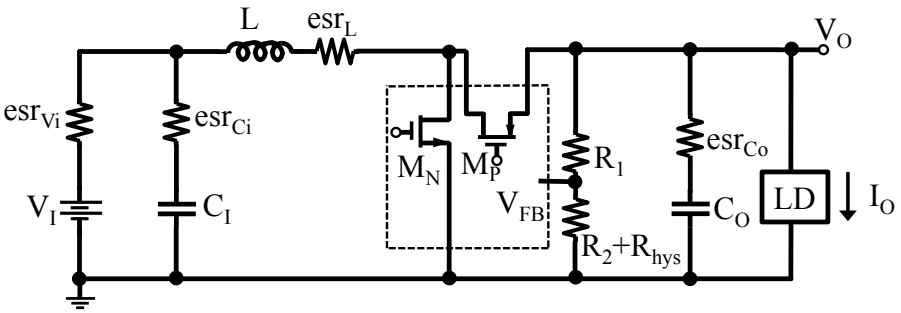


Figure 5.10: Simulation schematic including parasitic resistances.

Table 5.2: Simulation values

Circuit Component	Value
V_I	300 mV
V_O	1.0 V
L	10 μH
C_I	2.2 μF
C_O	5.0 μF
esr_{Vi}	100 mΩ
esr_L	90 mΩ
esr_{Ci}	10 mΩ
esr_{Co}	10 mΩ
R_1	1.7 MΩ
R_2	531 kΩ
R_{hys}	28 kΩ
t_{on}	1.5 μs
V_{REF}	250 mV
NMOS size	5 mm / 0.18 μm
PMOS size	10 mm / 0.18 μm

5.5 SIMULATION RESULTS

5.5.1 *Simulation Schematic*

Simulations were performed on the circuit shown in Fig. 5.10, with the simulation values shown in Table 5.2. Since circuit parasitics have a large effect on the operation of a boost regulator, parasitic resistances have been included wherever possible. Note that the dashed box in the middle of Fig. 5.10 shows the internal (transistor-level) circuitry, while everything outside this box is an external component.

Note that since this circuit operates with a hysteretic control scheme, frequency compensation is not needed, and hence there are no stability advantages to using a current source rather than a resistive load [19].

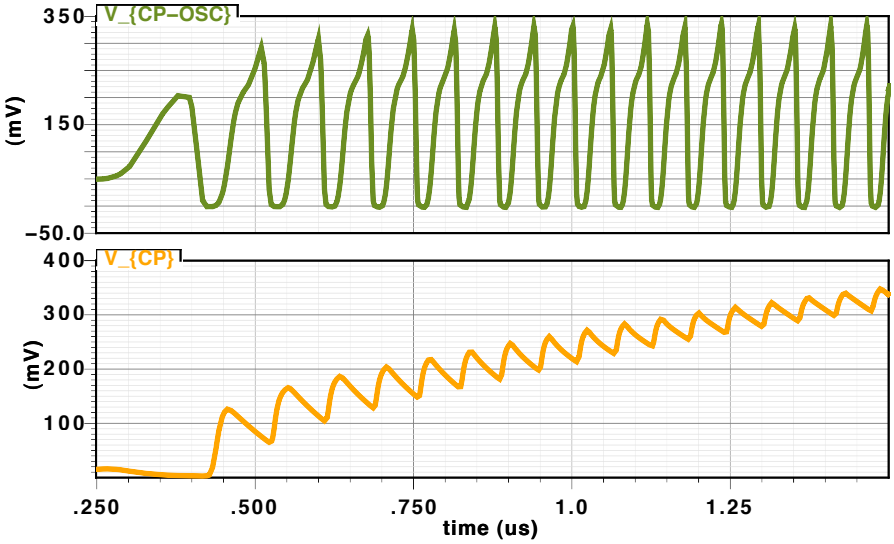
5.5.2 *Startup Results*

The initial startup of the regulator, using the charge pump circuitry and oscillator described in Sec. 5.3.1, is shown in Fig. 5.11. Once the charge pump oscillator starts switching, the output of the charge pump gradually rises (Fig. 5.11a). Once the charge pump output is large enough to run the startup oscillator and drivers (shown previously in Fig. 5.5), the main switches start commutating, and the output voltage V_O slowly rises as shown in Fig. 5.11b.

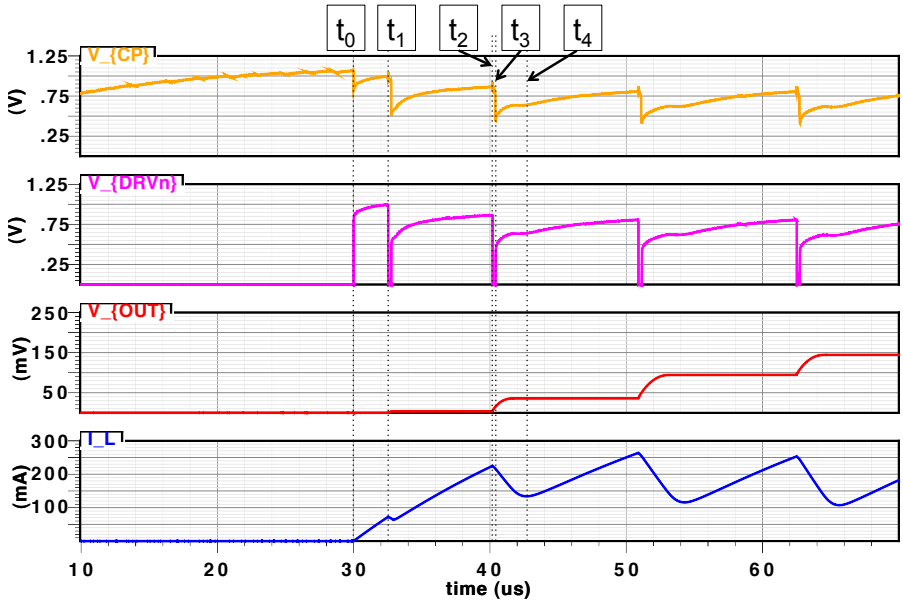
Since there are a lot of things changing in Fig. 5.11b, time points t_0 through t_4 have been highlighted to understand the circuit operation during initial startup. The following is a description of the circuit behavior at each of these time points:

$t < t_0$:
The charge pump output voltage V_{CP} slowly rises until it reaches a high level ($\approx$1 V).

$t = t_0$:
The startup oscillator and high duty cycle converter from Fig. 5.4 start working and send out a single, short pulse. Since the startup oscillator is a positive-feedback ring oscillator that starts up in an unknown state, it makes sense that this pulse does not have the same width as subsequent oscillator pulses. Since the oscillator output is high, the voltage on the gate of the NMOS switch



(a) Initial V_{CP} startup.



(b) V_{CP} driving switch transistors. Notable times points are labelled t_0—t_4

Figure 5.11: Charge pump startup simulation.

(V_{DRVn}) is also high, which causes the inductor current I_L to increase.

$t = t_1$:
The oscillator output goes low and stays off for a fixed amount of time based on the high duty cycle circuit delay. During the short amount of time that V_{DRVn} is low (and hence the PMOS is on), the inductor current decreases and the output voltage increases as energy stored in the inductor flows to the output capacitor and load. At this time point, V_{CP} also jumps downward, since the charge pump output is high impedance and is barely able to support the load of switching the drivers and output switches on and off.

$t = t_2$:
After a period where the oscillator signal is high and V_{CP} keeps charging up slowly, the NMOS turns off and the PMOS turns on, once again causing V_{CP} to fall down quickly.

$t = t_3$:
After a short delay caused by the high duty cycle circuit, the switches change again and the NMOS tries to turn back on. However, in this case the voltage on the NMOS gate (supplied from V_{CP} is too small to properly turn on the NMOS switch, since this device has a fairly high threshold voltage (0.5 V). Thus, instead of turning on the NMOS switch immediately at time t_3, the circuit has to wait until V_{CP} reaches a value high enough to turn on the switch.

$t = t_4$:
At this point, V_{CP} has reached a high enough level to turn on the NMOS switch and let it continue to build up several mA of current. In the interval $t_3 < t < t_4$, I_L decreases, making it look like the NMOS is off, when in reality the circuit is trying to turn on the NMOS but there is not a large enough voltage supply available at V_{CP}.

$t > t_4$:
After time t_4, the oscillator and high duty cycle circuit reach an equilibrium and continuously produce pulses at the same frequency on duty cycle. During this time, the main switches operate at a constant duty cycle which raises the output voltage. Once the output voltage is high enough to bias the internal circuitry, the steady state hysteretic control loop takes over.

Note that since the charge pump is not able to deliver a large amount of current, and since it is loaded by the drivers and output switches, the output of the charge pump reaches a maximum value of only 0.8 V, even with the 10-stage configuration described in

Fig. 5.3. But this circuit is strong enough to raise the output voltage during initial startup, and once V_O has risen to the reference point, the constant-on time controller takes over and the circuit switches to the steady state, constant-on-time mode.

5.5.3 *Steady State Results*

Fig. 5.12 shows the simulated steady-state operation of the proposed circuit. Starting from the far left of the figure, both switches are off and the output voltage is slowly coasting downward, with a slope determined by the output load current (i.e. this is the "Coasting" time shown in Fig. 5.7). During the coast time however, the hysteretic comparator is still watching V_O, and as soon as it reaches the lower threshold of the comparator, the constant-on time control is enabled. Until the comparator reaches its upper threshold, the circuit turns on the NMOS (and hence charges the inductor) for a fixed amount of time, then turns off the NMOS (and hence turns on the PMOS) until the inductor current reaches zero. When the upper threshold of the comparator is finally reached, both switches are turned off and the circuit re-enters the coasting mode, as was previously shown in the state diagram of Fig. 5.7.

5.5.4 *Calculation and Simulation Comparison*

Using the values shown in Table 5.2 along with the analysis in Sec. 5.4.1, notice that the maximum load should be $I_{O(max)} = 6.7$ mA with a peak-to-peak voltage ripple of $\Delta V_O = 40$ mV (using the results from (5.6) and (5.7) respectively). As can be seen in Fig. 5.13, the maximum

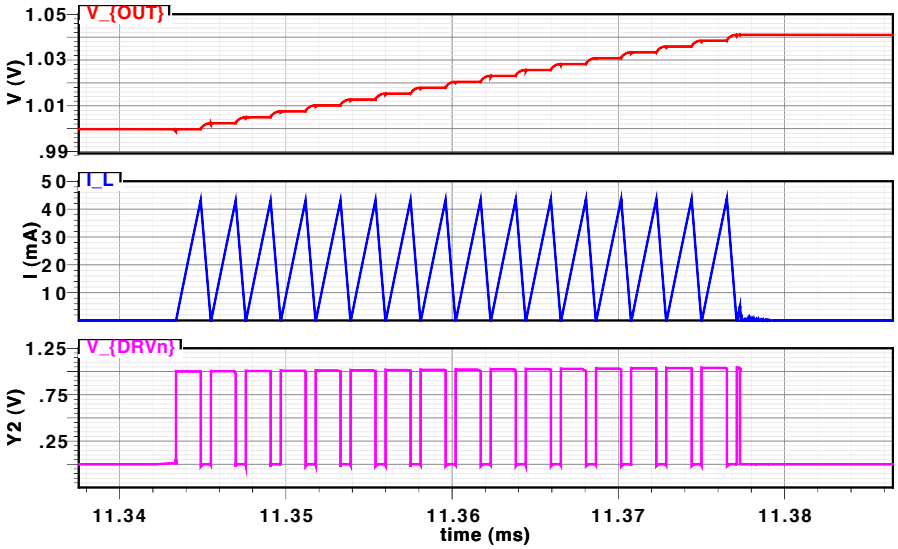


Figure 5.12: Steady state operation simulation.

load is just past $P_O = 6.2$ mW, and hence this agrees well with the predicted value. From Fig. 5.12, it can be seen that the voltage ripple is about 40 mV.

5.5.5 *Efficiency*

The total end-to-end efficiency of the proposed circuit is shown in Fig. 5.13. While the efficiency drops off slightly at lower load, it remains above 95% for most of the load range, reaching a maximum of 97% at a load of 6.2 mW. The high efficiency in the proposed circuit is a virtue of the fact that switching losses are very low, and the control circuitry consumes very little quiescent current. Note that this data comes from simulation results, and the efficiency values for an actual circuit will likely be lower. This is because there are various parasitic components that are difficult to model in simulation.

The efficiency curve for this circuit shows that the efficiency increases as the load increases. Since the circuit uses a hysteretic control scheme, the amount of *coasting* time decreases as the load increases, and hence the amount of switching time increases. Even at maximum load (i.e. the highest load point on the efficiency graph), the efficiency is quite high, which verifies that the majority of power loss in this circuit is not due to switching losses. A more detailed analysis of efficiency in a switching regulator will be presented in Sec. 5.6. Also note that further increasing the load beyond the maximum load point will cause the output voltage to fall, since the regulator becomes current limited. Any data collected beyond the 6.2 mW point would likely show the efficiency decrease as the load increases.

A comparison between my peak efficiency and maximum load with recently published papers in the field of energy harvesting is shown in Table 5.3. Note that "Magnetic" architecture refers to a circuit that uses at least one inductor—switched capacitor circuits require no inductor.

Table 5.3: Peak values in related works

Publication	Max Eff.	Max Load	Architecture	Drawback
[2]	49.9%	72 μW	Magnetic	External 4 V
[3]	88%	60 μW	Magnetic	External 1.8 V
[8]	79%	300 μW	Magnetic	Off-chip bias
[9]	58%	500 μW	Magnetic	Mechanical sw
[10]	70%	1.0 mW	Switched Cap	
[5]	60%	3.9 mW	Magnetic	
This work	97%	6.2 mW	Magnetic	

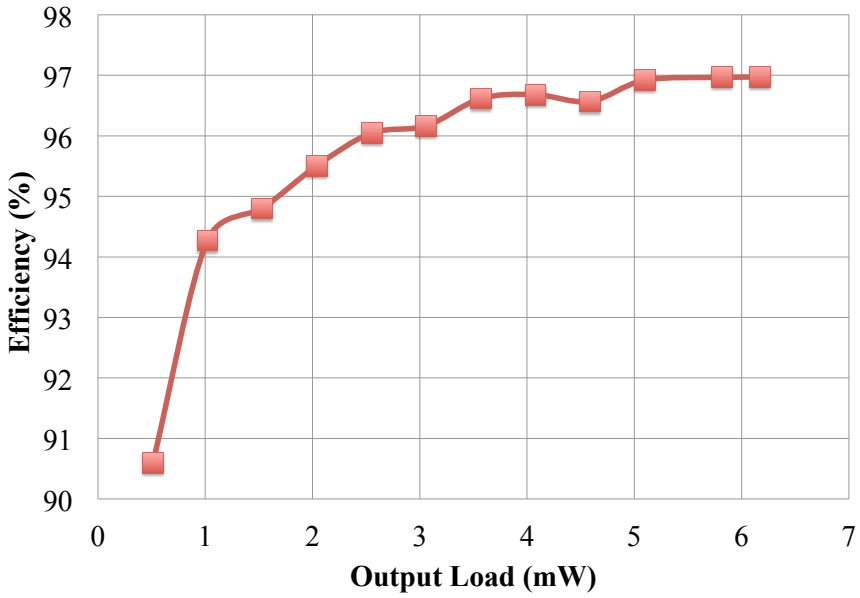


Figure 5.13: Efficiency over load range.

5.6 EFFICIENCY ANALYSIS

Based on the discussion in [20], it can be shown that the conduction losses of the circuit are as shown in (5.15).

$$P_{Lc} = I_{rms}^2 \times r_{DS(on)} \tag{5.15}$$

$r_{DS(on)}$ is the equivalent resistance of the switch in the ON state. Accordingly, the on-resistance value can be represented as:

$$r_{DS(on)} \approx \frac{1}{k' \frac{W}{L}(V_{GS} - V_t)} \tag{5.16}$$

where k' is the process parameter for the MOSFET, V_{GS} is the gate-to-source voltage, V_t is the threshold voltage and W and L are the transistor width and length, respectively. By increasing the width of the transistor (or increasing the W/L ratio), the equivalent on-resistance will decrease.

When the converter is switching, there are also switching losses which can be written as

$$P_{Lsw} = t_r \, V_{ds(max)} \, I_{Load} \, f_{sw} + \frac{1}{2}\left(C_{oss} \, V_{ds(max)}^2 \, f_{sw}\right) + f_{sw} \, Q_g \, v_{drive}, \tag{5.17}$$

where t_r is the turn-on rise time of the switching signal, Q_g is the total gate charge, and C_{oss} is the output capacitance.

5.6.1 *Design Optimizations*

5.6.1.1 *Inductor Current*

After running simulations over various conditions, the current simulation values shown in Fig. 5.10 with an on-time of 1.5 μs seem to maximize the efficiency of the current circuit.

Decreasing the inductor value will lead to a higher peak inductor current and a higher load capability as shown in (5.6), but this paradoxically increases the conduction and switching losses as shown in (5.15) and (5.17). Because of this tradeoff, the inductor value is set at 10 μH which sets a peak inductor current of 45 mA as shown in Fig. 5.12.

It should be noted that increasing the on-time will also increase the peak inductor current and maximum load capability, but will have the same effect in increasing conduction and switching losses.

5.6.1.2 *MOSFET Size*

The size of the switch transistors also has an optimum point. By increasing the size (i.e. increasing the W/L ratio), the on-resistance shown in (5.16) will decrease, leading to lower conduction losses.

Increasing the switch transistor size also increases the gate charge Q_g, which is a component of the switching power losses shown in (5.17). Furthermore, increasing the transistor size also requires using larger drivers for the same gate drive, leading to more power losses in the driver stage. With this in mind, simulations have shown favorable results with MOSFET sizes of of 5 mm/0.18 μm and 10 mm/0.18 μm for the NMOS and PMOS respectively.

5.7 TEST CHIP

5.7.1 *Chip Photomicrograph*

A test chip comprising all the components of the charge pump startup circuit (i.e. those shown in Fig. 5.3) was taped out in a 0.18 μm process from Taiwan Semiconductor Manufacturing Company (TSMC). A photomicrograph of the test chip is shown in Fig. 5.14. The 10 charge pump gain stages, star connected on top of the oscillator and buffer, can be clearly seen in the test chip image.

5.7.2 *Chip Packaging*

Due to packaging limitations, the chip was packaged in a QFP64 package even though the test chip only uses 5 pins. This package was then soldered down to a simple breakout board for lab verification. A photograph of the packaged chip on the breakout board is shown in Fig. 5.15, and the pinout of the test chip is shown in Table 5.4.

5.7.3 *Bench Results*

5.7.3.1 *Lab Setup*

Using the lab setup shown in Fig. 5.16, bench measurements were performed with the packaged part on the breakout board shown in Fig. 5.15.

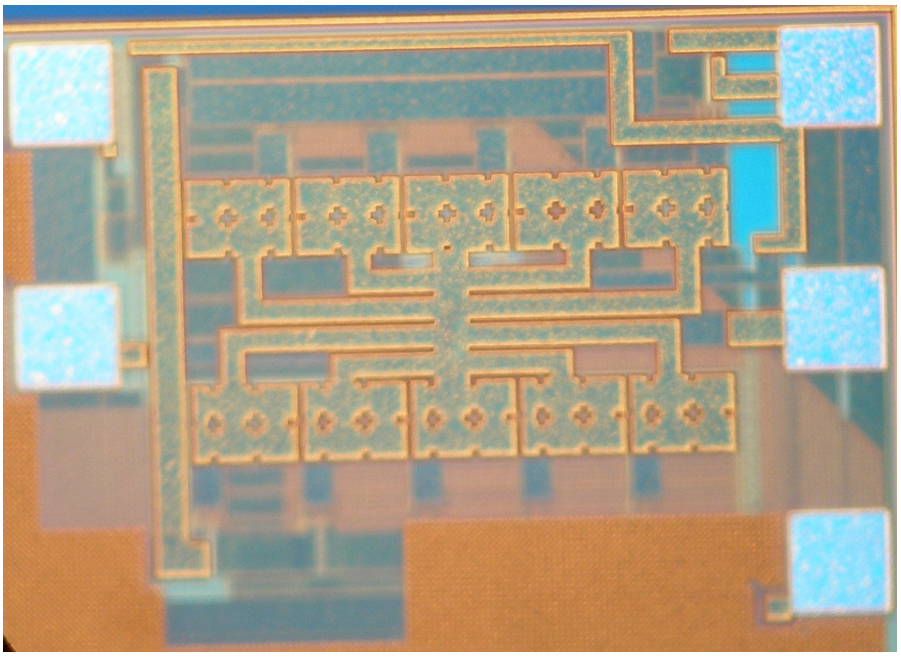


Figure 5.14: Charge pump test chip.

With an input voltage of 400 mV, the charge pump oscillator switches as shown in Fig. 5.17. While this plot proves that the oscillator switches and the charge pump works, adding an oscilloscope probe to the buffer output adds a very large loading capacitance to this node and ruins the gain capability of this circuit. This data point is very important to prove that the part is switching properly, but later data were taken without the oscilloscope connected to minimize loading effects.

As expected, with an input voltage of 400 mV, the charge pump oscillator switches between 0 V and 400 mV. Including the effect of loading the buffer with a large capacitance oscilloscope probe (as de-

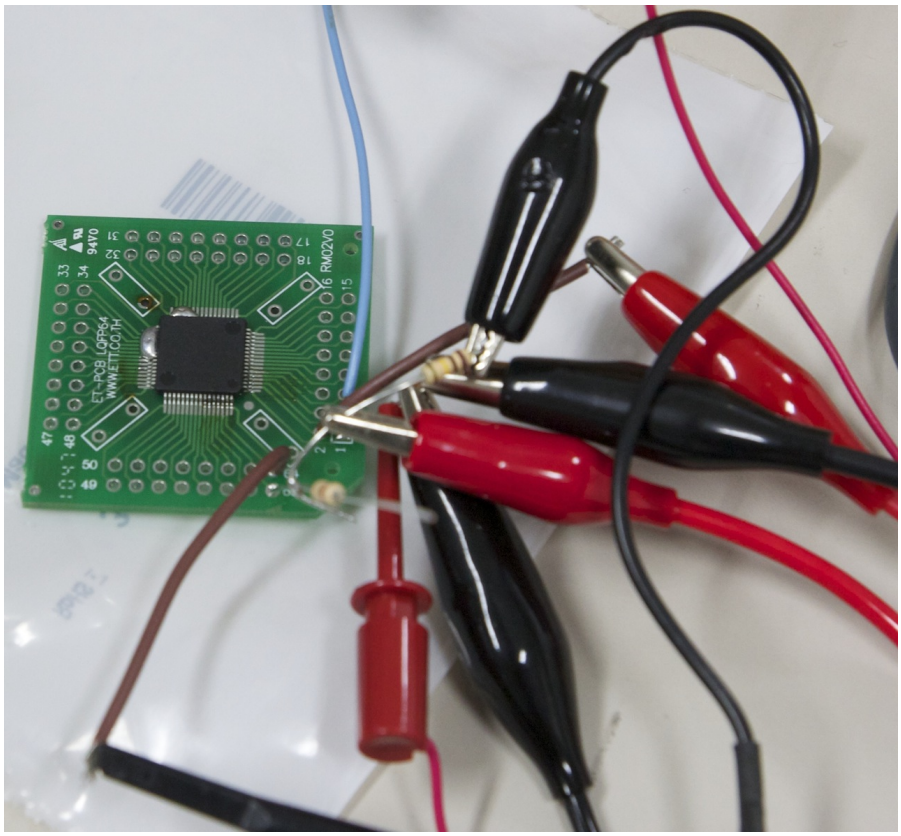


Figure 5.15: Packaged charge pump chip.

Table 5.4: Charge pump test chip pinout.

Pin #	Function
1	V_N
2	V_P
3	$\overline{en}$
63	V_{OUT}
64	Driver Output
Others	No Connection

scribed above), the circuit operates at a frequency of about 30 MHz in this condition. The shape of the switching frequency and the operating frequency are similar to what was predicted in the simulation shown in Fig 5.11a.

5.7.3.2 *Charge Pump Transfer Function*

In order to test the real-world performance of the charge pump, the chip was tested both with no load and with a 100 kΩ resistive load. Results from these experiments are shown in Fig. 5.18.

As expected, with no load there is a decent amount of gain, and the output voltage rises to almost 2 V with an input voltage of 340 mV, corresponding to a gain of about 6 V/V. With a resistive load however, the output voltage rises slower for a given input voltage, but it still seems that the output voltage would rise high enough to start switching the part.

5.7.4 *Bench and Simulation Comparison*

Keeping in mind the loading effect from the capacitor probe, the shape of the ring oscillator signal in the test chip is the same as the simulated result, shown previously in Fig. 5.11a. The frequency of the oscillator is different from the simulated value, but this can be

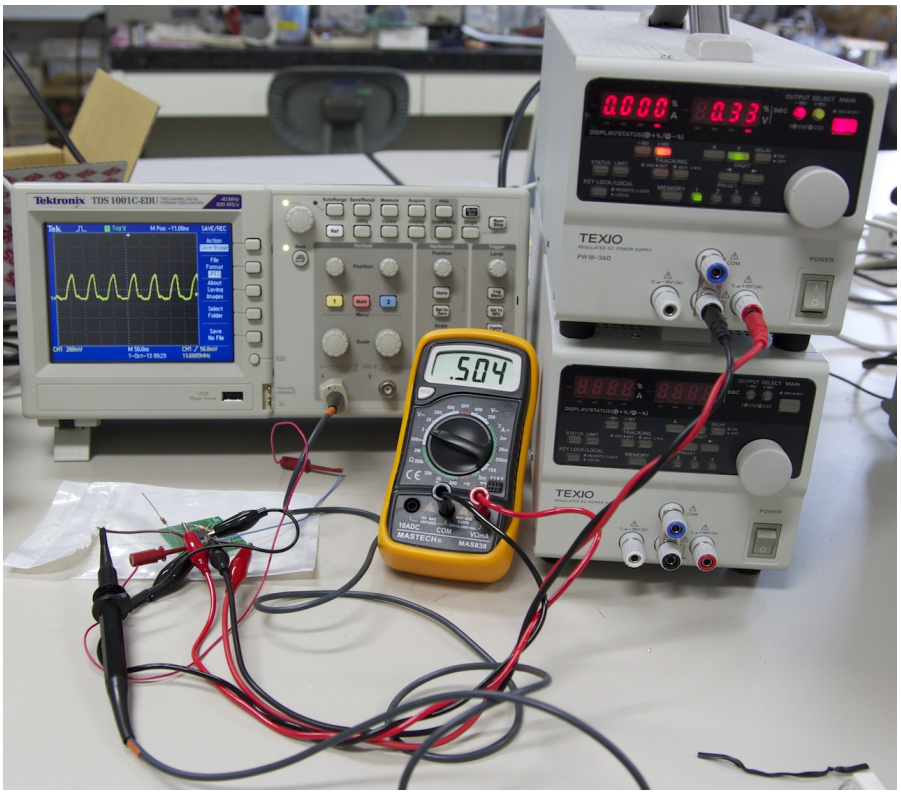


Figure 5.16: Charge pump lab setup.

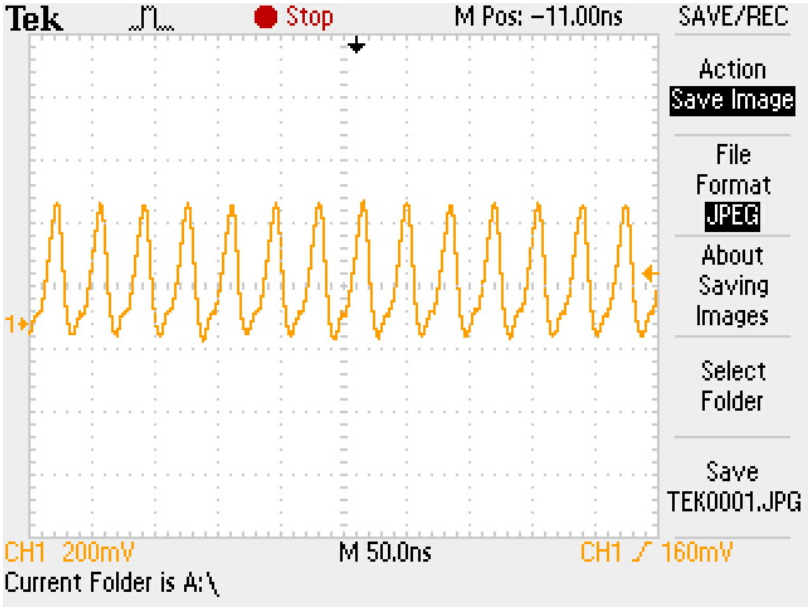


Figure 5.17: Charge pump oscillator buffer output at 400 mV.

explained by two different phenomena. First, capacitive loading of the driver output will cause the oscillator to run slower. Second, the ring oscillator architecture of the circuit is very sensitive to the input voltage and the threshold voltage of the transistors—any small variation from the simulated values will have a large effect on the actual oscillation frequency.

In the actual application, this charge pump output would be applied to an oscillator and the main switch drivers, as shown previ-

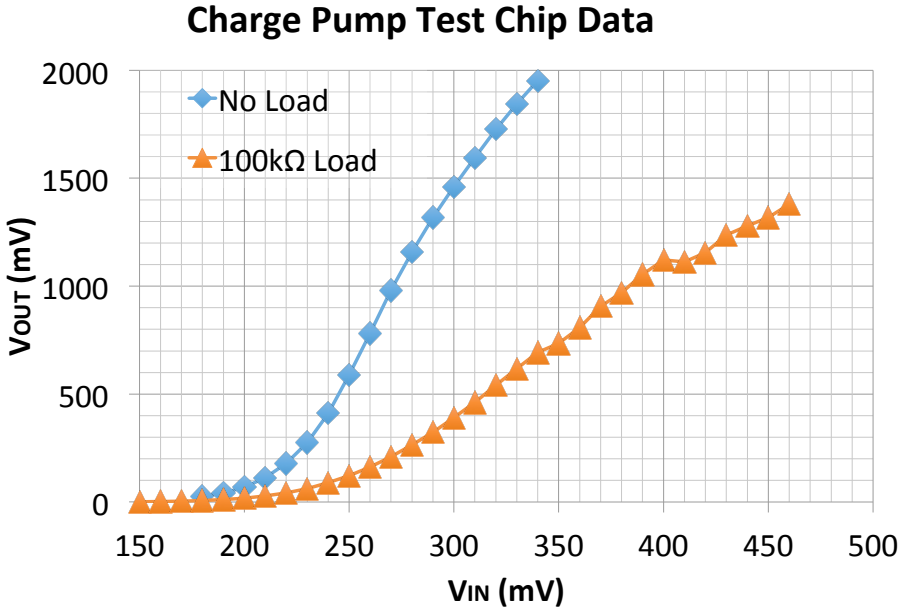


Figure 5.18: Test chip transfer function with and without load.

ously in Fig. 5.5. Unfortunately it is difficult to model this condition without the actual circuit that the charge pump would be powering. But data from this test chip shows that the charge pump oscillator functions, and that the diode-connected native-NMOS charge pump stages should be able to work together to create a high enough output voltage to startup the circuit.

5.8 CONCLUSION

In this chapter, I have introduced a low-power boost regulator that is optimized for energy harvesting applications. While previously presented papers have shown that it is possible to convert energy from extremely low-power input sources, they have not designed their circuits to work with a realistic load nor to maximize the system efficiency. Compared to previous works, my circuit can handle enough output load to power a typical microcontroller system, while maximizing the end-to-end efficiency over the entire load range. Additionally, my circuit does not require any external biasing, mechanical switches or any other tricks to start or improve performance of the circuit. The proposed circuit accomplishes all of this while only requiring a single input voltage source and three external components—an input capacitor, an output capacitor, and an inductor.

5.9 FUTURE WORK

Recent works related to energy harvesting place special emphasis on the minimum input voltage. To this end, it would be advantageous if this circuit could start up with an input voltage less than 240 mV. The minimum input voltage in the current design is determined by the minimum voltage at which the startup charge pump oscillator can function. The charge pump itself should be able to operate with an even lower input voltage, but the simple charge pump ring oscillator needs a voltage of at least 240 mV to function properly.

To this end, using a different kind of oscillator for startup could reduce the minimum input voltage. Either by designing a better CMOS oscillator or using an oscillator based on an external LC resonant circuit could potentially create an oscillating signal that runs at an even lower DC input voltage.

Additionally, the proposed circuit has been designed to use a DC input voltage with a very low equivalent series resistance. In a real application where a TEG transducer is used, the equivalent resistance of the transducer is rather large and cannot be ignored. Future work should also work on accurately modeling the input transducer and optimizing the circuit operation to work around this non-negligible resistance.

Part III

APPENDIX

A

MULTIPHASE BUCK CONVERTER LOAD TRANSIENT PERFORMANCE ANALYSIS THROUGH OUTPUT IMPEDANCE MEASUREMENT

The appendix of this report summarizes additional experiments that I performed at Gunma University but are outside the realm of energy harvesting. Additionally, while the results herein are interesting from an industry perspective, these investigations have not reached a point of breakthrough academic discoveries. It is hoped that further investigations will yield more rigorous theoretical results in the future.

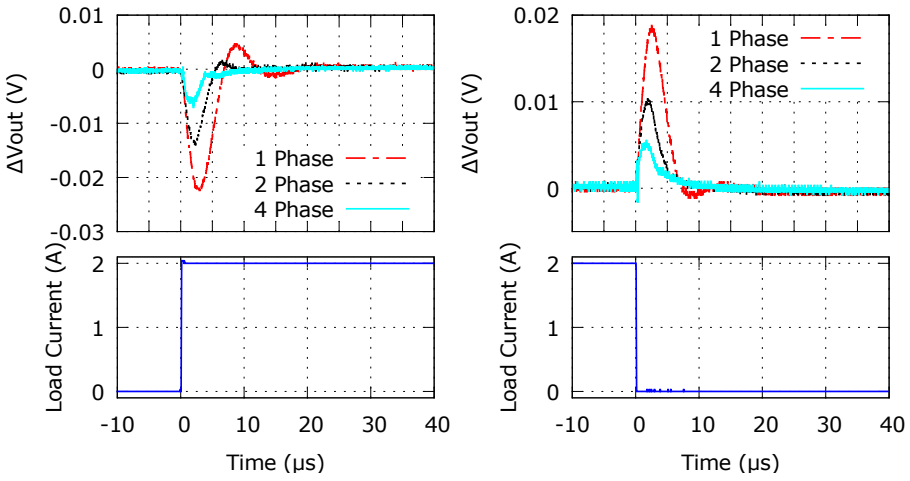
This chapter focuses on experiments on output impedance of a multiphase buck regulator. Results in this chapter were gathered using an NF 5095 Frequency Response Analyzer (FRA) and a DA9210 evaluation board provided by Dialog Semiconductor. The DA9210 part is a 4–phase buck regulator that can handle an output current of 12 A from a Li-ion battery input voltage.

A.1 BACKGROUND

In modern digital circuit design, the voltage fed to a microprocessor must be tightly controlled to ensure there are no bit-flips or other errors. Even over wide ranges of temperature, input/battery voltage or changes in load, the output voltage is only allowed to change by a few tens of millivolts. While DC variations in output voltage are mostly caused by the accuracy of the internal reference, dynamic variations are caused by the *load transient response* of the power supply.

The load transient response shows how the circuit reacts when the output load is changed. In the case of a microprocessor, the load requirements will change quickly based on the computation being performed. While power supply designers try their best to minimize the overshoot and undershoot during these load transient situations, there is always some amount of voltage ripple present, and if this is too large it can cause errors to occur in the microprocessor.

Figure A.1 shows an example of how the output voltage of a multiphase regulator responds to a step change in output current. Changing the output current causes the control loop to adjust to a new operating point, and based on the controller there may be ringing and a certain amount of overshoot and undershoot. The figure shows an overshoot/undershoot of about +18 mV/-22 mV and a small amount of ringing during 1 phase operation. Note that increasing the number of phases lowers the overshoot or undershoot of the load transient response.



(a) Positive load step.

(b) Negative load step.

Figure A.1: DA9210 load transient response, 1 phase 2.8 V.

The load transient response of a circuit is influenced by the frequency or rise time of the applied load step as well as the initial and final values of the load. Additionally, the control loop is generally affected by the input voltage of the circuit, the output voltage of the circuit and a number of other components that can be changed dynamically. Since the load transient response (ie the undershoot or overshoot of the output voltage) can change based on so many parameters, it can be difficult to test or guarantee a certain transient response over all conditions. But one way of easily testing the amount of overshoot or undershoot is by measuring the circuit's output impedance over a range of frequencies.

While previous works [21, 22] have discussed output impedance in power electronic circuits, they focus on design of the control loop instead of how the impedance of the circuit affects the dynamic circuit operation. The following sections will show how this output impedance measurement directly correlates with the load transient response of the circuit, and how output impedance measurements can guarantee the transient response.

A.1.1 *Impedance*

Recall from basic circuit theory that the equivalent impedance of a circuit is similar to the equivalent resistance of a circuit, though impedance is complex due to the time-dependent components in the circuit. The equivalent impedance of any circuit can be written as

$$Z(s) = \frac{V(s)}{I(s)}. \tag{A.1}$$

Note from this that if the impedance of a circuit under test is known and a certain current is applied, the resulting voltage can be calculated:

$$V(s) = Z(s) \times I(s). \tag{A.2}$$

To put this in a different form,

$$v(t) = \mathscr{L}^{-1}\{Z(s) \times I(s)\}. \tag{A.3}$$

Hence, by using Laplace transformations, the resulting output voltage can be determined as long as the equivalent impedance of the circuit is known. For an ideal capacitor or inductor, the impedance is $Z_C = 1/j\omega C$ and $Z_L = j\omega L$, respectively. In order to illustrate how these look over frequency, Fig. A.2 shows the impedance of several capacitors and inductors of different values. Note that the capacitor impedance lines slope downward as frequency increases while the inductor lines slope upward.

A.1.1.1 *Rise Time and Frequency Relationship*

While power electronics generally talks about pulses and square waves, practical signals have a finite rise and fall time. From the discussion in [23], a square wave with a low frequency ($f = 1/T$), 50% duty cycle and equal rise and fall times ($t_f = t_r$) has a frequency spectrum of:

$$c_n = \frac{A}{2T}\text{sinc}\left(n\omega_0\frac{T}{4}\right)\text{sinc}\left(n\omega_0\frac{t_r}{2}\right)\mathrm{e}^{-jn\omega_0\frac{T/2+t_r}{2}}. \tag{A.4}$$

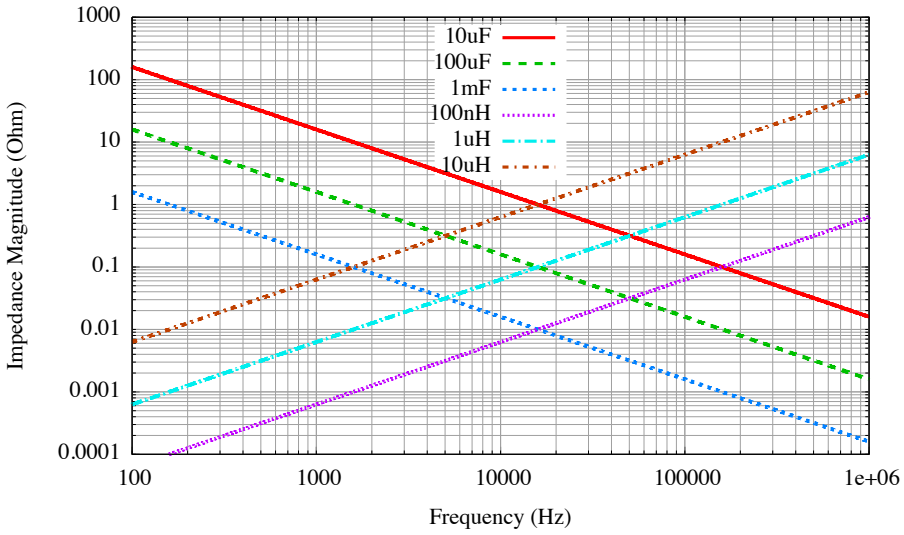


Figure A.2: Impedance of ideal inductors and capacitors.

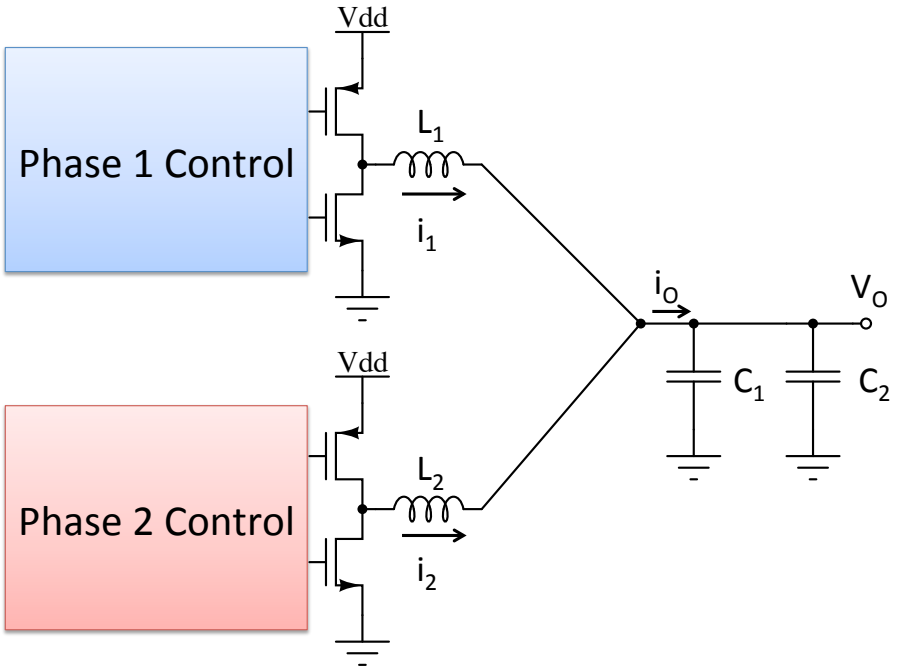


Figure A.3: Multiphase buck regulator conceptual schematic.

It can also be shown that the bandwidth of this signal is

$$f_{BW} = \frac{1}{\pi t_r}. \tag{A.5}$$

For modern mobile processor applications, the load step is on the order of 100 ns/A. For a load step from 0 A to 2 A with a rise time of 200 ns, the bandwidth is

$$f_{BW} = \frac{1}{\pi \times 200 \text{ ns}} = 1.59 \text{ MHz}. \tag{A.6}$$

This means that the energy of this signal is mostly below 1.59 MHz, hence the output impedance response below this frequency will predict how the circuit reacts to this load step.

A.1.2 *Multiphase Buck Regulator*

In modern mobile devices, the load current requirements for processors or SoCs keep increasing with newer generations. Since an individual buck regulator is limited in the amount of current it can supply, many designs have switched to a multiphase architecture, like the two-phase conceptual circuit shown in Fig. A.3.

If each phase of the circuit shown in Fig. A.3 is operated with a duty cycle of 25% and supplies a current of 1 A, it follows that the maximum output current is 2 A, as shown in Fig. A.4. By using this multiple phase approach, the output current can be increased by adding

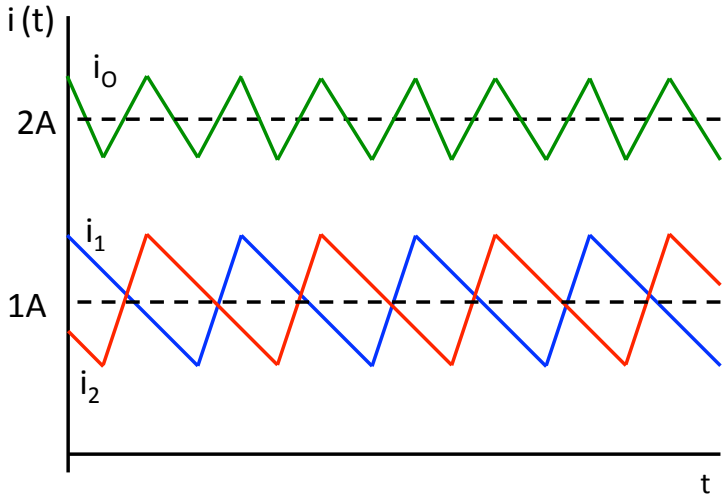


Figure A.4: Multiphase buck current waveforms.

more phases. The Dialog Semiconductor DA9210 is a 4-phase buck regulator, though it can be configured to operate from 1 to 4 phases.

A.2 BUCK REGULATOR OUTPUT IMPEDANCE

The open-loop output impedance of a buck converter (like that shown in Fig. 2.10) can be analyzed using the circuit in Fig. A.5. This circuit shows the output capacitor, inductor and a fixed load resistor as well as a model of the switch resistance based on the averaged model of the circuit and represented by r_L. By inspecting the circuit, that output impedance can be written as

$$Z_O(s) = \left(\frac{1}{sC} + r_C\right) \parallel (sL + r_L) \parallel R_L. \tag{A.7}$$

This can further be simplified as:

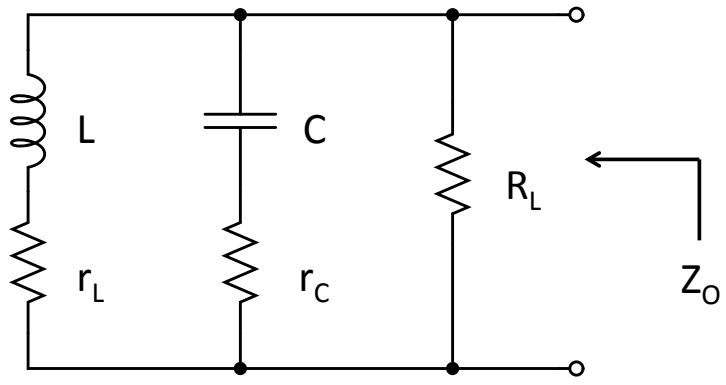


Figure A.5: Circuit to analyze open-loop output impedance of a buck converter.

$$Z_O(s) = \frac{R_L r_C \left(s + \frac{1}{Cr_C}\right)\left(s + \frac{r_L}{L}\right)}{(R_L + r_C)\left[s^2 + \left(\frac{L + r_L C(R_L + r_C) + (R_L C r_C)}{LC(R_L + r_C)}\right) s + \frac{R_L + r_L}{LC(R_L + r_C)}\right]} \tag{A.8}$$

By closing the feedback loop around this inductance, the closed loop output impedance can be expressed as:

$$Z_{O(cl)} = \frac{Z_O(s)}{1 + G_P(s)G_C(s)} \tag{A.9}$$

where $G_P(s)$ and $G_C(s)$ model the *plant* and *controller*, respectively. Simplifying further,

$$Z_{O(cl)} = \frac{Z_O(s)}{1 + T(s)} \tag{A.10}$$

where $T(s)$ is the overall loop gain of the circuit, including all control circuitry. This means that the actual value of the output impedance depends on the control loop of the regulator, and changes in the control loop (gain, compensation, etc) will have an effect on the output impedance of the circuit.

A.3 LAB SETUP

Output impedance was measured using the FRA5095 FRA from NF Corporation. A block diagram of the test setup is shown in Fig. A.6 and a photograph of the actual lab bench is shown in Fig. A.7. In this setup, the FRA creates a voltage signal at a certain frequency. This voltage signal is fed into the transconductance amplifier which turns the signal into a current; this current is then used to perturb the Device Under Test (DUT). By measuring the output voltage of the DUT across the load resistance (R_L), and measuring the test current (as the voltage drop over a 1 Ω sense resistor), the FRA can measure the impedance seen looking into the DUT.

A.3.1 *Transconductance Amplifier*

This lab setup relies heavily on the transconductance amplifier, whose abbreviated schematic is shown in Fig. A.8. The transconductance amplifier is a fairly standard voltage-to-current buffer with a gain of 200 mA / V. In the test setup, the DUT is earth grounded while the FRA and transconductance amplifier are floating, ensuring correct measurement results. Additionally, power for the transconductance

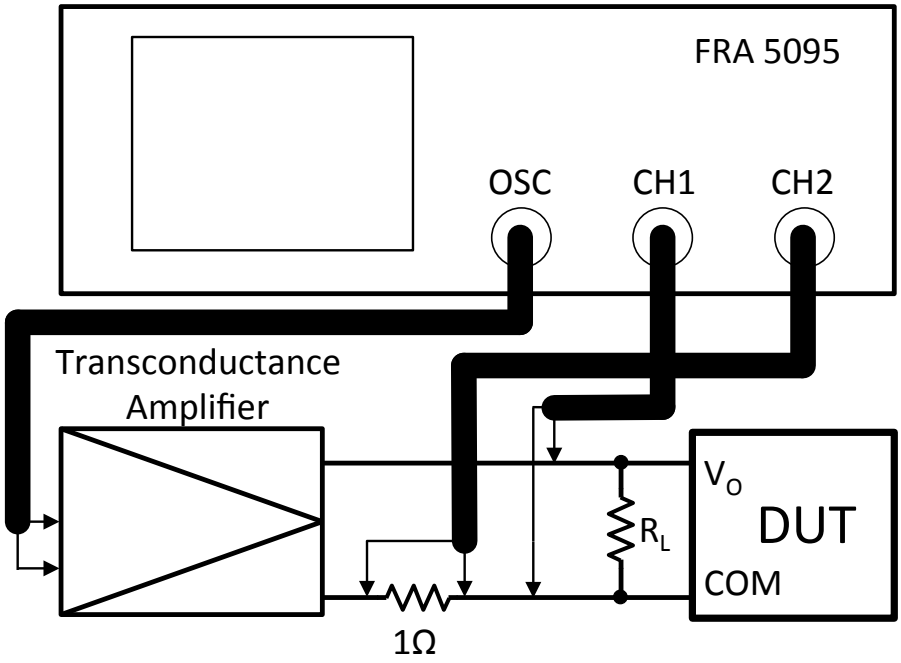


Figure A.6: Output impedance lab setup block diagram.

amplifier is supplied by a separate line voltage stepped down with linear regulators which is completely separate from the FRA or DUT. The 1 Ω sense resistor is embedded within the transconductance amplifier housing and is a 1% resistor with a power rating of 3 W.

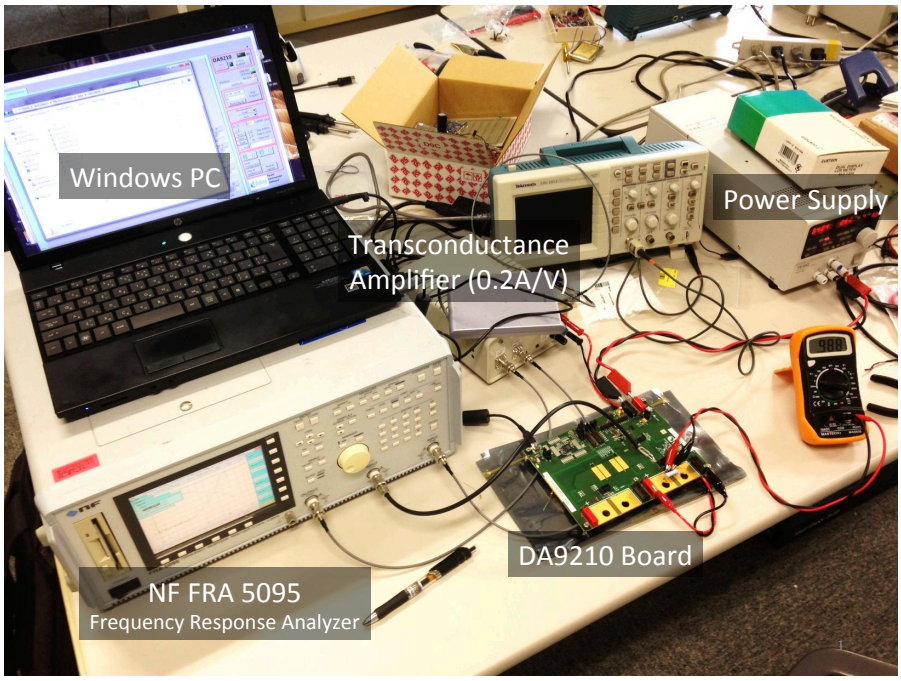


Figure A.7: Output impedance lab bench photograph.

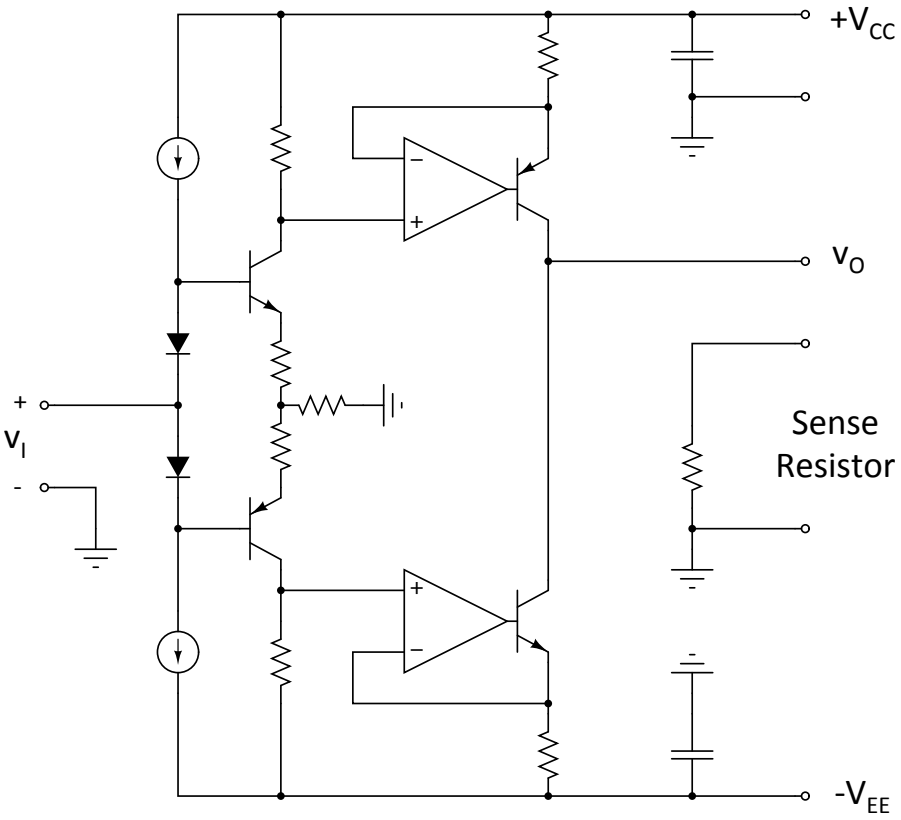


Figure A.8: Transconductance amplifier simplified schematic.

A.3.2 *Frequency Response Analyzer Settings*

Since the output impedance testing setup relies on injecting a current into the output load to disturb the circuit, the rule of thumb is that for an asynchronous power supply, we should inject a test signal (current) that is 10% of the load current. Since the DA9210 part is synchronous, a fairly large current can be injected even with no load, since the load current can be negative. Nevertheless, the injected signal should remain fairly small, and testing over various conditions showed that a 200 mV peak input signal from the FRA (injected current = 40 mA) is acceptable for measuring output impedance. Injecting a larger signal reduces the amount of noise seen in the response, but this also runs the risk of making the perturbation large-signal instead of small-signal. The other important settings used with the FRA are shown in Table A.1.

A.4 MEASUREMENT RESULTS

This section summarizes some of the output impedance measurement results for the DA9210 part.

Table A.1: Frequency response analyzer settings.

Parameter	Value
Input Voltage	200 mV Peak
Input Type	Sine Wave
Minimum f	100 Hz
Maximum f	2.2 MHz
Points per Decade	100
Averaging	50 Cycles

A.4.1 *Disabled Response*

The *disabled response* of the circuit is an interesting data point from an overall output impedance perspective. When the output impedance is measured with the converter disabled, only the effect of the output capacitor(s), load resistor and any parasitic impedances will be seen in the measured impedance.

Fig. A.9 shows the measured impedance when the DA9210 part is disabled, with no output load and 4×47 μF output capacitors connected from the output voltage to ground. From this plot you can see that at low frequency, the impedance looks like a capacitor, with a calculated value of 160 μF at 100 Hz. At high frequency however, the response looks like an inductor, due to parasitics in the traces on the board. At some point between these two extremes, there is a resonant valley frequency, which in this case was measured at 427 kHz.

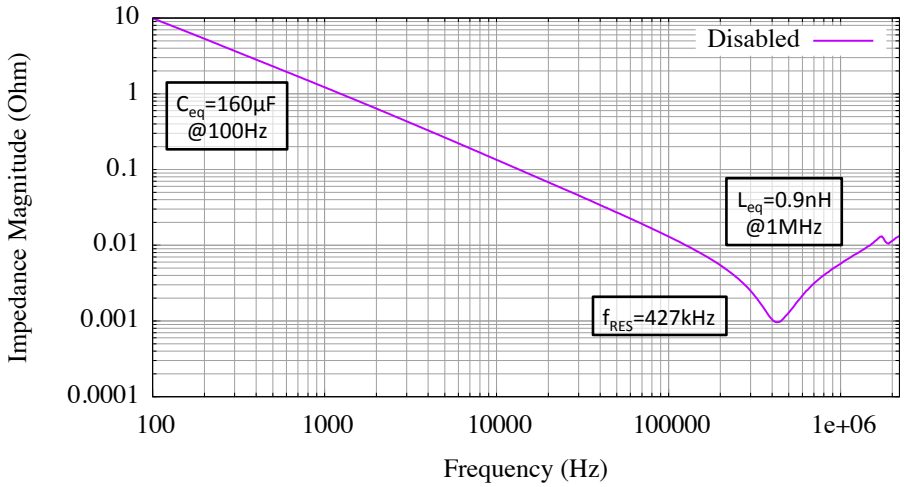


Figure A.9: Typical *disabled* impedance response.

A.4.2 *Single Phase Output Impedance*

The output impedance of the DA9210 was measured with the part in single-phase mode as shown in Fig. A.10. At low frequency, the output impedance of the converter is very low (<1 mΩ), which makes sense considering that a power supply generally has very good DC load regulation. Due to the scale of this figure, the maximum value of the disabled response can't be seen clearly, but it can be seen that the output impedance follows the disabled response at higher frequency, especially as the board parasitic inductance takes over around 1 MHz.

With an input voltage of 5.0 V, there is a slight spike in output impedance just above 1 MHz. This spike is due to sub-harmonic oscillation or *jitter*, which affects the duty cycle of the switch node. In a customer application, a little bit of jitter is not generally a problem, but any instability in the loop shows a large effect when measuring the output impedance with the FRA.

A.4.3 *Output Impedance as a Function of Number of Phases*

Increasing the number of phases during operation should decrease the overall output impedance of the circuit. If the output impedance of one phase is Z_O, then the output impedance as a function of the number of phases should be

$$Z_{eq} = \frac{Z_O}{\phi} \tag{A.11}$$

where ϕ is the number of phases that are switching.

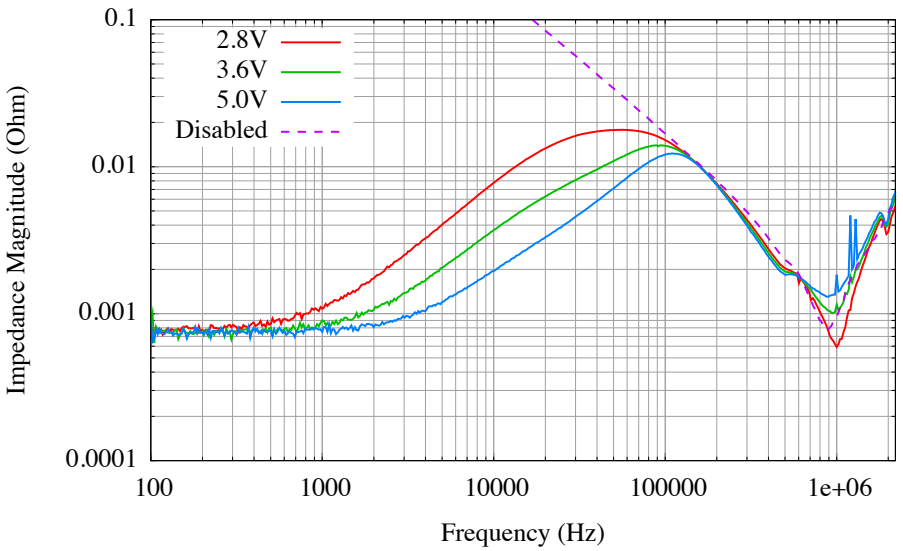


Figure A.10: Single phase output impedance response over V_{IN}.

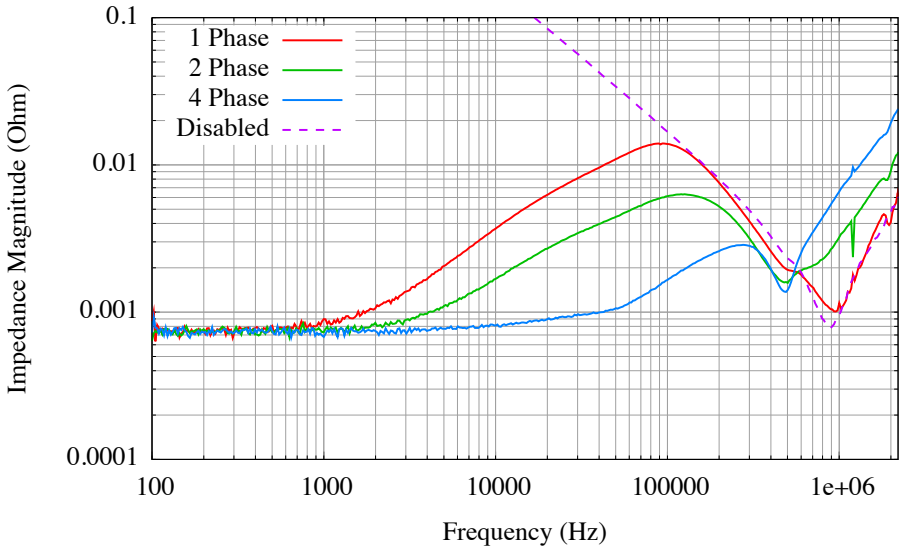
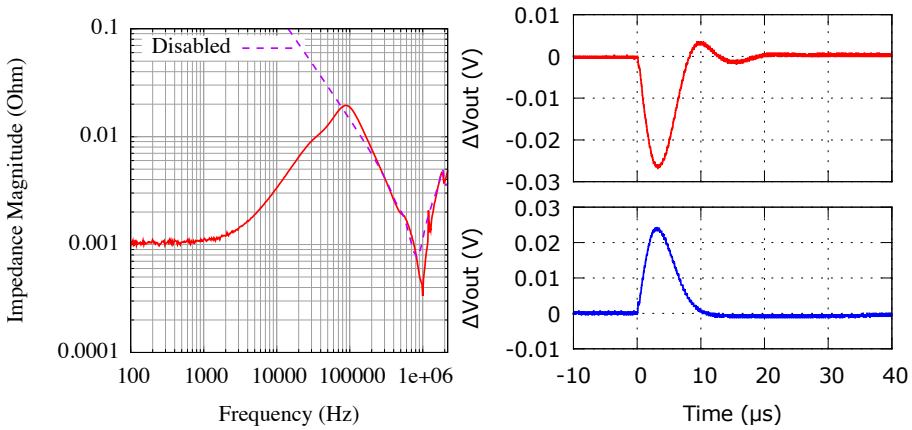


Figure A.11: Output impedance with a constant input voltage but number of phases changed.

Fig A.11 shows the output impedance response with the number of phases changed. Around a frequency of 100 kHz, we can see that 2 phase has a lower impedance magnitude than 1 phase, and 4 phase has a lower magnitude than 2 phase. At higher frequency (>1 MHz), the magnitude of the 2– and 4–phase curves is higher than the 1–phase and disabled curves. The cause of this discrepancy is still under investigation.

A.4.4 *Measured Load Transient Response*

Fig. A.12 shows output impedance and the load transient response of the circuit during 1 phase operation with an input voltage of 2.8 V.



(a) Positive load step.

(b) Measured output impedance.

Figure A.12: Measured load transient response (0A→2A).

The load step in this case is a 0 A→2 A→0 A current with a rise/fall time of 200 ns.

Under these conditions, the output impedance shows a peak of about 20mΩ at a frequency just under 100kHz. This would predict a worst-case overshoot and undershoot of

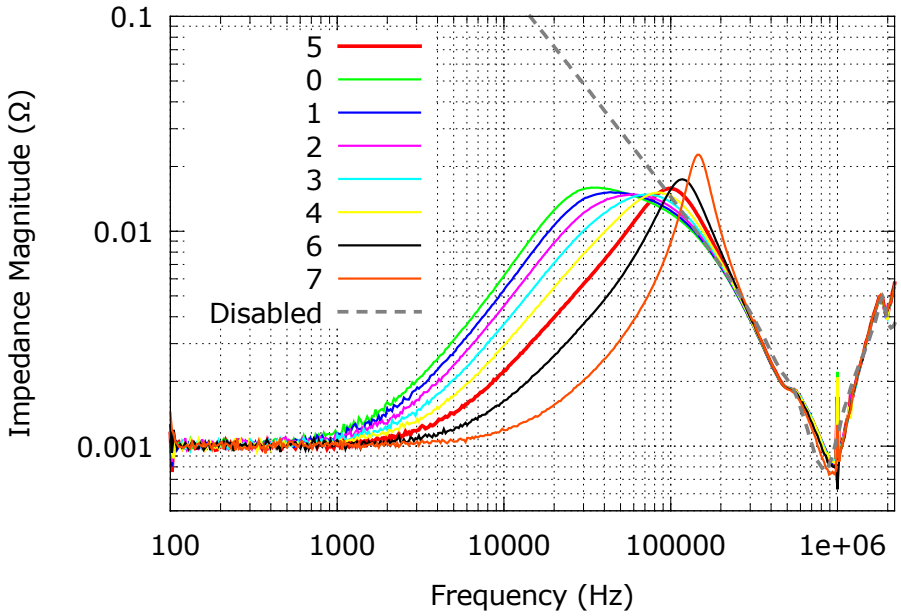
$$\Delta v_{wc} = Z_O(f_{peak}) \times I_O = 20\ \text{m}\Omega \times 2\ \text{A} = \pm 40\ \text{mV} \tag{A.12}$$

but Fig. A.12b shows that the overshoot and undershoot are +24 mV and -26 mV, respectively. From this result, we can see that there is a difference between the peak value predicted from the output impedance measurement and the observed load transient response.

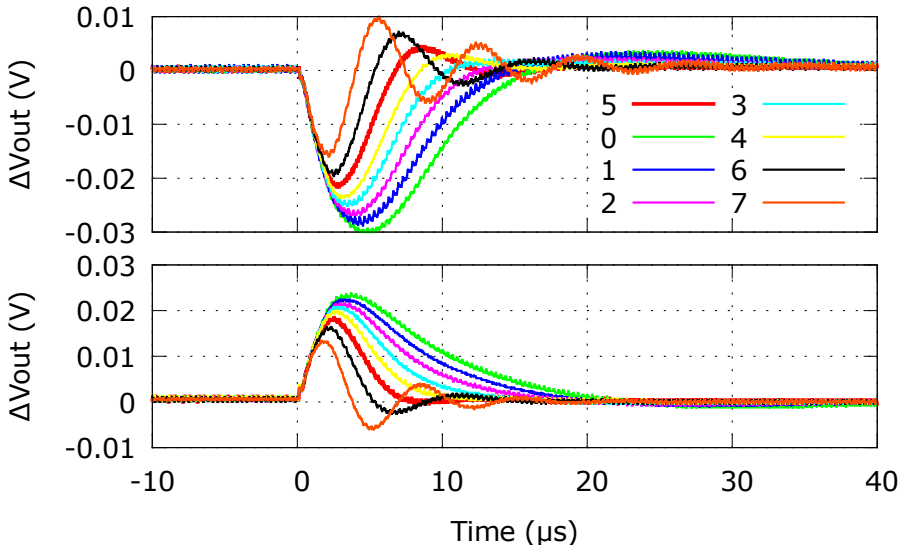
A.5 COMPENSATION EFFECT ON OUTPUT IMPEDANCE

The preceding output impedance data points have all been taken with the default compensation settings around the error amplifier. Fig. A.13 shows the effect of changing the location of the 1st compensation pole. The different lines represent different compensation codes, with '0' indicating a pole at a lower frequency (lower bandwidth) and '7' indicating a pole at a higher frequency (higher bandwidth). All data points were taken in 1 phase operation with an input voltage of 3.6 V. The output impedance response is shown in Fig. A.13a while the response to a 0 A→2 A load step is shown in Fig. A.13b.

This plot shows an interesting correlation between measured output impedance and load transient response. With a higher control bandwidth, the circuit also operates with lower phase margin, as shown in the plots for trim code 7. Because of this low phase margin, there is a significant amount of ringing when the load step is applied. Accordingly, the output impedance measurement predicts that this ringing will occur, based on the large peak seen in the output impedance measurement. Changing the trim code from 7 to 6 both reduces this peak and moves it to a lower frequency. In the time-domain, this corresponds to lowering the peak-to-peak ripple and frequency of oscillation during a load transient response.



(a) Output Impedance Response



(b) Load Transient Response

Figure A.13: Output impedance based on compensation pole trim code.

A.6 FUTURE WORK

Although the output impedance data collected so far for the DA9210 is preliminary, the results are interesting and there is good agreement between the measured output impedance and the load transient response of the circuit.

It has been suggested that a mathematical model of the output impedance of this converter could be constructed. By including phase information and matching the location of poles and zeroes, it should

be possible to create an open-loop circuit model to simulate the output impedance of this converter.

The next steps for this project are both to create an equivalent circuit model, as well as continuing to run the circuit over various conditions (different output capacitors, inductors, etc).

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