DYNAMIC PERFORMANCE ANALYSIS AND IMPROVEMENT FOR DC-DC BUCK CONVERTER

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Dynamic Performance Analysis and Improvement for DC-DC Buck Converter

DISSERTATION

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Declaration

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person, nor material which has been accepted for the award of any other degree of the university or other institute of higher learning, except where due acknowledgement has been made in the text.

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Abstract

The purpose of this dissertation is improving the dynamic performance for switching converter. The continuous advancement of signal processing technologies for integrated circuits has posed stringent challenges to power supplies. Higher speed clock, faster dynamic current slew rate and lower output voltage require improving the dynamic performance of switching converter.

Chapter 2 reviews three basic topologies of switching converter. The structure, steady-state equivalent circuit model and transfer function are introduced. Then focusing only on dc-dc buck converter, dynamic performance is analyzed in Chapter 3. From the frequency characteristic of loop gain, we can deduce the expression of transient response which caused by the variation in the reference signal, the input voltage and the load current. The results of these analyses lead the control system design for voltage-mode control and current-mode control. Although voltage-mode control is more advantageous than current-mode control, the gain-bandwidth product of op-amp severely limits the closed-loop bandwidth, and any change in the system must first be sensed as an output change. These usually mean bad dynamic performance.

Inspiration from the current-mode control, a slope adjustable triangular wave is introduced into voltage-mode control, instead of the conventional fixed triangular wave to compare to the control variable, and then generates pulse-width-modulated signal that is used to drive the switching elements. The proposed triangular wave slope is dependent on the input voltage and the deviation of the output voltage. The triangular wave generator (TWG) circuit is introduced in Chapter 4, and then the stability analysis and simulation result are included. Using the proposed TWG, both the load and line transient responses are improved. Since the TWG provides a line feed-forward control for the line transient response, it increases the closed-loop bandwidth, and then better dynamic performance is obtained. While the additionally required circuit components are only a voltage adder, a voltage controlled linear resistance and a voltage controlled current source. The proposed TWG is a simple-yet-effective method for improving dynamic performance of dc-dc buck converter.

In Chapter 5, the TWG is also applied in Single-Inductor Dual-Output buck converter to improve the cross-regulation.

CHAPTER I
INTRODUCTION

Now human depends on the electric more and more as the air. Maybe we sometimes ignore the importance of electric, but once you recall the convenience which electric brings to us, you must realize that so much amazing and essential change has happened. Over the last few decades, the development of electronic device is dizzying, especially the portable devices, as smart phone, PDA (personal digital assistant) and wearable device what boom starts in recent years. The continuously adding new features, increasing processor speeds, shrinking size and decreasing cost, all of them present challenge to the electrical power system.

1.1 POWER PROCESSING

The field of power electronics is concerned with the processing of electrical power using electronic device [1-7]. The key element is the switching converter, illustrated in Fig. 1.1. In general, a switching converter contains power input and control input ports and a power output port. The raw input power is processed as specified by the control input, yielding the conditioned output power [2].

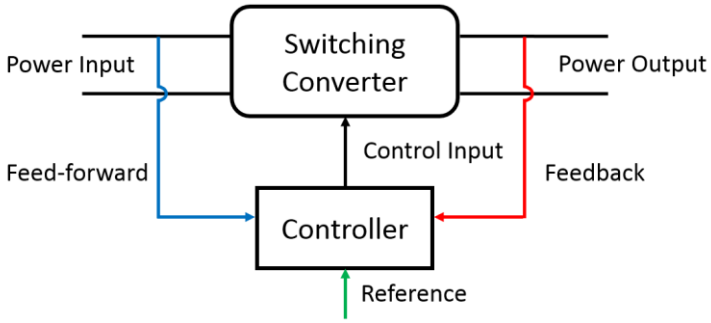


Fig. 1.1 The switching converter

Therefore, the control is invariably required. It is nearly always desired to produce a well-regulated output voltage or current, in the presence of variations in the input voltage and load current. A controller block is an integral part of any power processing system

By the different function and the type of input and output, the switching converter can be classified into dc-dc converter, ac-dc rectifier, dc-ac inverter and ac-ac cycloconverter. Normally, as the electronic power system of daily electronic devices, the ac-dc rectifier and dc-dc converter are widely utilized. In an ac-dc rectifier, an ac input voltage is rectified, producing a dc output voltage. The dc output and/or ac input current waveform could be controlled. It directly supplies power to home appliance, as television, refrigerator and so on, or works as a charging system for portable devices. In a dc-dc converter, the dc input voltage is converted to a dc output voltage having a larger or smaller magnitude. In a portable device, the charged battery supplies power to different components. While by different function, several different output voltages of dc-dc converter are required synchronously. In this dissertation, we should focus on dc-dc converter.

1.1.1 Efficiency

High efficiency is essential in any power processing application. The efficiency of a converter having output power P_{out} and input power P_{in} is

$$\eta = \frac{P_{out}}{P_{in}} \tag{1.1}$$

The power loss in the converter is

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right) \tag{1.2}$$

The continually adding new features in portable device require more power. At the same time, the standby time must be guaranteed. Except adopting a larger capacity battery, of course, the further increased efficiency is necessary. However, this is not the primary reason of pursuing high efficiency. In fact, consumers perceive little value in several percent increasing of power supply efficiency, and

no one will desire to save money on their electric bills through this way. Rather, high efficiency converters are necessary because of the system reliability. Since the most of power loss is dissipated on resistance element. This power is converted into heat. In a switching converter, the most common power loss happens on switching element what is constituted by MOSFETs or some other semiconductor components. No matter is the conduction interval or the switching interval, there is power which is dissipated on these switching elements and converted into heat which must be removed from the converter. In a low-efficiency converter, if without cooling system, the power loss will cause the electronic elements within the converter to operate at high temperature, and it reduces the system reliability.

1.1.2 Reliability

As the power technology roadmap which is published by PSMA in 2013 [8], although the reliability of power technology is not mentioned as the challenges in future directly, any improvement should be on the condition that maintaining reliability. However, it never can be obtained easily.

As mentioned, the purpose of high efficiency pursuit is to avoid the power loss and deterioration of the component's performance by heating, even destroy them. The research about electro-magnetic interference (EMI) tries to decrease the affects that is caused by either electromagnetic devices and avoid releasing electro-magnetic radiation that should effect the nearby device or components.

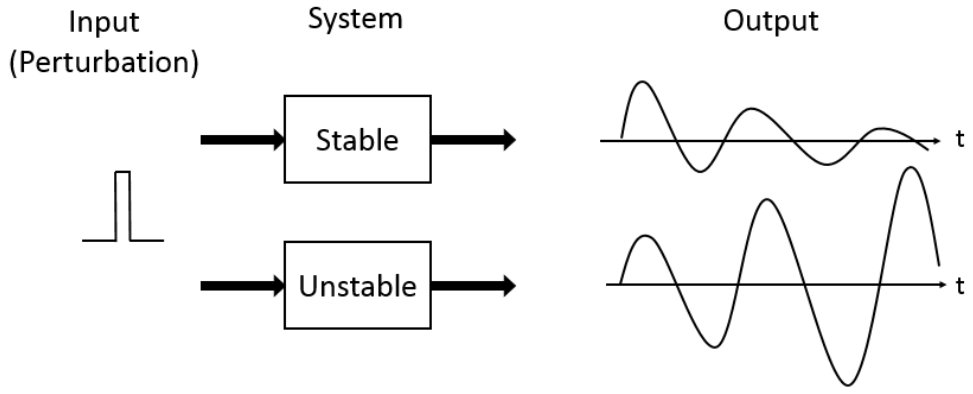


Fig. 1.2 Definition of stability

The control block in a power supply not only makes sure the circuit will work as setting, but also it plays a crucial role on insuring stability of the whole system. Fig. 1.2 gives a definition of stability. If a system is stable, when subjected to a perturbation from some source, its response to that perturbation eventually dies out [9].

It seems that there have been a lot of advanced technologies and control strategies, which are developed to maintain reliability. However, along with the high-speed development of integrated circuits, more stringent challenging will be presented to power supplies.

1.2 MOTIVATION AND OUTLINE OF THE DISSERTATION

Continuous advancement of signal processing technologies for integrated circuits has posed stringent challenges to the design of dc-dc converters. High-speed clock and fast dynamic current slew rate for advanced processors make the transient response performance of switching power supply to be more important. When we consider a stable power supply, there are three potential disturbance sources to take into account —the output reference signal, the applied input voltage and the load. Thanks to the well-developed band-gap reference circuit technology, we do not need worry about the reference signal. Input-voltage/line feed-forward control scheme ensures the system to be regulated as soon as the input voltage is changed. On the other hand, compared with these two disturbances, the load transient response is a troublesome issue.

During past twenty years, current mode control (CMC) is considered as a superior approach. Its reasons are not only that CMC has an inherent line feed-forward control, but also that CMC is easy to obtain wideband. A lot of researches for the load transient analysis of switching power supplies have indicated that higher bandwidth of the control loop can make enable faster load transient response [10-13]. However, the disadvantages of CMC (such as power loss caused by current sensor, additional slope compensation and complicated loop analysis)

give a revival chance to voltage mode control (VMC). By now, a VMC converter with the line feed-forward control has been proposed [14]. By using Type 3 compensation, the voltage mode control even can obtain comparable dynamic performance. Nevertheless, an expensive wideband amplifier is required. Some research also proposed using feed-forward controller to improve the load transient response. However, load current feed-forward control methods [15, 16] are limited in large load current transient conditions. Digital non-linear control methods have also been proposed [17, 18], but their main drawback is the complexity of non-linear calculation. Recently, hysteretic control scheme is very popular as its simple topology and fast transient response. However, the variable switching frequency of hysteretic control always causes unpredictable electromagnetic interference.

In order to improve the dynamic performance of dc-dc buck converter, this dissertation proposes a simple control method. This approach applies a slope adjustable triangular wave generator (TWG), and the slope of this triangular wave is regulated based on the input and output voltages. Therefore, we obtain not only line feed-forward control, but also load transient response improvement, because the feedback loop bandwidth is increased by a novel way, and the loop gain is modulated by a non-linear way. This dynamic performance improving method also can be used in single-inductor dual-output buck converter to improve the cross-regulation.

Chapter 2 introduces three basic topologies of switching converter---Buck, Boost and Buck-Boost. We will review the structure, steady-state equivalent circuit model and transfer function of them. The two most common feedback control schemes--- VCM and CMC also be included in this part.

Chapter 3 focuses only on Buck converter. The dynamic performance of Buck converter is analyzed by associating the frequency characteristics. This will help us to increase the insight of transient response. The limitation and challenge of improving transient response by conventional control scheme are illustrated.

Chapter 4 describes a simple-yet-effective control method for a dc-dc buck converter with VMC, with a TWG that regulates the slope of triangular wave based on the input and output voltages of the converter. Using the proposed TWG, both the load and line transient responses are improved. The SIMtrix simulation results show the effectiveness of the proposed method.

Chapter 5 introduces single-inductor dual-output (SIDO) buck converter. The cross-regulation phenomenon is the main drawback of this cost-efficient technique. The proposed TWG is applied to improve the dynamic performance of each sub-converter, and then the cross-regulation should be improved.

Chapter 6 gives the dissertation conclusions and further research directions. We will see the advantages of the proposed triangular wave slope modulation as follow:

Compare to CMC buck converter. Since the proposed method is based on voltage-mode control, it does not require current sensor and slope compensation. At the same time, it provides line feed-forward control and wide band what are the main advantages of CMC to VMC buck converter.

Compare to conventional VMC buck converter. The proposed method only requires a normal bandwidth op-amp to realize the Type 3 compensator, but can get a wider loop bandwidth. Especially, when the output voltage deviates from the reference signal, the loop gain non-linearly increases. Therefore, the buck converter has a temporary and very wide band during transient response. For line transient response, the line feed-forward control in [14] can only feed-forward the input variation. However, by the proposed method, the output voltage variation during line transient is also considered. It means the proposed method can provide better line transient response than the reference [14]. For load transient response, we need not current sensor which is necessary for load current feed-forward control in the reference [15,16]. And although the loop gain will non-linearly changes, in fact, we doesn't need to do the complicated non-linear calculation as in [17,18]. It means Analog-Digital Converter (ADC) and Digital Signal Processor (DSP) are not required. So that, the proposed method is low-cost and fast.

Compare to hysteretic control that has very fast transient response, the proposed method has comparable transient response and constant switching frequency. Although some research [23-26] have proposed variant method to overcome the disadvantages of the pure hysteretic control, the switching frequency still cannot keep constant during transient response, and this variable switching frequency always cause some unpredictable EMI problem.

The proposed method also can be applied in SIDO buck converter to improve cross-regulation. Unlike the time multiplexing control in [35] and the pseudo-

continuous conduction mode in [36] to force the inductor current operate under discontinuous conduction mode, the propose method improve cross-regulation just by improving load transient response for every sub-converter. This prevents large inductor current ripple.

CHAPTER II

FUNDAMENTALS OF SWITCHING CONVERTER

Normally, a dc-dc switching converter is constituted by switching element (transistor and diode), inductor and capacitor. There are several ways to set up circuits using these components. But some of these are usually disqualified because the input and output do not share a common rail, and thus there is no proper ground reference available for the converter and the rest of system. According to the way of the inductor connection, we have three available basic topologies: step-down type---Buck, step-up type---Boost and invert type---Buck-Boost. This chapter reviews their fundamental and analyzes the equivalent circuit model and the corresponding transfer function. Finally, the control system design is introduced.

2.1 BASIC TOPOLOGY

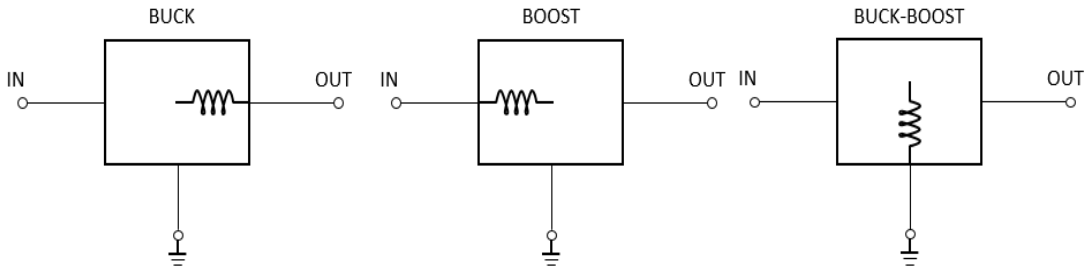


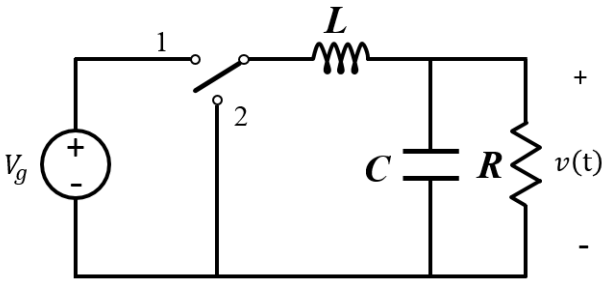
Fig. 2.1 Three basic topologies

There are three distinct rails possible for an inductor to be connected--- the output, the input and the ground. These three connecting ways realize three basic topologies of dc-dc switching converter. They are buck converter, boost converter

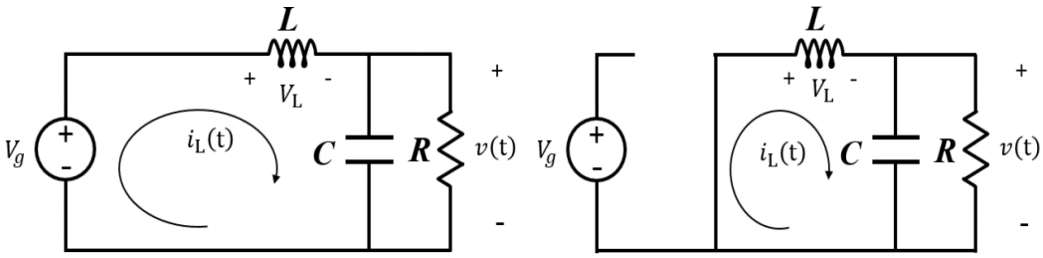
and buck-boost converter respectively, as shown in Fig. 2.1.

2.1.1 Buck converter

The converter of Fig. 2.2 is a buck converter with lossless elements. The switching elements has two positions, while this two positions switching element is realized by two transistors or one transistor plus one diode. When the switch is in position 1, the main switch is on. If the switch is in position 2, the main switch is off. The switch is set at these two positions alternately, and the circuit is operated at two different states accordingly, as shown in Fig. 2.2 (b) and (c)



(a) Buck converter circuit



(b) Switch is in position 1 (c) Switch is in position 2

Fig. 2.2 Buck converter

In order to analyze the steady state of switching converter, these two common principles are derived: inductor volt-second balance and capacitor charge balance.

Inductor volt-second balance is brought by the inductor equation

$$V_L = L\frac{\Delta I}{\Delta t} \tag{2.1}$$

During a steady state $\Delta I_{L\_on} = \Delta I_{L\_off} \equiv \Delta I$. Therefore, the product of the

voltage applied across inductor, multiplied by the duration which this voltage appears across the inductor must be equal. We get

$$V_{L\_on} \times t_{on} = V_{L\_off} \times t_{off} \tag{2.2}$$

Capacitor charge balance means that the charge and discharge of the output capacitor must be equal to each other, ensuring that the charge amount stored in the capacitor is maintained in a certain range. Otherwise, the output voltage will continually increase or decrease, meaning that the circuit will not reach to a steady state.

From the capacitor charge balance, a truth must be known that although the output voltage is desired as complete dc voltage, it is the sum of a dc component and an ac component. The ac component is generated at switching frequency and its harmonics. It is named as switching ripple $v_{ripple}(t)$. Hence, in practice the output voltage waveform $v(t)$ appears as illustrated in Fig. 2.3, and can be expressed as

$$v(t) = \mathrm{V} + v_{ripple}(t) \tag{2.3}$$

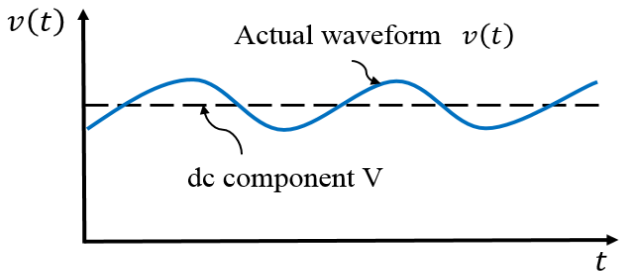


Fig. 2.3 Output voltage waveform consisting of dc component and switching ripple

However, from the buck converter circuit in Fig. 2.2 (a), we can see a low-pass filter which is constituted by the output capacitor and the load. It allows the dc component to pass but removes the switching ripple as much as it can. For a well-designed converter, the switching ripple is normally required to be less than 1% of the dc component. Therefore, it is always a good approximation to assume that the magnitude of the switching ripple is much smaller than the dc component

$$\left\| v_{ripple} \right\| \ll \mathrm{V} \tag{2.4}$$

Therefore, the output voltage can be approximated by the dc component with neglecting the small ripple term $v_{ripple}(t)$

$$v(t) \approx V \tag{2.5}$$

This is a useful approximation. The analysis of inductor volt-second balance is simplified. According to Fig. 2.2 (b) and (c), the voltage across the inductor during the switch turn on and off can be given by

$$V_{L\_on} = V_g - v(t) \approx V_g - V \tag{2.6}$$

$$V_{L\_off} = 0 - v(t) \approx -V \tag{2.7}$$

With the small-ripple approximation and a premise the circuit is operated under continuous current mode (CCM, it means that there always is a current through the inductor, even during the main switch off. Conversely, if the inductor current drops to zero during the main switch off, and keeps at zero until the next period starts, we can say that the circuit is operated under discontinuous current mode, DCM. (The discussion about DCM will be found in later section). The inductor current, capacitor current and the output voltage should be as shown in

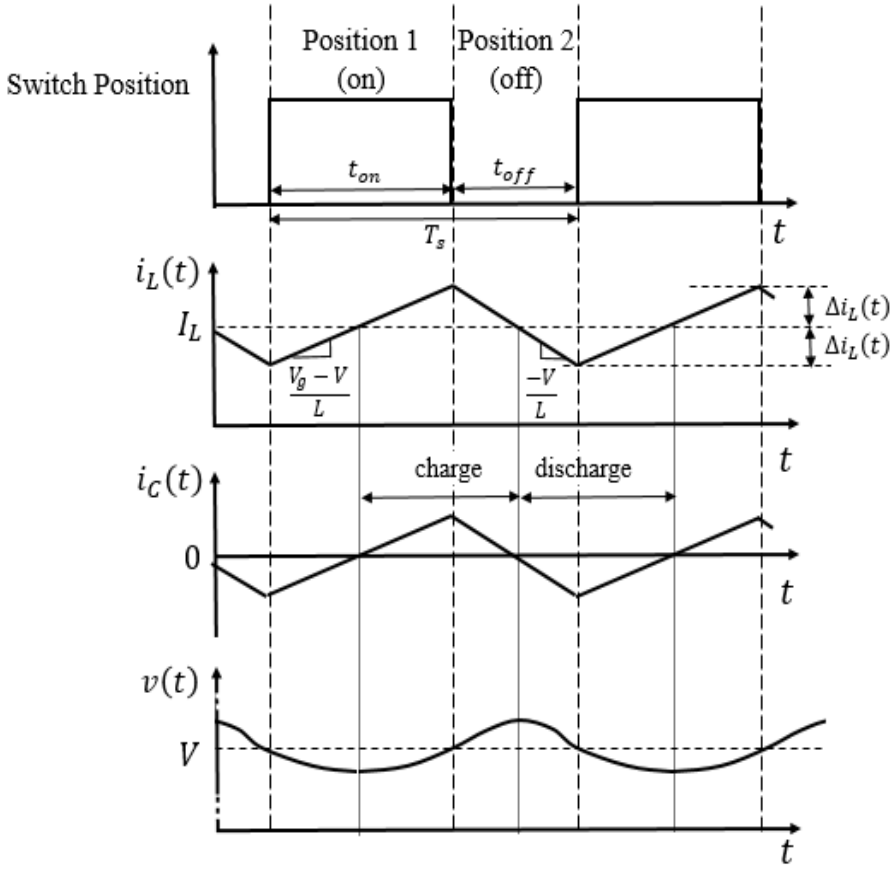


Fig. 2.4 Timing chart of buck converter

Fig. 2.4. When the switch is in position 1 (the main switch turns on), the inductor current increases with the slope $(V_g - V)/L$. When the switch is in position 2 (the main switch turn off), the inductor current decreases with the slope V/L. According the inductor volt-second balance

$$(V_g - V) \times t_{on} = V \times t_{off} \tag{2.8}$$

We can get the relation between the input voltage and the dc component of output voltage from Eq. (2.8), as

$$\frac{V}{V_g} = \frac{t_{on}}{t_{on} + t_{off}} \tag{2.9}$$

Since the circuit is operated under CCM, $t_{on} + t_{off} = T_s$. The ratio of t_{on} and T_s is named as duty cycle, it is denoted as D usually. Then Eq. (2.9) can be rewritten as duty cycle

$$\frac{V}{V_g} = \frac{t_{on}}{T_s} = D \qquad under\ CCM \tag{2.10}$$

Where $0 \leq D \leq 1$. Therefore, the output voltage of buck converter must be less than the input voltage.

The inductor is always connected to the output regardless of the switch position. The load current equals to the average of inductor current which is the dc component of actual inductor current---I_L. We can get

$$I_{out} = I_L \tag{2.11}$$

While, the input current flows through the inductor only during the main switch is on, therefore, the relation among the average of input current $\langle i_{in} \rangle$, the inductor current i_L are as shown in Fig. 2.5. It can be expressed as

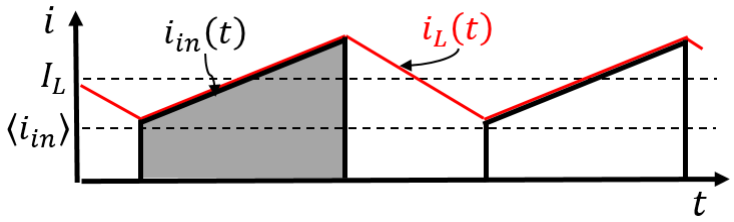


Fig. 2.5 The input current and the inductor current

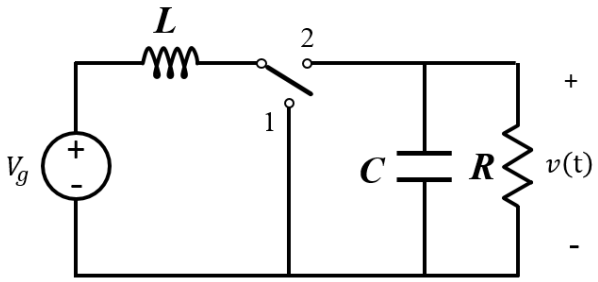
$$\langle i_{in}(t)\rangle = \frac{I_L \times t_{on}}{T_s} = I_{out} \times D \tag{2.12}$$

If the power loss in circuit is not considered, the input power and the output power are equal to

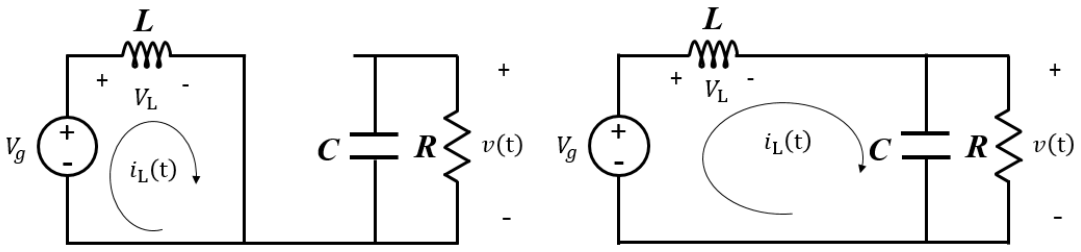
$$V_g \times I_g = \frac{V}{D} \times I_{out} \times D = V \times I_{out} \tag{2.13}$$

2.1.2 Boost converter

The converter of Fig. 2.6 is a boost converter with lossless elements. Similar to buck converter in previous section, the switch can be set at two positions alternately, and the circuit is operated at two different states accordingly, as shown in Fig. 2.6 (b) and (c)



(a) Boost converter circuit



(b) Switch is in position 1 (c) Switch is in position 2

Fig. 2.6 Boost converter

When the switch is in position 1, the inductor current increases by the slope V_g/L. When the switch is in position 2, the inductor current decreases by the slope $(V - V_g)/L$. The timing chart of a boost converter under steady state is shown in Fig. 2.7

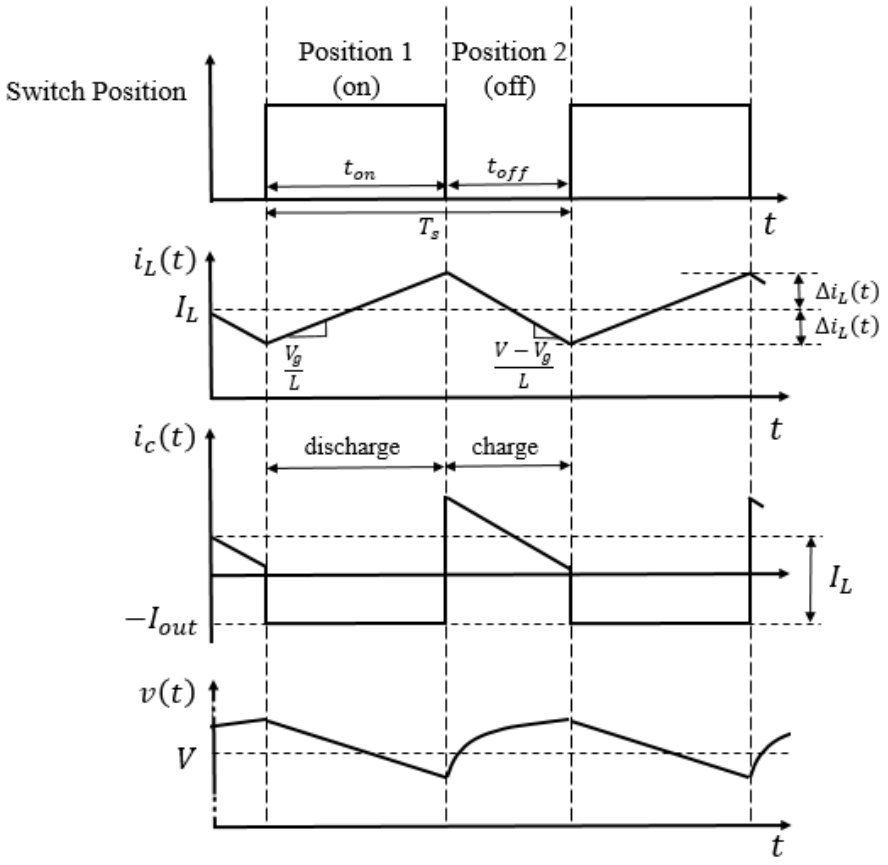


Fig. 2.7 Timing chart of boost converter

According to the steady-state principle of inductor volt-second balance, the relation between the input voltage and the output voltage is obtained

$$V_g \times t_{on} = (V - V_g) \times t_{off} \quad \Rightarrow \quad \frac{V}{V_g} = \frac{t_{on} + t_{off}}{t_{off}} = \frac{1}{1 - D} \tag{2.14}$$

Where $0 \leq D \leq 1$. Therefore, the output voltage of boost converter V must be larger than the input voltage V_g.

The inductor is always connected to the input port. The input current equals to the average of inductor current I_L. We can get

$$I_g = I_L \tag{2.15}$$

The load current is provided only by the output capacitor during the main switch turns on. Only when the main switch is turned off, the inductor current can flow to the load. Therefore, the relation between the inductor current and the load current is given in Fig. 2.8. It can be expressed as

$$I_{out} = \frac{I_L \times t_{off}}{T_s} = I_g \times (1 - D) \tag{2.16}$$

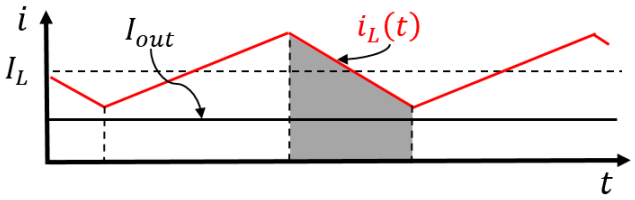
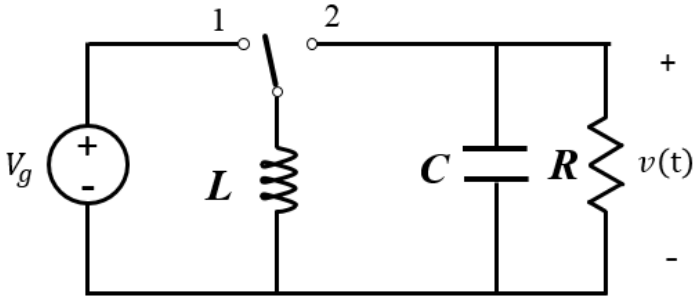


Fig. 2.8 The output current and the inductor current

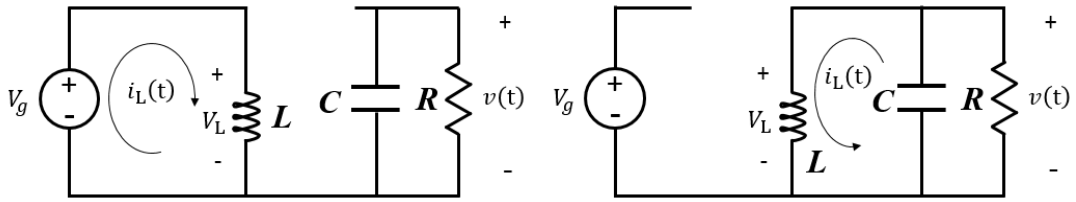
2.1.3 Buck-boost converter

The converter in Fig. 2.6 is a boost converter with lossless elements.

When the switch is in position 1, the inductor current increases by the slope V_g/L. When the switch is in position 2, the inductor current decreases by the slope $-V/L$. The timing chart of a buck-boost converter under steady state is as shown in Fig. 2.10



(a) Buck-boost converter circuit



(b) Switch is in position 1 (c) Switch is in position 2

Fig. 2.9 Buck-boost converter

According the steady-state principle of inductor volt-second balance, the relation between the input voltage and the output voltage is obtained

$$V_g \times t_{on} = -V \times t_{off} \quad \Rightarrow \quad \frac{V}{V_g} = -\frac{t_{on}}{t_{off}} = -\frac{D}{1-D} \tag{2.17}$$

From Eq. (2.17), we can know that the output of buck-boost converter is an inverting voltage. When $0 \leq D < 0.5$, the magnitude of output voltage is reduced, when $0.5 < D \leq 1$, the magnitude of output voltage is amplified, when $D = 0.5$, we can get $V = -V_g$.

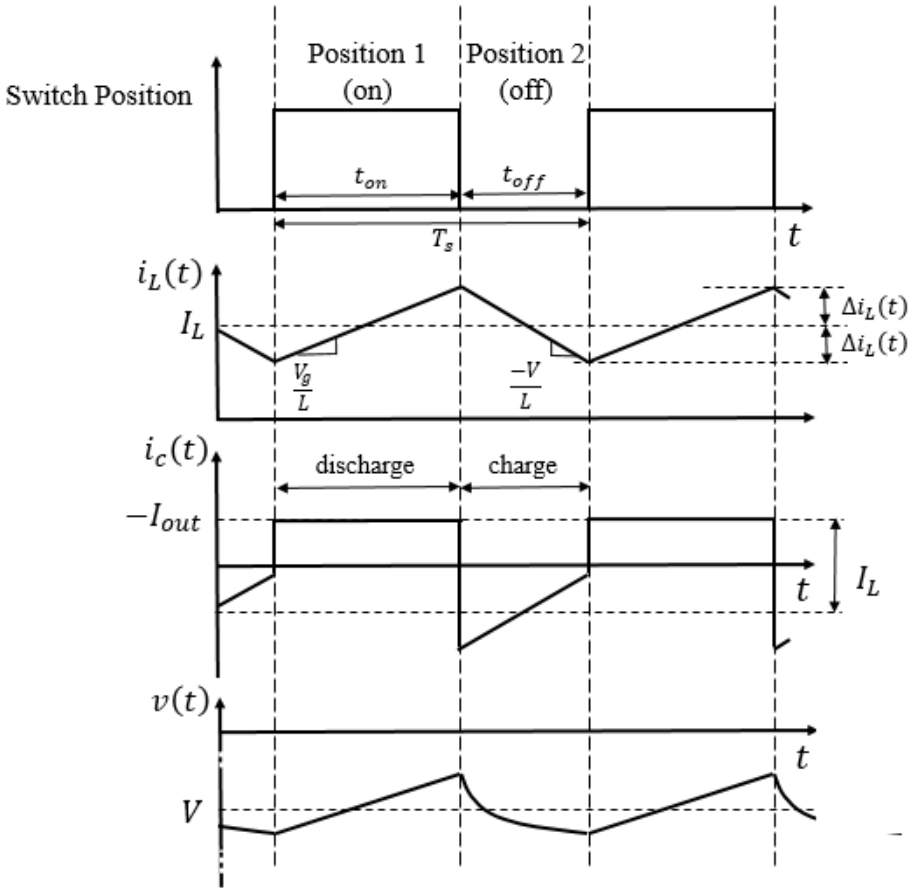


Fig. 2.10 Timing chart of buck-boost converter

One port of the inductor is always connected to the ground reference. The other port is connected to input during the main switch on. While, when the main switch is turned off, the connection with input is cut off, and then this port is connected to the output. Therefore, the relation among the input current, the output current and the inductor current is given by

$$\langle i_{in}(t)\rangle = I_L \frac{t_{on}}{T_s} \quad and \quad I_{out} = -I_L \frac{t_{off}}{T_s} \tag{2.18}$$

$$I_{out} = -\frac{(1-D)}{D} \times I_g \tag{2.19}$$

2.1.4 Power-loss element

In previous sections, the switching elements are assumed ideal and no power loss. However, the switching elements are actually realized by transistors and diodes. An actual buck converter is shown in Fig. 2.11

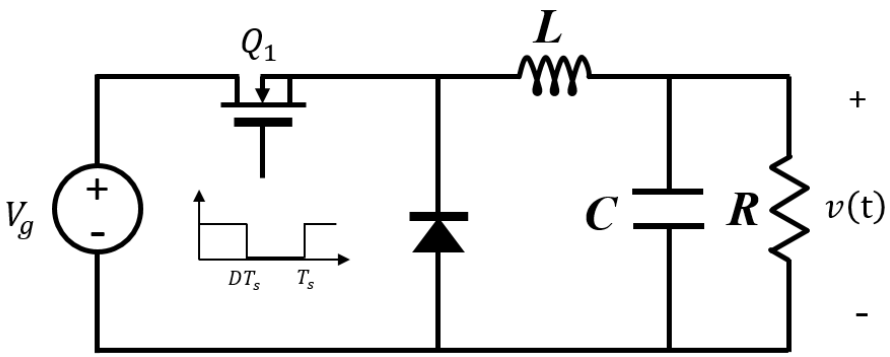


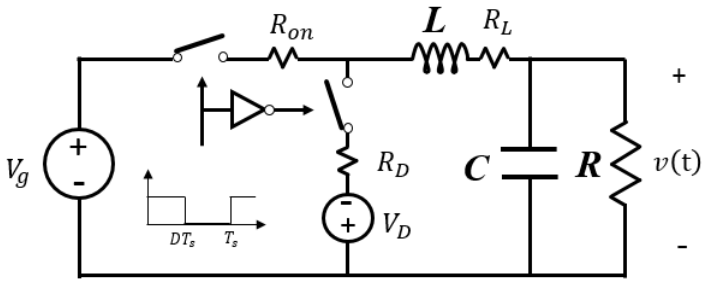
Fig. 2.11 An actual buck converter circuit

The metal oxide semiconductor field-effect transistor (MOSFET) and the diode both are not ideal switch. When MOSFET is conducted, there is a forward voltage between its two ends. This forward voltage can be modeled with reasonable accuracy as a voltage drop at on-resistance R_{on}. In the case of diode, a voltage source plus an on-resistance yields a model with good accuracy. A part of input power will be dissipated on these equivalent resistances.

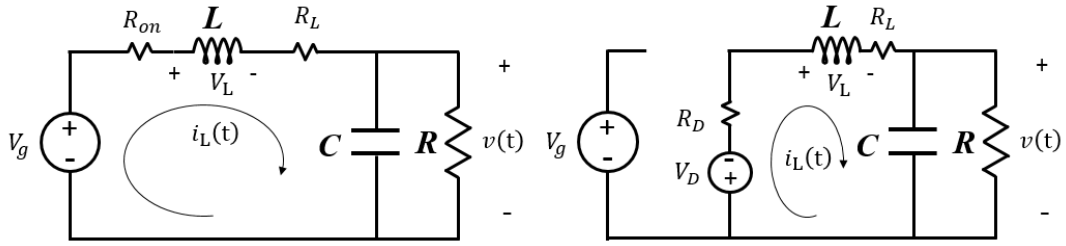
Another major source of power loss is the inductor copper loss. A suitable model that describes the inductor copper loss is an ideal inductor connected in series with a copper loss equivalent resistance R_L.

These equivalent resistances not only cause power loss, but also affect the relation between the input port and the output port. Considering the power loss element, let us examine the buck converter again. The equivalent circuit including

power loss elements is given by Fig. 2.12 (a), and the two state---MOSFET conducts and diode conducts are shown in Fig. 2.12 (b) and (c) respectively. The inductor current flows through these resistances to cause power loss and voltage drop. We know that the inductor current is consisted of a dc component I_L and a switching frequency ripple $2\Delta i_L$. Not like the output voltage, we cannot use small-ripple approximation to neglect the ripple in inductor current. But since these equivalent resistances normally are very small (tens of milliohm), using the product of the resistance multiplied by the dc component of the inductor current is a good approximation for simplifying analysis.



(a) Buck converter equivalent circuit with power loss element



(b) MOSFET conducts (c) Diode conducts

Fig. 2.12 The equivalent circuit of an actual buck converter

When the MOSFET conducts, the voltage across the inductor is given by

$$V_{L\_on} = V_g - \mathrm{V} - I_L(R_{on} + R_L) \tag{2.20}$$

When the diode conducts, the voltage across the inductor is given by

$$V_{L_{off}} = -\mathrm{V} - V_D - I_L(R_D + R_L) \tag{2.21}$$

According to the inductor volt-second balance

$$D\left(V_g - \mathrm{V} - I_L(R_{on} + R_L)\right) = D'\left(\mathrm{V} + V_D + I_L(R_D + R_L)\right) \tag{2.22}$$

Where $D' = 1 - D$. By collecting terms, one obtains

$$DV_g - \mathrm{V} - D'V_D - I_L\big(D(R_{on} + R_L) + D'(R_D + R_L)\big) = 0 \qquad (2.23)$$

In a buck converter, the dc component of inductor current is equal to the load current, therefore

$$I_L = I_{out} = \frac{V}{R} \qquad (2.24)$$

Substituting Eq. (2.24) into Eq. (2.23)

$$V = \big(DV_g - D'V_D\big)\frac{R}{R + DR_{on} + D'R_D + R_L} \qquad (2.25)$$

Dividing by V_g gives the voltage conversion ratio:

$$\frac{V}{V_g} = D\left(1 - \frac{D'V_D}{DV_g}\right)\frac{R}{R + DR_{on} + D'R_D + R_L} \qquad (2.26)$$

It can be seen that the effect of the power loss elements V_D, R_{on}, R_L and R_D is to decrease the voltage conversion ratio below the ideal value D.

From $P_{in} = V_g I_{in}$ and $P_{out} = VI_{out} = V\, I_{in}/D$, the efficiency is given by

$$\eta = \frac{V}{DV_g} = \frac{R\left(1 - \frac{D'V_D}{DV_g}\right)}{R + DR_{on} + D'R_D + R_L} \qquad (2.27)$$

For high efficiency, we require

$$DV_g/D' \gg V_D \quad \text{and} \quad R \gg DR_{on} + D'R_D + R_L \qquad (2.28)$$

For boost converter and buck-boost converter, we can get similar results. The voltage conversion ratios of boost converter and buck-boost converter with power loss elements are given by

$$Boost: \quad \frac{V}{V_g} = \frac{1}{D'}\left(1 - \frac{D'V_D}{V_g}\right)\frac{D'^2 R}{D'^2 R + DR_{on} + D'R_D + R_L} \qquad (2.29)$$

$$Buck - boost: \quad \frac{V}{V_g} = -\frac{D}{D'}\left(1 - \frac{D'V_D}{DV_g}\right)\frac{D'^2 R}{D'^2 R + DR_{on} + D'R_D + R_L} \qquad (2.30)$$

2.1.5 Discontinuous conduction mode

The discontinuous conduction mode (DCM) typically occurs with large inductor current ripple in a converter operating at light load and containing current-unidirectional switches (the semiconductor switches hold back reverses current). A buck converter as an example is used to explain the origins of DCM, and the mode boundary is derived. The buck converter is as shown in Fig. 2.11, the MOSFET and the diode conduct alternately. Along with the decreased load current, the inductor current will change from CCM to DCM, just as shown in Fig. 2.13

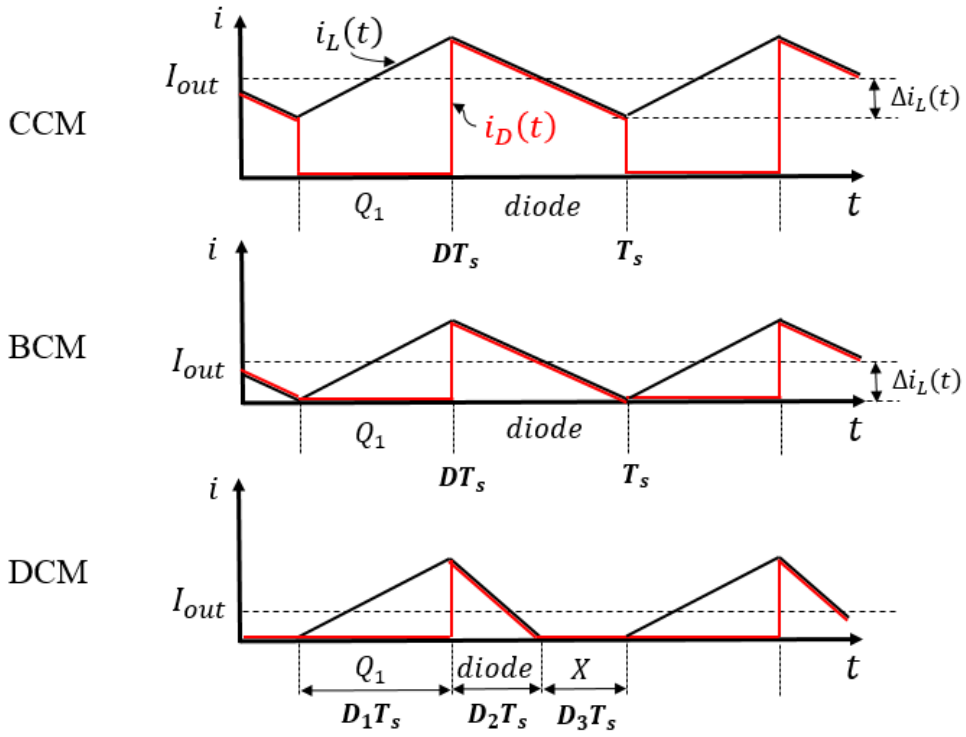


Fig. 2.13 The inductor current and diode current waveforms of a buck converter in CCM, BCM and DCM

We have known that the load current is equal to the dc component of inductor current in a buck converter, $I_{out} = I_L$. The switching ripple peak amplitude of the inductor current is

$$\Delta i_L = \frac{V_g - V}{2L} DT_s = \frac{V_g DD'T_s}{2L} \tag{2.31}$$

Suppose that the load resistance R is increased. Then the dc load current is

decreased, the dc component of inductor current will also decrease, but the ripple magnitude Δi_L will remain unchanged. When $I_L = \Delta i_L$, the inductor current $i_L(t)$ and the diode current $i_D(t)$ are both zero at the end of the switching period. This state is called boundary conduction mode (BCM).

If it is continued to increase the load resistance R, the diode current cannot be negative; therefore, the diode becomes reverse-biased before the end of the switching period. According to the previous description, we can get a criterion for finding the boundary between CCM and DCM, as

$$I_L > \Delta i_L \quad \text{for CCM}$$

$$I_L < \Delta i_L \quad \text{for DCM} \tag{2.32}$$

In a buck converter, we have the relation of $I_L = I_{out} = DV_g/R$. Insertion of Eq. (2.31) into Eq. (2.32) yields the following condition for operation in DCM

$$\frac{DV_g}{R} < \frac{V_g DD'T_s}{2L} \tag{2.33}$$

Simplification leads to

$$K < K_{crit}(D) \tag{2.34}$$

Where $K = 2L/RT_s$ and $K_{crit}(D) = D'$

The dimensionless parameter K is a measure of the tendency of a converter operating in DCM. Large values of K lead to CCM, while small values lead to DCM for the same duty cycle.

If the converter is operated in CCM, the voltage conversion ratio is independent of load. However, when the converter is in DCM, the conversion ratio becomes load-dependent. For example, a buck converter in DCM, according to volte-second balance, the output voltage can be expressed as

$$V = V_g \frac{D_1}{D_1 + D_2} \tag{2.35}$$

And the dc component of inductor current can be obtained by

$$I_L = \frac{1}{2} i_{peak}(D_1 + D_2) = \frac{(V_g - V)D_1 T_s}{2L}(D_1 + D_2) \tag{2.36}$$

Since $I_L = I_{out} = V/R$, from Eqs. (2.35) and (2.36), we obtain the voltage conversion ratio of buck converter in DCM, as

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + \frac{4K}{D_1^2}}} \tag{2.37}$$

Where $K = 2L/RT_s$ and $K < K_{crit}$.

The characteristics of the basic buck, boost and buck-boost converter are summarized in Table. 2.1.

Table. 2.1 Summary of DCM and CCM characteristics

Converter	$K_{crit}(D)$	DCM $M(D,K)$	*CCM* $M(D)$
Buck	$(1-D)$	$\frac{D^2}{2K}\left(\sqrt{1+4K/D^2}-1\right)$	D
Boost	$D(1-D)^2$	$\frac{1+\sqrt{1+4D^2/K}}{2}$	$\frac{1}{1-D}$
Buck-boost	$(1-D)^2$	$-\frac{D}{\sqrt{K}}$	$-\frac{D}{1-D}$

Since converters are usually operated with their loads removed, DCM is frequently encountered. Indeed, some converters are purposely designed to operate in DCM for all load.

2.2 EQUIVALENT CIRCUIT MODELING

For a converter system, only knowing voltage conversion ratio is not enough. For example, if there is some change in the input voltage $v_g(t)$ or in the effective load resistance R, the output voltage will be affected. We need more detailed

information to understand the relations between the output voltage and the variations in the system. Modeling is the representation of physical phenomena by mathematical means. This section describes the equivalent circuit modeling of dc-dc converter system.

Since the buck converter is the simplest topology, this dissertation is focused on the dynamic performance improvement of dc-dc buck converter. Although only the buck converter model is derived in this part, it is not hard to get the equivalent modes of boost converter and buck-boost converter by the same methodology.

2.2.1 DC transformer model

The dc transformer is used to model the ideal function performed by a dc-dc converter [19~22]. This simple model correctly represents the relationships between the dc voltages and currents of the converter. The model can be refined by including losses. The resulting model can be directly solved to find the voltages, currents, losses and efficiency in the actual non-ideal converter.

Considering an ideal converter with 100% efficiency, we have

$$V_g I_g = V I_{out} \tag{2.38}$$

In the previous sections, we used voltage conversion ratio to express the output voltage by the input voltage. According to the voltage relationship and Eq. (2.38), we can also express the input current by the load current

$$I_g = M(D) I_{out} \tag{2.39}$$

Where $M(D) = V/V_g$.

From Eq. (2.39), the converter could be modeled using dependent sources. The relationship of voltage and current in converter is similar to the voltage and current in a transformer system. The conversion ratio can be defined by the turns ratio. Although standard magnetic-core transformer cannot transform dc signals,

we still can use an imaginary dc transformer to model a dc-dc converter, as shown

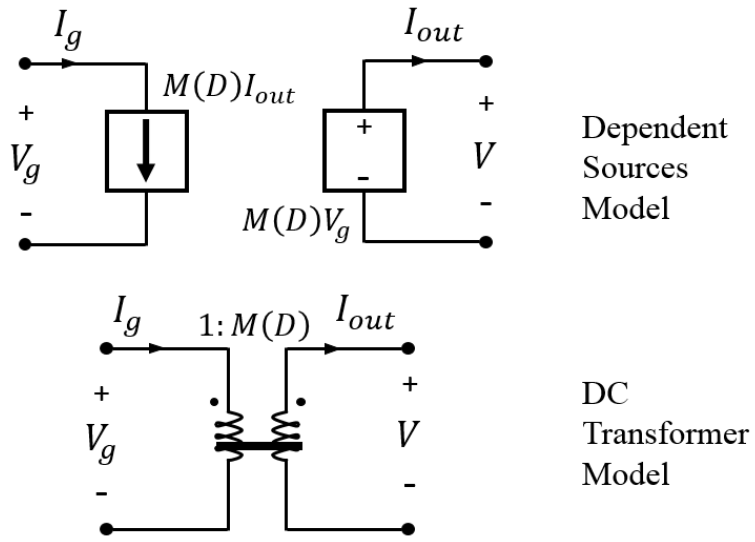


Fig. 2.14 Dependent sources model and dc transformer model

in Fig. 2.14

Let us use the dc transformer model to modeling a buck converter with power loss elements R_{on}, R_L, R_D and V_D. According to the volt-second balance principle, the average of the inductor voltage should be zero during one switching period. The inductor voltage of buck converter is shown in Fig. 2.15

The average of inductor voltage can be expressed as

$$\langle v_L(t)\rangle = 0 = DV_g - V - I_L(DR_{on} + D'R_D + R_L) - D'V_D \tag{2.40}$$

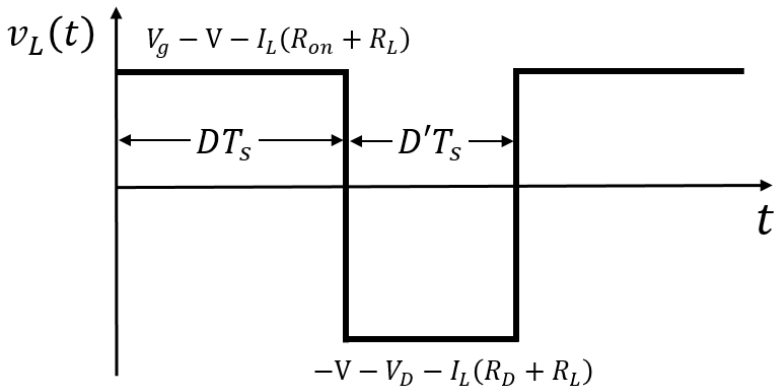


Fig. 2.15 Inductor voltage waveform for the non-ideal buck converter

Corresponding to Eq. (2.40), we can construct a circuit with a loop current I_L.

Using Kirchoff's voltage law, the circuit should be shown in Fig. 2.16

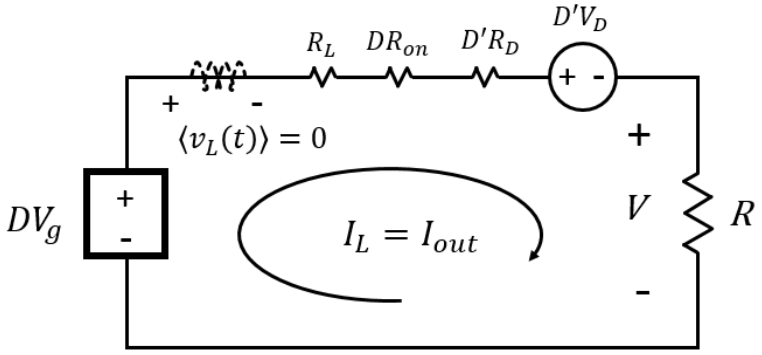


Fig. 2.16 Equivalent circuit corresponding to Eq. (2.40)

In previous section, we have derived the relationship between the input current and the dc component of inductor current, Eq. (2.12). Corresponding to this equation, we can construct the input port dc equivalent circuit, as shown in Fig. 2.17

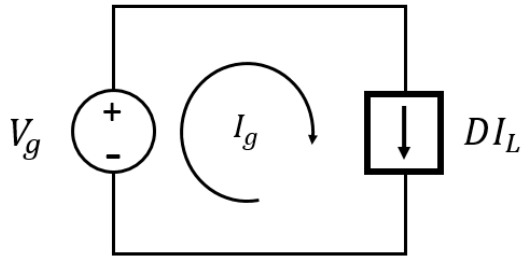


Fig. 2.17 Buck converter input port dc equivalent circuit

Combining Figs. 2.16 and 2.17, the dc transformer model of the non-ideal buck converter is represented by Fig. 2.18

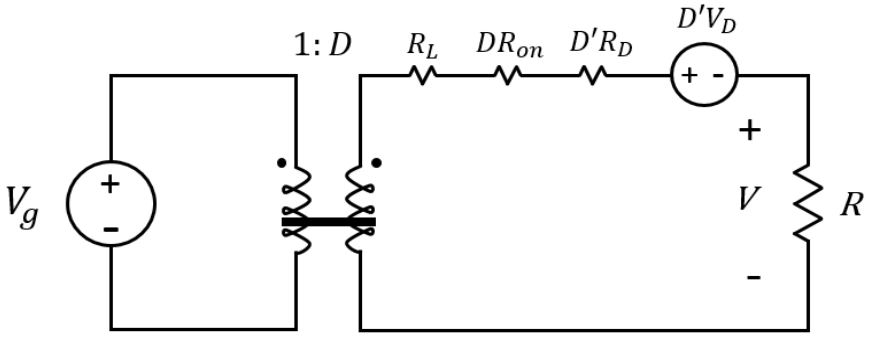


Fig. 2.18 Dc transformer model of non-ideal buck converter

2.2.2 AC equivalent circuit model

By dc equivalent model, we can refine the converter system with including power loss elements, and then the accuracy expression of voltage conversion and efficiency are obtained. However, the converter system is invariably required that the output voltage must be kept constant to be equal to a desired reference voltage, regardless of changes in the input voltage or in the effective load resistance. Therefore, a feedback loop is necessary to regulate the duty cycle in such a way that the output voltage is regulated to keep constant. It means that excepting the relationship of voltages and currents of converter under steady state, we need more detail information and relationship among the changed input voltage, the changed load, the duty cycle and the output. This section will construct the ac equivalent circuit model for an ideal buck converter.

Different from the dc model, we should plus a very small signal on all of the dc components. It means that there is a little change in the voltages, currents and duty cycle. Therefore, the ac equivalent circuit model is normally called small-signal model. Since the low-pass filter in converter system removes the ripple in high frequency, only the low-frequency change should be considered in ac circuit model. The average of voltages, currents and duty cycle during one switching period is given by

$$\begin{aligned} \langle v_g(t)\rangle_{T_s} &= V_g + \hat{v}_g(t) \\ \langle v(t)\rangle_{T_s} &= V + \hat{v}(t) \\ \langle i_L(t)\rangle_{T_s} &= I_L + \hat{\imath}_L(t) \\ \langle i_g(t)\rangle_{T_s} &= I_g + \hat{\imath}_g(t) \\ d(t) &= D + \hat{d}(t) \end{aligned} \tag{2.41}$$

The inductor voltage can be expressed as

$$\langle v_L(t)\rangle_{T_s} = L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = d(t)\big(\langle v_g(t)\rangle_{T_s} - \langle v(t)\rangle_{T_s}\big) - \big(1-d(t)\big)\langle v(t)\rangle_{T_s} \tag{2.42}$$

Inserting Eq. (2.41) into Eq. (2.42) and simplifying, we get

$$L\left(\frac{dI_L}{dt} + \frac{d\hat{\imath}_L(t)}{dt}\right) = \big(DV_g - V\big) + \Big(D\hat{v}_g + V_g\hat{d}(t) - \hat{v}(t)\Big) + \Big(\hat{d}(t)\hat{v}_g(t)\Big) \tag{2.43}$$

With the assumptions that the ac variations are small in magnitude compared to the dc quiescent values, we obtain

$$\begin{aligned} |\hat{v}_g(t)| &\ll |V_g| \\ |\hat{v}(t)| &\ll |V| \\ |\hat{\imath}_L(t)| &\ll |I_L| \\ |\hat{\imath}_g(t)| &\ll |I_g| \\ |\hat{d}(t)| &\ll |D| \end{aligned} \tag{2.44}$$

The dc terms in Eq. (2.43) have the relation

$$L\frac{dI_L}{dt} = (DV_g - V) = 0 \tag{2.45}$$

The 2nd order ac term $\hat{d}(t)\hat{v}_g(t)$ can be neglected. Eq. (2.43) rewrites as

$$L\frac{d\hat{\imath}_L(t)}{dt} \approx D\hat{v}_g + V_g\hat{d}(t) - \hat{v}(t) \tag{2.46}$$

Similarly, the input port can be expressed as

$$\hat{\imath}_g(t) \approx D\hat{\imath}_L(t) + \hat{d}(t)I_L \tag{2.47}$$

According to Eqs. (2.46) and (2.47), we can construct the small-signal ac equivalent circuit of an ideal buck converter as shown in Fig. 2.19

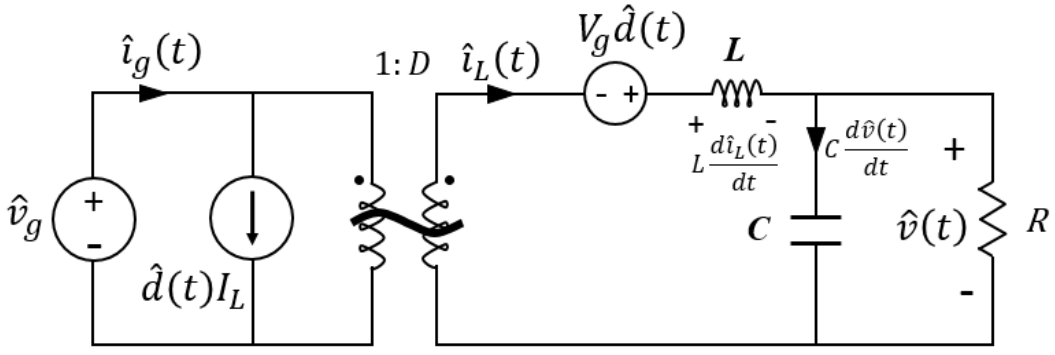


Fig. 2.19 Small-signal ac equivalent circuit model of ideal buck converter

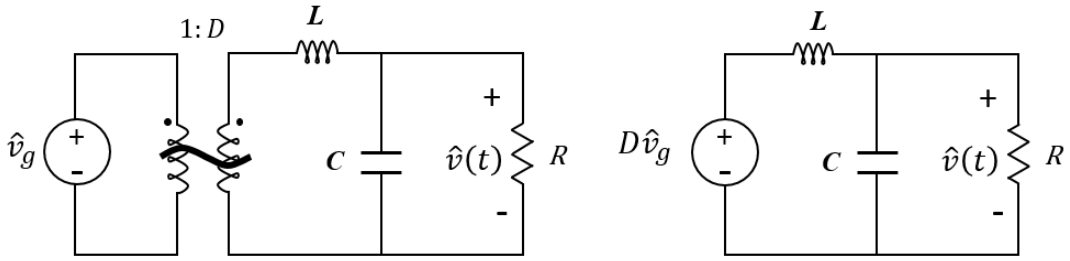
2.3 CONVERTER TRANSFER FUNCTION

In the engineering design process, after modeling the system, design-oriented analysis of the circuit is performed. The transfer functions help the design engineers to choose the element values to meet the specifications and design goals, and gain additional understanding and physical insight into the circuit behavior. Normally, for a dc-dc converter, the interested performance is the output voltage behavior that follows the variation in the input voltage $\hat{v}_g(t)$, load current $\hat{\imath}_{out}(t)$ and duty cycle $\hat{d}(t)$. According the small-signal ac equivalent model which is shown in Fig. 2.19, the transfer function of from the input voltage to the output voltage $G_{vg}(s)$, from the duty cycle to the output voltage $G_{vd}(s)$ and from the load current to the output voltage $Z_{out}(s)$ can be obtained.

Considering the transfer function $G_{vg}(s)$, the variation $\hat{d}(t)$ is set zero

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} \tag{2.48}$$

The small-signal model of buck converter is simplified as Fig. 2.20 (a). Then the rest source and element in primary side is moved to the secondary side of the $1:D$ transformer, as shown in Fig. 2.20(b)



(a) Set $\hat{d}$ sources to zero (b) Move $\hat{v}_g$ source through transformer

Fig. 2.20 Manipulation of buck equivalent circuit to find $G_{vg}(s)$

From Fig. 2.20(b)

$$\hat{v}(s) = D\hat{v}_g(s)\frac{\left(\frac{1}{Cs} \parallel R\right)}{\left(\frac{1}{Cs} \parallel R\right) + Ls} \tag{2.49}$$

Simplifying Eq. 2.49, the input-to-output transfer function $G_{vg}(s)$ is given by

$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} = \frac{D}{LCs^2 + \frac{L}{R}s + 1} \tag{2.50}$$

In order to obtain the transfer function from duty cycle to the output, similarly set all $\hat{v}_g$ sources to zero. In the buck converter equivalent circuit, if the $\hat{v}_g$ source in primary side of the $1:D$ transformer is set to zero, the current source

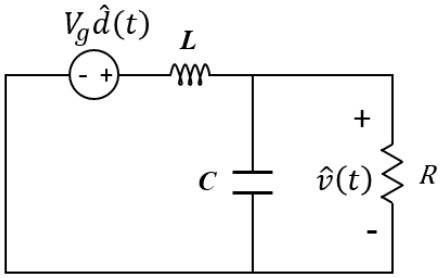


Fig. 2.21 Manipulation of buck equivalent circuit to find $G_{vd}(s)$ and set $\hat{v}_g = 0$

$\hat{d}I_L$ is shorted. The equivalent circuit should be as Fig. 2.21

The output voltage can be expressed as

$$\hat{v}(s) = \hat{d}(s)V_g \frac{\left(\frac{1}{Cs} \parallel R\right)}{\left(\frac{1}{Cs} \parallel R\right) + Ls} \tag{2.51}$$

Therefore, the transfer function from the duty cycle to the output voltage is

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0} = \frac{V_g}{LCs^2 + \frac{L}{R}s + 1} \tag{2.52}$$

The transfer function from the load current to the output voltage actually is the output impedances of the converter system

$$Z_{out}(s) = \left.\frac{\hat{v}(s)}{\hat{\imath}_{out}(s)}\right|_{\hat{v}_g(s)=0,\hat{d}(s)=0} \tag{2.53}$$

Both of $\hat{v}_g$ sources and $\hat{d}$ sources are set to zero, the equivalent circuit is as shown in Fig. 2.22

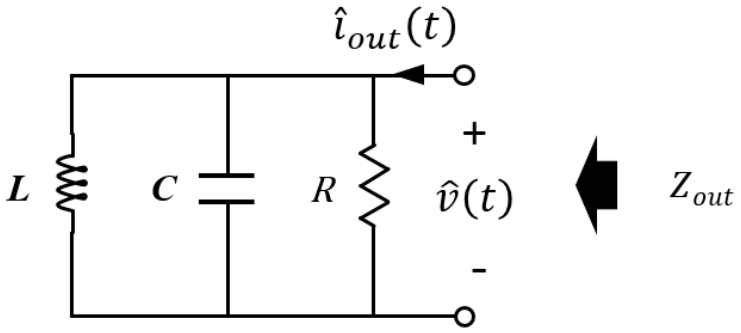


Fig. 2.22 The output impedances of a buck converter

The output impedance can be expressed as

$$Z_{out}(s) = Ls \parallel \frac{1}{Cs} \parallel \mathrm{R} = \frac{Ls}{LCs^2 + \frac{L}{R}s + 1} \tag{2.54}$$

We can find that all of these three transfer functions have the same denominator. The denominator can be written in the following standard normalized form

$$\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0\omega_0} + 1 \tag{2.55}$$

Where ω_0 is an angular corner frequency, and the parameter Q_0 is called as the damping factor or the quality factor of the circuit, and in buck converter, they equal to

$$\omega_0 = \frac{1}{\sqrt{LC}}, \qquad Q_0 = R\sqrt{\frac{C}{L}} \tag{2.56}$$

The transfer function whose denominator as Eq. (2.55) presents a second-order system. The effect of the corner frequency ω_0 and the damping factor Q_0

for the system should be shown as the Bode plot in Fig. 2.23.

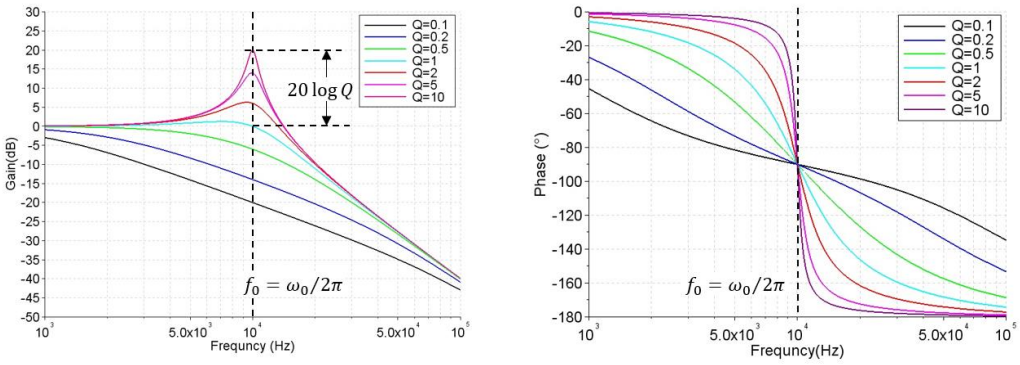


Fig. 2.23 Bode plot of second-order system

For example, a buck converter with $V_g = 10V$, $L = 1\mu H$, $C = 100\mu F$, $R = 5\Omega$ and $D = 0.5$. The corner frequency and the damping factor should be

$$\omega_0 = 10^5\ rad/s\ \ (f_0 = 10^5/2\pi\ \text{Hz}), \qquad Q_0 = 50 \tag{2.57}$$

The Bode plots of $G_{vg}(s)$, $G_{vd}(s)$ and $Z_{out}(s)$ as Fig. 2.24

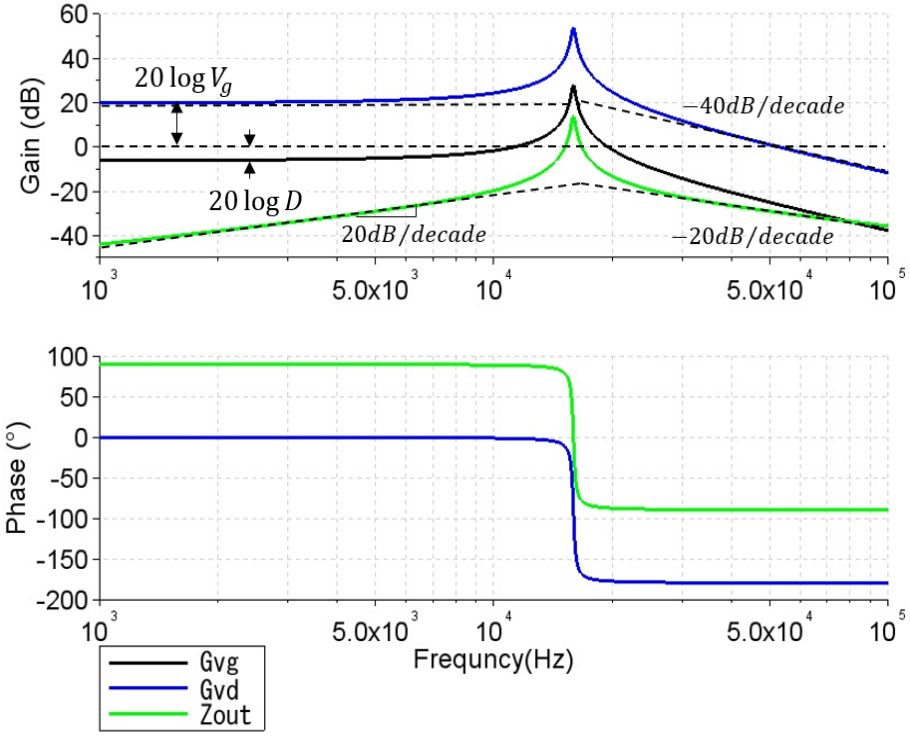


Fig. 2.24 Bode plots of the transfer functions

2.4 CONTROL SCHEME

The design objective of control system is keeping the output voltage at a constant value, regardless any disturbance. The feedback from output voltage is necessary. The information acquired from $v(t)$ is used to regulate the duty cycle $d(t)$. Then the regulated $d(t)$ affect $v(t)$ through the transfer function $G_{vd}(s)$. They constitute a closed loop to guarantee desired output voltage. In order to improve the dynamic performance, feed-forward control schemes are useful. The disturbance information is obtained and directly regulates the duty cycle. It let the duty cycle need not to wait the disturbance affect $v(t)$, and then get regulation through the feedback loop. However, although the feed-forward control scheme can effectively improve the dynamic performance, but normally, it cannot be used alone, because one feed-forward controller only corresponds to a particular disturbance. For example, the line/input feed-forward controller cannot sense the change in load current, of course there will not be any duty cycle regulation for this change. The output deviates from the desired value, and even the system becomes unstable. Therefore, feedback control is invariably required.

There are two common feedback control scheme. One is comparing the output voltage and the reference signal by an error amplifier, and then the error signal is compared to a fixed ramp signal. It is named as Voltage Mode Control (VMC). The other one also generates error signal as VMC, but the ramp signal is derived from the inductor current. It is named as Current Mode Control (CMC). These two control schemes can be called as pulse-width modulation (PWM) since the duty cycle regulation is realized by changing the width of fixed-frequency pulse signal. While, another recently emerging major thrust is actually heading towards hysteretic control which is very simple and has fast transient response.

2.4.1 PWM control

2.4.1.1 Voltage mode control

Fig. 2.25 illustrates a buck converter with voltage mode control. The output voltage is detected and divided by two high accuracy resistors, $\mathrm{H}(s)$ is denoted as the voltage divider gain. Then the output of voltage sensor is compared to a reference voltage signal V_{ref} which normally utilizes band-gap reference technology to avoid the temperature effect. An op-amp amplifies the deviation V_e between $\mathrm{H}(s)V$ and V_{ref} by the gain $G_c(s)$. This op-amp also be called as error amplifier, and it is very important in feedback control scheme. Since we need design the phase compensation to guarantee the system stability and get desired system performance, the error amplifier always is utilized to implement phase compensation. (The detail of the phase compensation design is included in next chapter, after the dynamic performance analysis). The amplified error signal

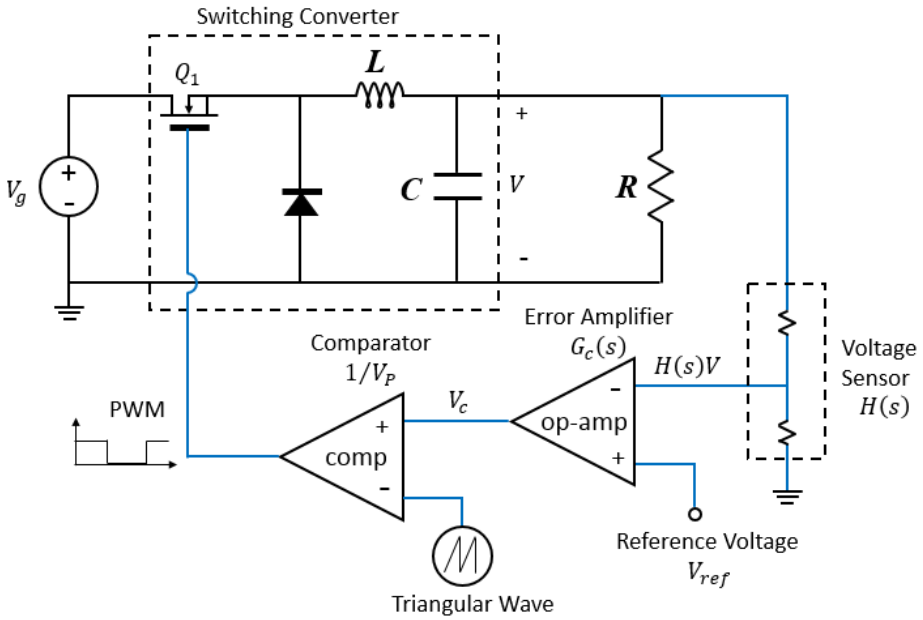


Fig. 2.25 Buck converter with voltage mode control

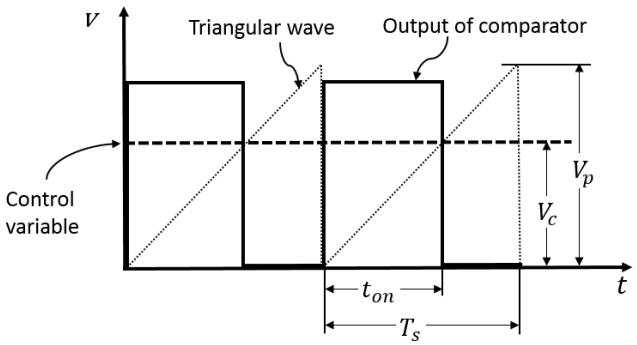


Fig. 2.26 Error signal and triangular wave generate PWM signal

V_c as control variable is compared to a triangular wave signal by a comparator. A PWM signal is generated as shown in Fig. 2.26. The PWM signal drives the transistor gate to control the switch Q_1 turn on or turn off, and the duty cycle is given by

$$D = \frac{t_{on}}{T_s} = \frac{V_c}{V_p} \tag{2.58}$$

Considering the system small-signal model with the voltage mode controller, the complete block diagram is as shown in Fig. 2.27

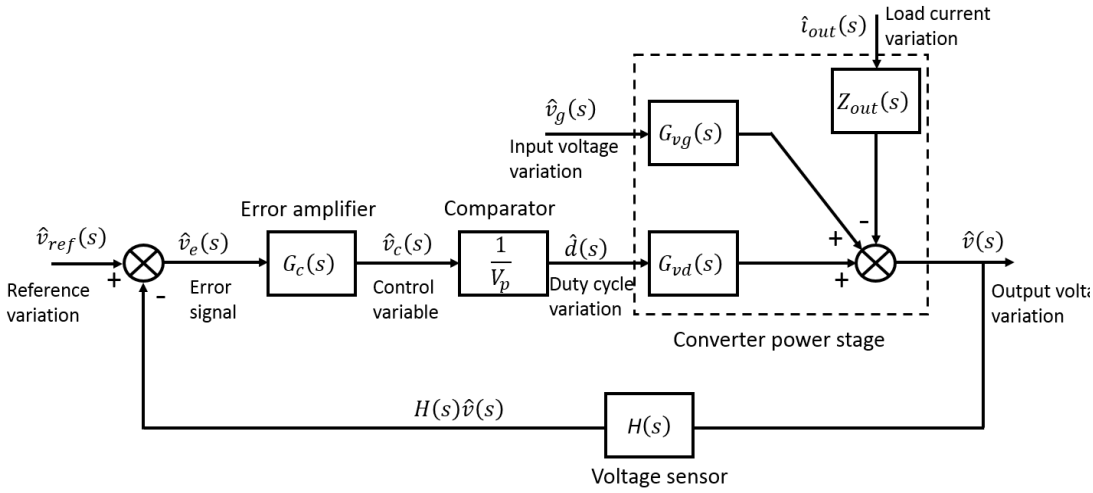


Fig. 2.27 Small-signal model of buck converter with voltage mode control

$G_c(s)$, $1/V_p$, $G_{vd}(s)$ and $H(s)$ constitute a feedback loop. There are three variation sources---reference signal, input voltage and load current. All of them will cause variation in output voltage. The output variation through the feedback loop regulates itself. The transfer function of feedback loop is given by

$$T(s) = H(s)G_c(s)G_{vd}(s)/V_p \tag{2.59}$$

First, consider the effect from reference signal to output, the input voltage and load current supposed as constant value, $\hat{v}_g(s) = \hat{\imath}_{out}(s) = 0$. We get

$$\left(\hat{v}_{ref}(s) - H(s)\hat{v}(s)\right) G_c(s)G_{vd}(s)/V_p = \hat{v}(s)$$

$$\Longrightarrow \quad \hat{v}(s) = \hat{v}_{ref}(s)\frac{1}{H(s)}\frac{T(s)}{1+T(s)} \tag{2.60}$$

The effect from input variation to output voltage can be expressed as

$$\big(0 - H(s)\hat{v}(s)\big)\, G_c(s)G_{vd}(s)/V_p + G_{vg}(s)\hat{v}_g(s) = \hat{v}(s)$$

$$\Longrightarrow \quad \hat{v}(s) = \hat{v}_g(s)\frac{G_{vg}(s)}{1+T(s)} \tag{2.61}$$

The solution of load current is similar to the input voltage. Finally, the output variation can be written in the form

$$\hat{v} = \hat{v}_{ref}\frac{1}{H}\frac{T}{1+T} + \hat{v}_g\frac{G_{vg}}{1+T} - \hat{\imath}_{out}\frac{Z_{out}}{1+T} \tag{2.62}$$

2.4.1.2 Current mode control

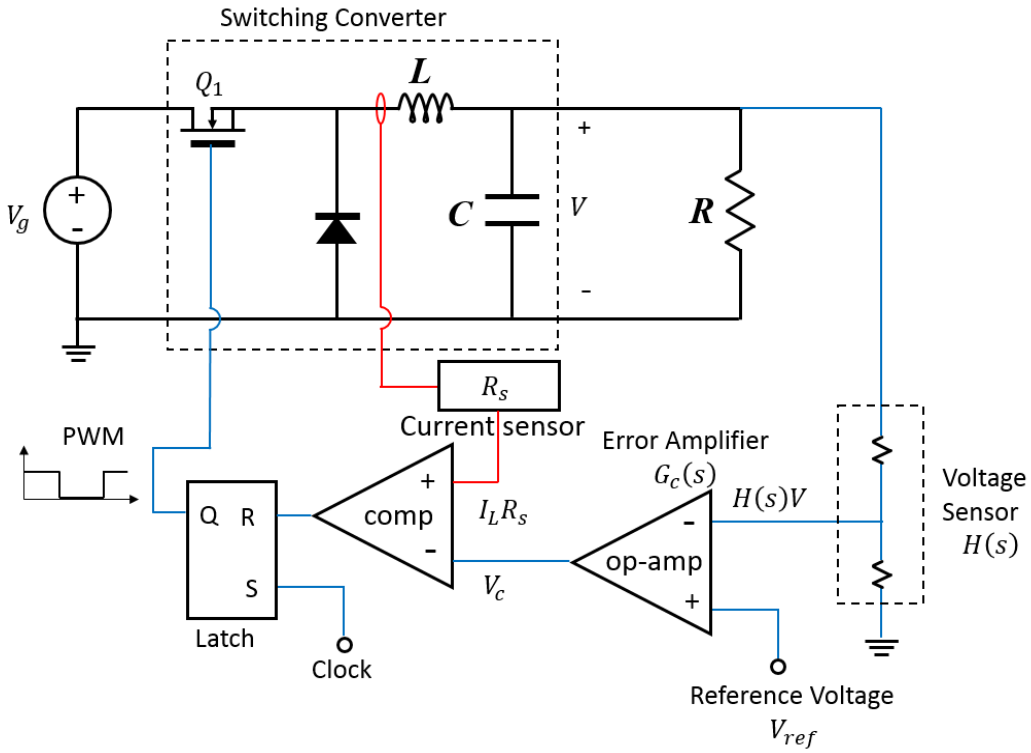


Fig. 2.28 Buck converter with current mode control

In voltage mode control, the triangular wave that compares to the control variable signal is applied by other generator circuit. The fixed frequency and peak value determine that the slope is constant. While, different with VMC, the

triangular wave in current mode control is derived from inductor current. The configuration of buck converter with CMC is illustrated in Fig. 2.28. Inductor current is transformed into a proportional voltage signal, and then compared to the control variable which is generated by the error amplifier as VMC. A fixed-frequency oscillator initially sets the latch which turn on Q_1, causing inductor current to rise. When the proportional voltage signal $I_L R_s$ crosses the control variable V_c, the comparator resets the latch turning off Q_1.

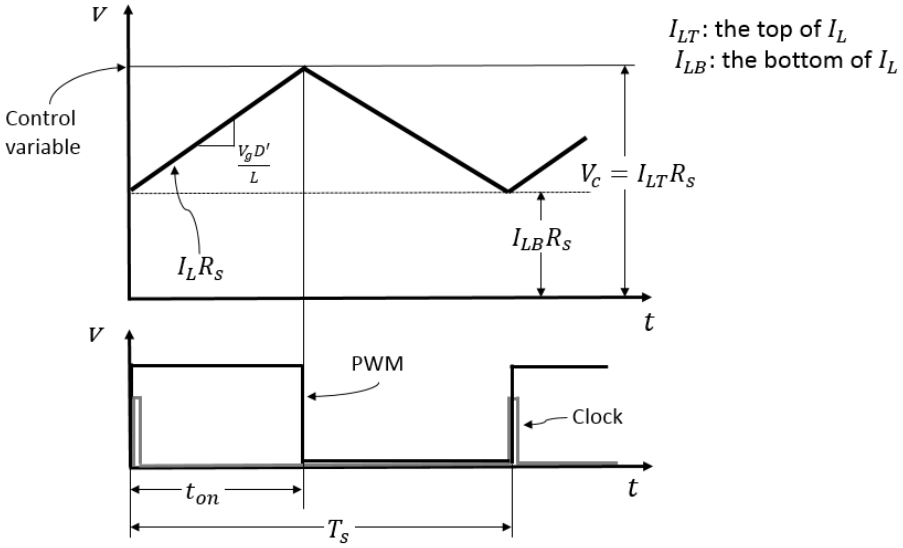


Fig. 2.29 Principle of duty cycle modulation in CMC

Fig. 2.29 illustrates the process of generating PWM signal. The triangular wave slope is proportional to the input voltage m $= V_g D'/L$, and the duty cycle is given by

$$\mathrm{D} = \frac{V_c - I_{LB} R_s}{m T_s} \tag{2.63}$$

Now, consider the system transfer function. First, in order to get inductor current, we need separate the transfer function from duty cycle to output G_{vd} into two parts. One is the transfer function from duty cycle to inductor current, denoted as G_{ld}; the other one is from inductor current to output voltage, denoted as G_{vl}. The inductor current flows through the parallel output capacitor C and load resistor R, therefore

$$G_{vl}(s) = \frac{\hat{v}(s)}{\hat{\imath}_L(s)} = \frac{R}{CRs + 1} \tag{2.64}$$

As above definition

$$G_{vl}(s) \times G_{ld}(s) = \frac{\hat{v}(s)}{\hat{\imath}_L(s)} \times \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = G_{vd}(s) \tag{2.65}$$

Therefore, the transfer function from duty cycle to inductor in buck converter can be expressed as

$$G_{ld}(s) = \frac{G_{vd}(s)}{G_{vl}(s)} = \frac{V_g}{R} \frac{CRs + 1}{LCs^2 + \frac{L}{R}s + 1} \tag{2.66}$$

Current mode control provides a special line/input feed-forward control for buck converter. It is because of the voltage conversion of buck converter equals to the duty cycle, so that the duty cycle is inversely proportional to the input voltage. At the same time, in the duty cycle modulation of current mode control as Eq. (2.63), the duty cycle also is proportional to the input voltage. Supposing that the input voltage is increased, the duty cycle of buck converter should be decreased to keep the output voltage at desired value. In VMC, we have to wait for the error amplifier to detect the error on the output, and respond by altering the control variable. However, in CMC, the triangular wave slope follows the input voltage directly. We do not need to wait until output voltage deviates the reference voltage. Including line feed-forward control, the complete system block diagram is as shown in Fig. 2.30

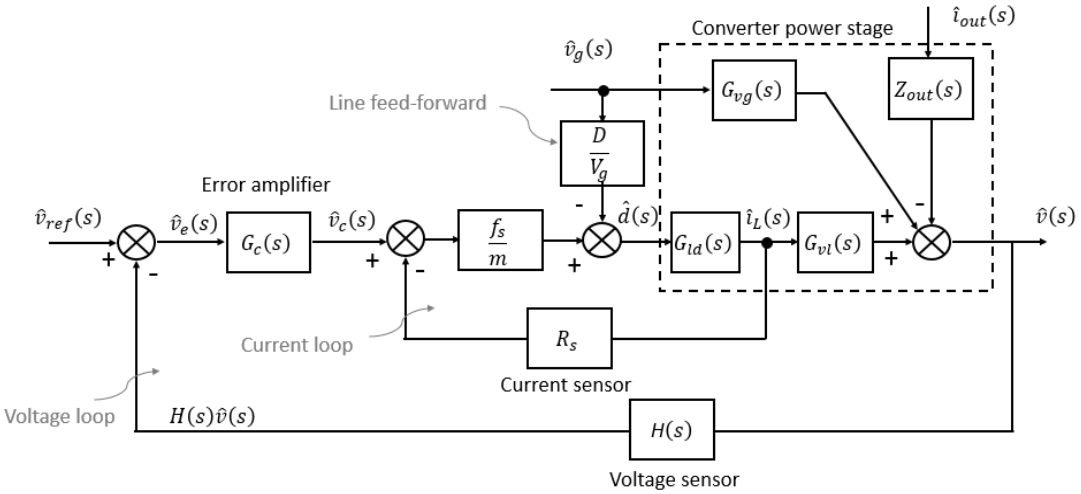


Fig. 2.30 Small-signal model of buck converter with voltage mode control

The system of buck converter with CMC consists of two feedback loops, the

inner one is current loop, and the outer loop is voltage loop. Closing the current loop as one part of the voltage loop which is given by

$$G_{iloop} = \frac{G_{ld}\frac{f_s}{m}}{1 + G_{ld}\frac{f_s}{m}R_s} \tag{2.67}$$

While, the voltage loop can be simplified as

$$G_{vloop} = \frac{1}{H}\frac{T}{1+T} \tag{2.68}$$

Where $T = HG_cG_{iloop}G_{vl}$.

Similar to VMC, the transfer functions from reference voltage to output voltage and from load current to output voltage can be expressed as

$$\hat{v}(s) = \hat{v}_{ref}(s)\frac{1}{H(s)}\frac{T(s)}{1+T(s)} \tag{2.69}$$

$$\hat{v}(s) = -\hat{\imath}_{out}(s)\frac{Z_{out}(s)}{1+T(s)} \tag{2.70}$$

The transfer function from input voltage to output voltage can be saw as the sum of two path. One is the input variation affect output through $G_{vg}(s)$ and the voltage loop, the other one is the input variation is inserted into current loop through the feed-forward path D/V_g, as shown in Fig. 2.31

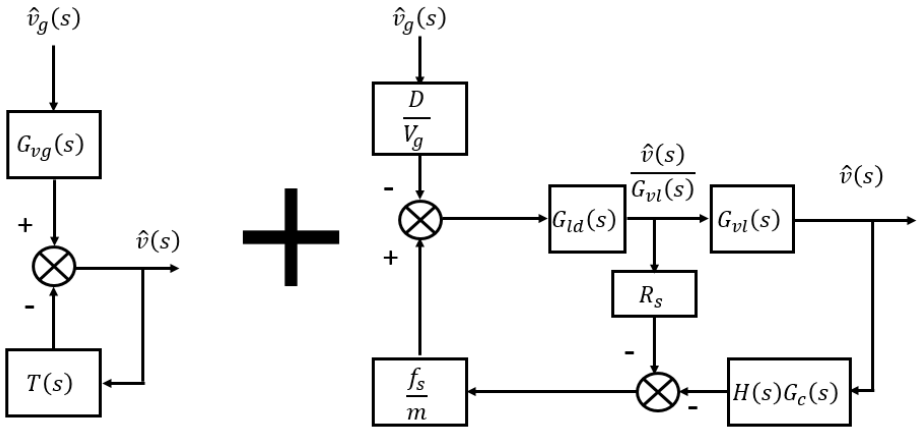


Fig. 2.31 Effect from input voltage to output voltage

From the left block diagram, we get

$$\hat{v}(s) = \hat{v}_g(s)\frac{G_{vg}(s)}{1+T(s)} \tag{2.71}$$

While the right block diagram can be expressed as

$$\hat{v}(s) = -\hat{v}_g(s)\frac{\frac{D}{V_g}G_{vd}(s)}{1+\frac{f_s}{m}\left(H(s)G_{vd}(s)G_c(s)+\frac{R_s}{G_{ld}(s)}\right)} \tag{2.72}$$

According to Eqs. (2.71) and (2.72), the whole transfer function from input voltage to output voltage can be expressed as

$$\hat{v}(s) = \hat{v}_g(s)\left(\frac{G_{vg}(s)}{1+T(s)} - \frac{\frac{D}{V_g}G_{vd}(s)}{1+\frac{f_s}{m}\left(H(s)G_{vd}(s)G_c(s)+\frac{R_s}{G_{ld}(s)}\right)}\right) \tag{2.73}$$

Although current mode control provide a natural line feed-forward control for buck converter, it is difficult to analyze the details.

2.4.2 Hysteretic control

In PWM control scheme, the basic way of a comparator works is by creating pulses signal from the intersection of two voltage signal at its input terminals---on steady voltage level (the control variable V_c), and another triangular wave voltage signal. If we apply the reference voltage directly as the steady voltage level, the system configuration should be as shown in Fig. 2.32. This control topology is called hysteretic control. It is extremely simple. A comparator with some small hysteresis between its terminals compares the output voltage directly to a high-accuracy reference voltage. As shown in Fig. 2.33, the hysteretic comparator terminates the ON-state if the triangular wave (output voltage with comparable ripple to the hysteresis window) exceeds the reference voltage by a certain amount---ΔHYS/2, and turns the switch back ON when the triangular wave falls below a certain threshold slightly lower than the reference voltage.

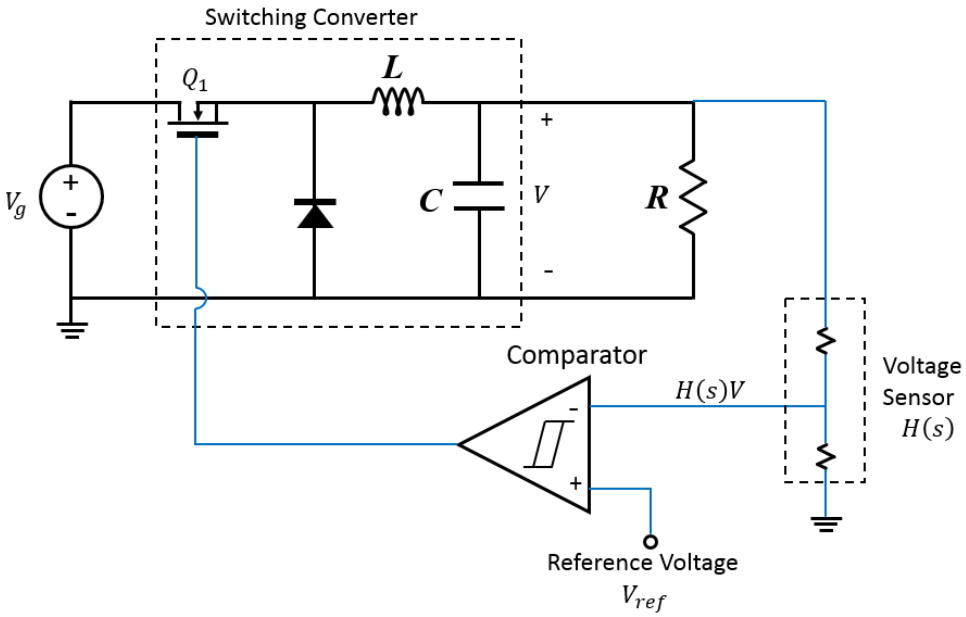


Fig. 2.32 Buck converter with hysteretic control

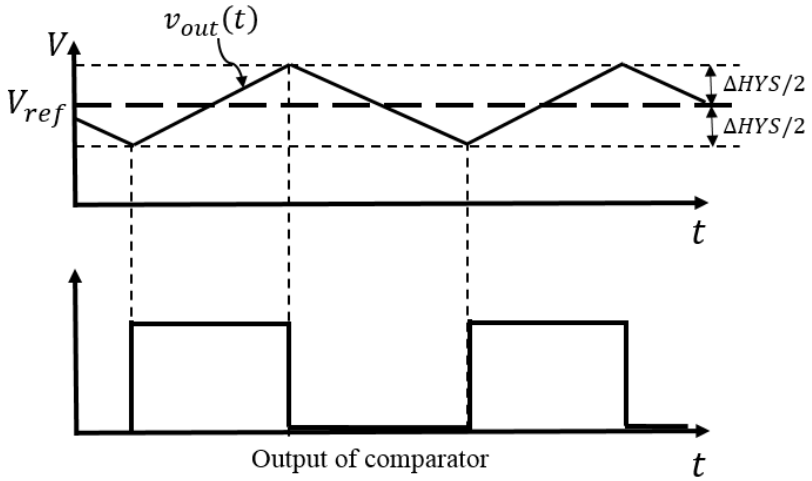


Fig. 2.33 Timing chart of hysteretic control

The advantage of hysteretic control is the speed of the control loop. When the output voltage changes due to a transient, the time it takes for the control loop is limited only by the propagation delays in the comparator and gate driver. It can react by either turning OFF completely for several pulses in succession, or by turning ON fully. Thus, the hysteretic is the fastest control topology. Additionally, its simplicity of operation makes it inherently stable without any loop

compensation. There is no feedback or compensator to design, nor poles and zeros to manipulate. In addition, without the requirement of error amplifier and oscillator, hysteretic control is very simple and low-cost topology.

However, a pure hysteretic control may not be practical for certain applications such as medical or industrial automation. The main disadvantage of hysteretic control is its switching frequency variation. There is no clock or synchronization signal setting the switching frequency. There can be a lot of erratic pulsing, usually accompanied by unacceptable audio noise, and unpredictable electromagnetic interference (EMI). Moreover, without a high-gain error amplifier, the dc set point of the output voltage may not be as precise as achieved with PWM control. Lastly, pure hysteretic control requires enhancing the output ripple. Therefore, the equivalent series resistance (ESR) in the outputs capacitor will not be too small, and even we should add typically 1Ω resistance to the output capacitor in series. The large ESR causes not only large ripple in the output voltage, but also large over-shoot and under-shoot when the load current stepwise changes. Since these disadvantages, the pure hysteretic control topology only can be accepted in some low-power, very low-cost applications due to the very low price point of such end equipment, as well as their low power, which produces low levels of EMI across the hysteretic power supply's wide switching frequency range.

In order to overcome the disadvantages of pure hysteretic control, numerous hysteretic-based control topologies are proposed recently. For example, TI's D-CAP, D-CAP2, and DCS-Control topologies **[23-25]**, they fix the ON-time to try obtaining hysteretic control with almost constant frequency. And by ripple injection, a large triangular wave signal which is proportional to the output voltage ripple is superposed on the DC level of the output voltage, then the use of low-ESR ceramic output capacitors are allowed. A "fixed on-time with bottom detection having ripple injection" control topology is introduced in reference **[26],** the system configuration is shown in Fig. 2.34. It fundamentally is a hysteretic topology, but the comparator does not require upper hysteretic threshold. Comparing the reference voltage to a triangular wave which is derived from injecting a large ripple into the detected output voltage signal. Once the triangular wave is lower than the reference signal, the switch Q_1 turns ON and maintains the ON-state for a constant time. The advantages of this topology are not only keeping the very fast transient response of hysteretic converter, but also

has the almost constant switching frequency under steady state and allows the use of low-ESR output capacitor.

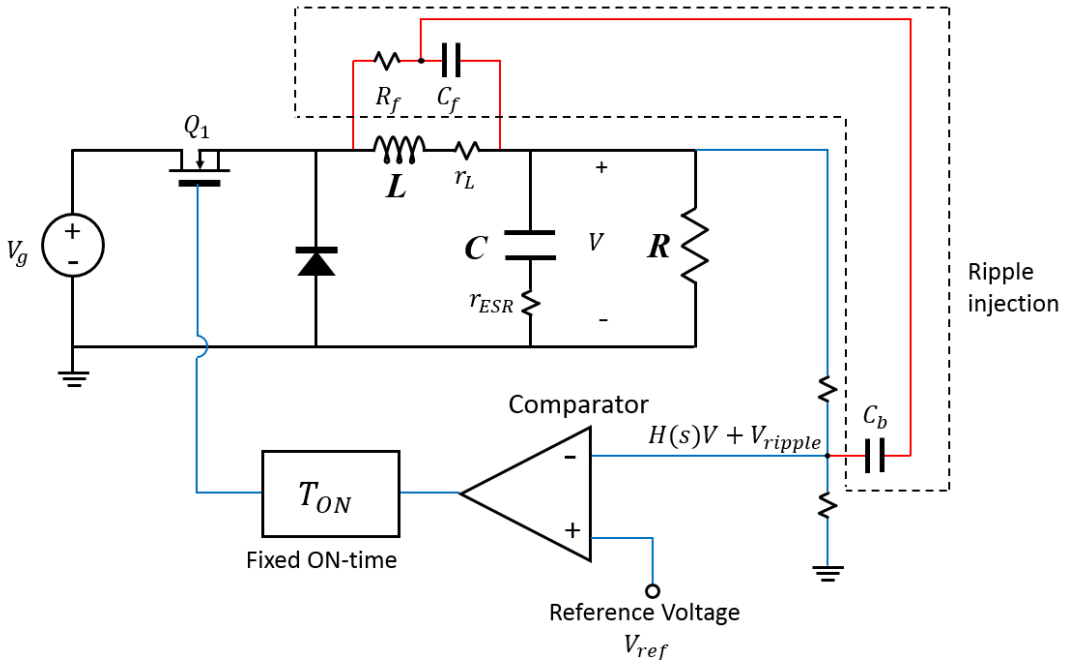


Fig. 2.34 Hysteretic control which is fixed ON-time with bottom detection having ripple injection

CHAPTER Ⅲ
DYNAMIC PERFORMANCE

As mentioned in the previous chapter, there are three most common disturbance sources in switching power supply system. They are reference signal variation $\hat{v}_{ref}$, input voltage variation $\hat{v}_g$ and load current variation $\hat{\imath}_{out}$. Normally, the reference variation is caused by temperature change around the circuit. The developed band-gap reference technology can achieve temperature dependence less than 50ppm/℃. However, some applications require the output voltage with several different values. In this case, we hope that the output voltage can track the reference signal rapidly with tolerable over-shoot. The input voltage variation normally means the residual AC component that is not removed by a low-pass filter. It is nearly always required that a filter be added at the power input of a switching converter to protect the converter and its load from transients that caused by the input variation. While, for buck converter, the line/input feed-forward control scheme also is an effective method. The load current variation breaks the charge balance of output capacitor, and the output voltage deviates from the reference signal until the capacitor reaches new balance. The dynamic performances reveal the output regulation capability of the switching converter when it encounters transients that appear in the reference signal, the input voltage and the load current.

This chapter analyzes the relation between the dynamic performance and the frequency characteristics. In order to improve the dynamic performance and guarantee the stability, phase compensation is designed. The design procedure for buck converter with VMC and CMC both will be demonstrated. Finally, the constraints and challenges in real world are introduced.

3.1 DYNAMIC PERFORMANCE AND FREQUENCY CHARACTERISTICS

We have shown how to derive the small-signal ac transfer function of a switching converter, and the system with feedback loop is described in last chapter. Therefore, the output voltage variation of a buck converter with VMC yields

$$\hat{v} = \hat{v}_{ref}\frac{1}{H}\frac{T}{1+T} + \hat{v}_g\frac{G_{vg}}{1+T} - \hat{\imath}_{out}\frac{Z_{out}}{1+T} \tag{3.1}$$

With

$$T(s) = H(s)G_c(s)G_{vd}(s)/V_p \tag{3.2}$$

$T(s)$ is named as "loop gain", but it's worth noting that the "loop" is not closed. When we close this feedback loop, the closed loop as a whole should be considered as one part of the transfer function from the variation to the output voltage.

3.1.1 Closing the feedback loop

A buck converter is a 2nd order system, and the power stage transfer functions are given by

$$G_{vd}(s) = \frac{V_g}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0\omega_0} + 1} \tag{3.3a}$$

$$G_{vg}(s) = \frac{D}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0\omega_0} + 1} \tag{3.3b}$$

$$Z_{out}(s) = \frac{Ls}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0\omega_0} + 1} \tag{3.3c}$$

Where $\omega_0 = \frac{1}{\sqrt{LC}}$, $Q_0 = R\sqrt{\frac{C}{L}}$.

Now only let us consider the simplest control scheme what is without phase compensation and the error amplifier only provides a dc gain---$G_c(s) = K$. The loop gain $T(s)$ can be written

$$T(s) = T_0 \frac{1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0\omega_0} + 1} \tag{3.4}$$

Where the dc gain is

$$T_0 = \frac{HV_gG_{c0}}{V_p} = \frac{HKV_g}{V_p} \tag{3.5}$$

Magnitude of the loop gain $T(s)$ is sketched in Fig. 3.1.

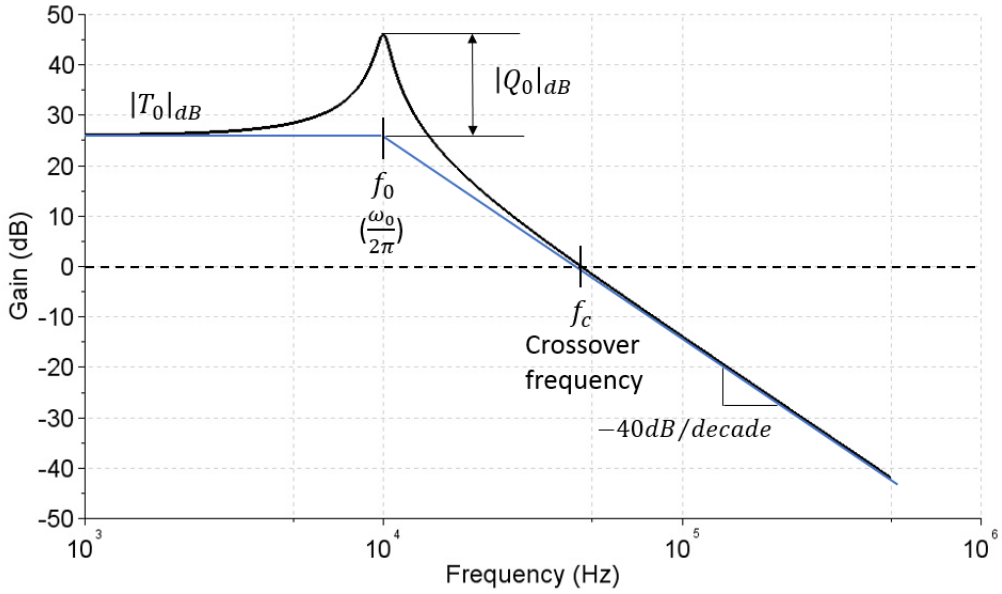


Fig. 3.1 Magnitude of the loop gain $T(s)$

The magnitude of the loop gain $\|T\|$ equals to one at frequency f_c. At frequencies lower then f_c, $\|T\| > 1$, while at frequencies higher than f_c, $\|T\| < 1$. Therefore, f_c is called as a crossover frequency.

Closing this loop gain, let us investigate how to plot $\|T/(1+T)\|$ and $\|1/(1+T)\|$. Since $\|T\| \gg 1$ for $f \ll f_c$, hence, at low frequency, $(1+T) \approx T$, $\|T/(1+T)\| \approx 1$ and $\|1/(1+T)\| \approx \|1/T\|$. Conversely, $\|T\| \ll 1$ for $f \gg f_c$.

So at high frequency, $(1+T)\approx 1$, $\|T/(1+T)\|\approx\|T\|$ and $\|1/(1+T)\|\approx 1$. They can be summarized as

$$\frac{T}{1+T}=\begin{cases}1 & for\ \|T\|\gg 1\\ T & for\ \|T\|\ll 1\end{cases} \tag{3.6a}$$

$$\frac{1}{1+T}=\begin{cases}\frac{1}{T} & for\ \|T\|\gg 1\\ 1 & for\ \|T\|\ll 1\end{cases} \tag{3.6b}$$

T and $T/(1+T)$ are plotted in Fig. 3.2

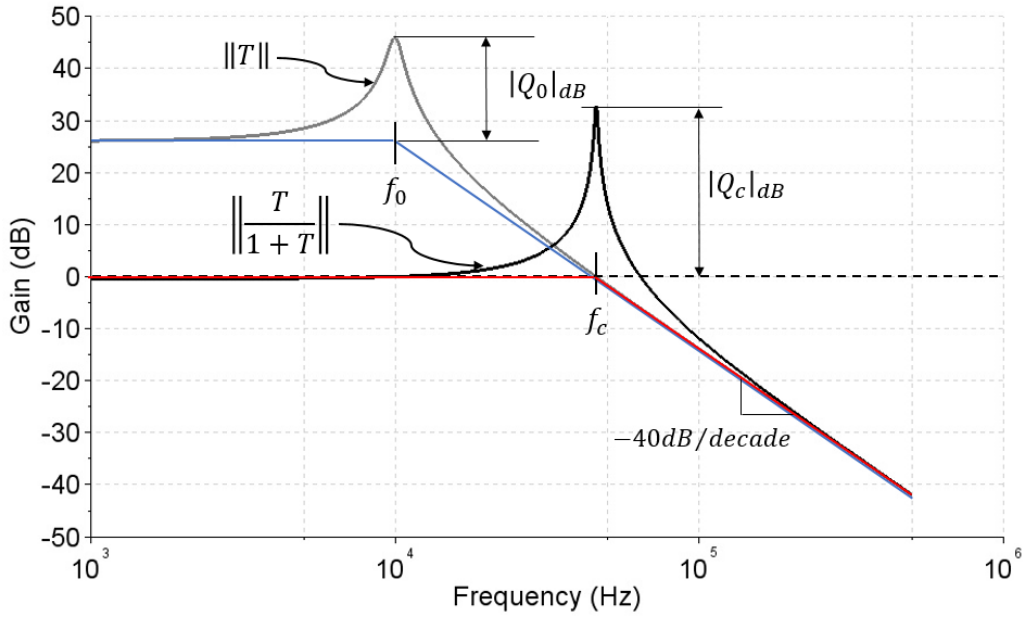


Fig. 3.2 Magnitude of $\|T\|$ and $\|T/(1+T)\|$

The closed-loop can be seen as a new 2nd order system with new resonant frequency ω_c and new damping factor Q_c. It can be written as

$$\frac{T(s)}{1+T(s)}=\frac{1}{\left(\frac{s}{\omega_c}\right)^2+\frac{s}{Q_c\omega_c}+1+\frac{1}{T_0}}\approx\frac{1}{\left(\frac{s}{\omega_c}\right)^2+\frac{s}{Q_c\omega_c}+1}\quad \text{for } T_0\gg 1 \tag{3.7}$$

Then consider what will happen to $1/(1+T)$, T and $1/(1+T)$ are plotted in Fig. 3.3

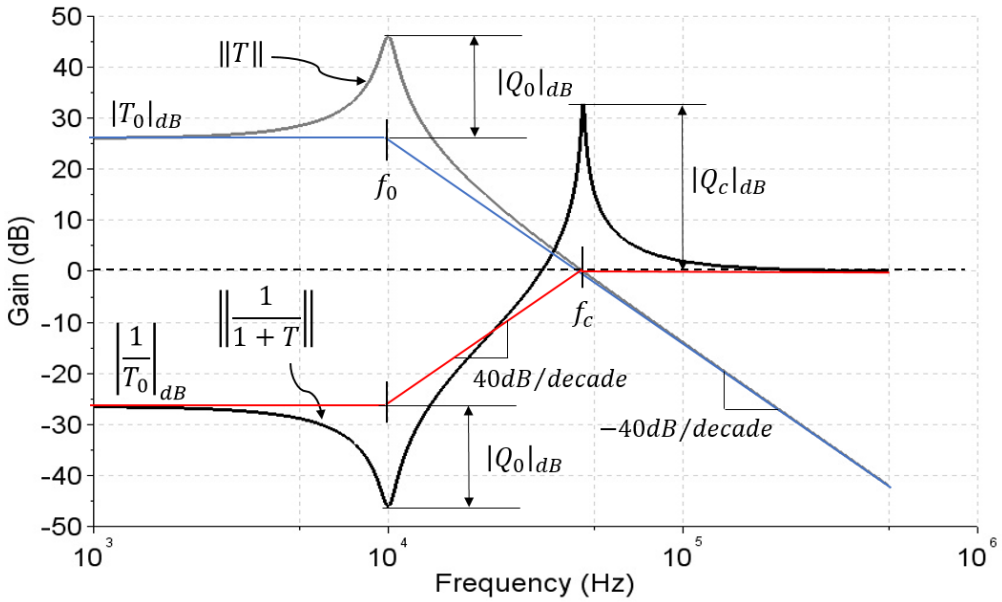


Fig. 3.3 Magnitude of $\|T\|$ and $\|1/(1+T)\|$

According to Fig. 3.3, $1/(1+T)$ can be expressed as

$$\frac{1}{1+T(s)} \approx \frac{1}{T_0}\frac{\left(\frac{s}{\omega_0}\right)^2+\frac{s}{Q_0\omega_0}+1}{\left(\frac{s}{\omega_c}\right)^2+\frac{s}{Q_c\omega_c}+1} \qquad \text{for } T_0 \gg 1 \tag{3.8}$$

Using the algebra-on-the graph method [27], the relation of ω_0 and ω_c is given by

$$\left(\frac{\omega_c}{\omega_0}\right)^2 = T_0 \qquad \text{for } T_0 \gg 1 \tag{3.9}$$

Therefore, the two damping factors Q_0 and Q_c have realtion

$$Q_c = \sqrt{T_0}Q_0 = \frac{\omega_c}{\omega_0}Q_0 \tag{3.10}$$

In the buck converter, $Q_0 = R\sqrt{C/L}$, it is a constant value, unless the load is changed. Although we cannot change the value of Q_0, the dc gain T_0 is adjustable. The results of $\|T/(1+T)\|$ are plotted in Fig. 3.4 with the condition of $T_0 \gg 1$, the peak value of $\|T\|$ at ω_0 and the peak value of $\|T/(1+T)\|$ at ω_c are given by

$$Peak_{\|T\|} = |T_0|_{dB} + |Q_0|_{dB} \qquad @\ \omega_0 \tag{3.11a}$$

$$Peak_{\|T/(1+T)\|} = \frac{1}{2}|T_0|_{dB} + |Q_0|_{dB} \qquad @\ \omega_c \tag{3.11b}$$

Therefore, between $Peak_{\|T\|}$ and $Peak_{\|T/(1+T)\|}$, we can get a line with the slope $-20dB/decade$

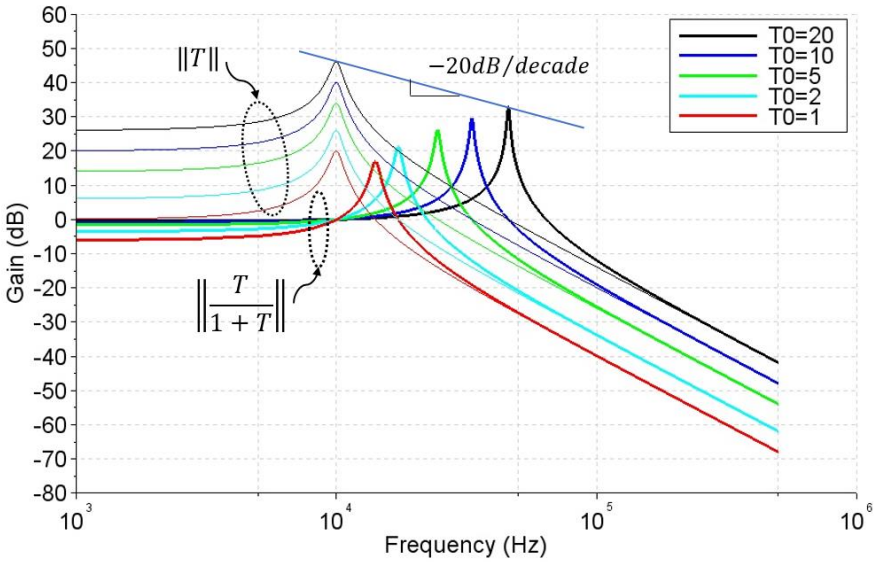


Fig. 3.4 Q_c for various values of T_0

3.1.2 Time-domain response

The system characteristic in frequency-domain determines the transient response in time-domain. Now let us investigate the relations between transient responses and frequency characteristics. This will improve our insight about the switching converter, and direct the system design for getting good dynamic performance.

All of the variation in V_{ref}, V_g and I_{out} are supposed as a unit-step change. The closed feedback loop combines with the rest parts to constitute new transfer function from the variation to the output voltage. For example, the transfer function from the input voltage variation $\hat{v}_g$ to the output voltage variation $\hat{v}$ with closed-loop becomes as

$$G_{vg\_c} = \frac{G_{vg}}{1+T} \tag{3.12}$$

The unit-step response can be derived from inserting the variation into the system. However, if we do that in time-domain, it always means a solution of higher order differential equation. It is complicated and fallible during the solution process. In order to simplify it, the conventional method transforms everything into frequency domain by Laplace transformation. The frequency-domain expression of the output voltage can be easily obtained after some algebraic operations. Nevertheless, what we concern is the responses in time-domain, so eventually, inverse Laplace transformation is utilized to map the responses from frequency-domain back into the time-domain, as shown in Fig. 3.5.

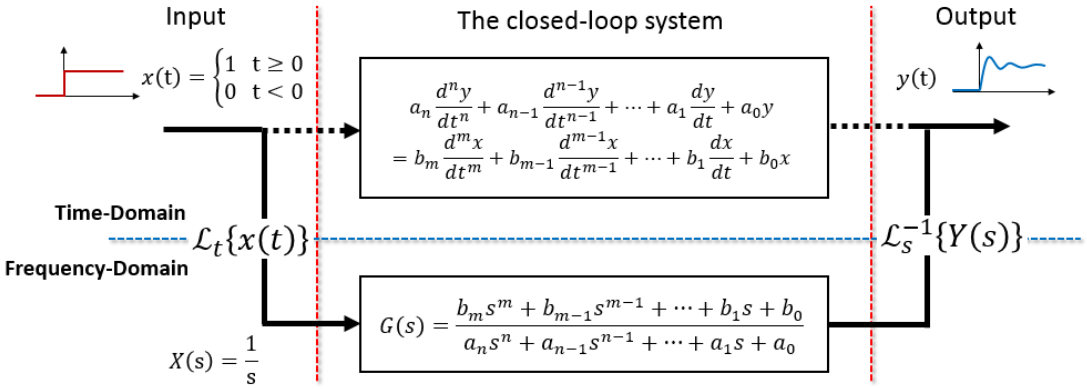


Fig. 3.5 Utilize frequency-domain to map the responses in time-domain

3.1.2.1 Reference transient response

First, let us investigate the transient response, which is caused by reference signal. The closed-loop transfer function from the reference signal variation to the output variation is given by

$$G_{vr\_c}(s) = \frac{1}{H(s)} \frac{T(s)}{1+T(s)} = \frac{1}{H(s)} \frac{1}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c \omega_c} + 1} \tag{3.13}$$

Supposing $H(s) = 1$, then its gain should as shown in Fig. 3.2. When the

reference variation is unit-step change, the frequency-domain expression of this variation is

$$V_{ref}(s) = \frac{1}{s} \tag{3.14}$$

Therefore, the output variation in frequency-domain can be written as

$$\mathrm{V}(s) = G_{vr\_c}(s) \times V_{ref}(s) = \frac{{\omega_c}^2}{\mathrm{s}^2 + \frac{\omega_c}{Q_c}\mathrm{s} + {\omega_c}^2} \times \frac{1}{s} \tag{3.15}$$

The characteristic equation of $G_{vr\_c}(s)$ is

$$\mathrm{s}^2 + \frac{\omega_c}{Q_c}\mathrm{s} + {\omega_c}^2 = 0 \tag{3.16}$$

This has the roots $s_{1,2} = -\frac{\omega_c}{2Q_c} \pm \omega_c\sqrt{\left(\frac{1}{2Q_c}\right)^2 - 1}$. According to different value of Q_c, the roots have different form. Therefore, the unit-step response in the output voltage also has different form. There are four forms

(a) $Q_c = \infty$, a pair of conjugate imaginary roots: $s_{1,2} = \pm j\omega_c$

$$\mathrm{V}(s) = \frac{{\omega_c}^2}{s(s^2 + {\omega_c}^2)} = \frac{1}{s} - \frac{s}{s^2 + {\omega_c}^2} \tag{3.17a}$$

$$\hat{v}(t) = \mathcal{L}_s^{-1}\{\mathrm{V}(s)\} = 1 - \cos\omega_c\,\mathrm{t} \tag{3.17b}$$

The output voltage oscillates at frequency ω_c. We can say this system is undamped

(b) $Q_c > 0.5$, a pair of conjugate complex roots with negative real part: $s_{1,2} = -\frac{\omega_c}{2Q_c} \pm j\omega_c\sqrt{1 - \left(\frac{1}{2Q_c}\right)^2}$

$$\mathrm{V}(s) = \frac{1}{s} - \frac{s+\frac{\omega_c}{2Q_c}}{\left(s+\frac{\omega_c}{2Q_c}\right)^2 + \left(\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\omega_c\right)^2} - \frac{\frac{\omega_c}{2Q_c}}{\left(s+\frac{\omega_c}{2Q_c}\right)^2 + \left(\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\omega_c\right)^2} \tag{3.18a}$$

$$\hat{v}(t) = 1 - \frac{e^{-\frac{\omega_c}{2Q_c}t}}{\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}}\sin\left(\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\,\omega_c t + \tan^{-1}\left(2Q_c\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\right)\right) \tag{3.18b}$$

The output voltage has an amplitude gradually decreased oscillation component at frequency $\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\,\omega_c$. This status is called underdamp.

(c) $Q_c = 0.5$, two equal real roots: $s_{1,2} = -\omega_c$

$$\mathrm{V}(s) = \frac{{\omega_c}^2}{s(s+\omega_c)^2} = \frac{1}{s} - \frac{1}{s+\omega_c} - \frac{\omega_c}{(s+\omega_c)^2} \tag{3.19a}$$

$$\hat{v}(t) = 1 - \mathrm{e}^{-\omega_c \mathrm{t}}\,(1+\omega_c \mathrm{t}) \tag{3.19b}$$

The output voltage tracks the reference signal and returns to equilibrium as quickly as possible without oscillation. This status is called critically damped.

(d) $0 < Q_c < 0.5$, two unequal real roots: $s_{1,2} = -\frac{\omega_c}{2Q_c} \pm \omega_c\sqrt{\left(\frac{1}{2Q_c}\right)^2 - 1}$

$$\mathrm{V}(s) = \frac{s_1 s_2}{s(s-s_1)(s-s_2)} = \frac{1}{s} - \frac{s_2}{s_2-s_1}\frac{1}{s-s_1} - \frac{s_1}{s_1-s_2}\frac{1}{s-s_2} \tag{3.20a}$$

$$\hat{v}(t) = 1 - \frac{s_2}{s_2-s_1}\mathrm{e}^{s_1 \mathrm{t}} - \frac{s_1}{s_1-s_2}\mathrm{e}^{s_2 \mathrm{t}} \tag{3.20b}$$

The output voltage returns to equilibrium without oscillation, however, the deviation between the output voltage and the reference signal exponentially decays with two different time constants. This status is called overdamped.

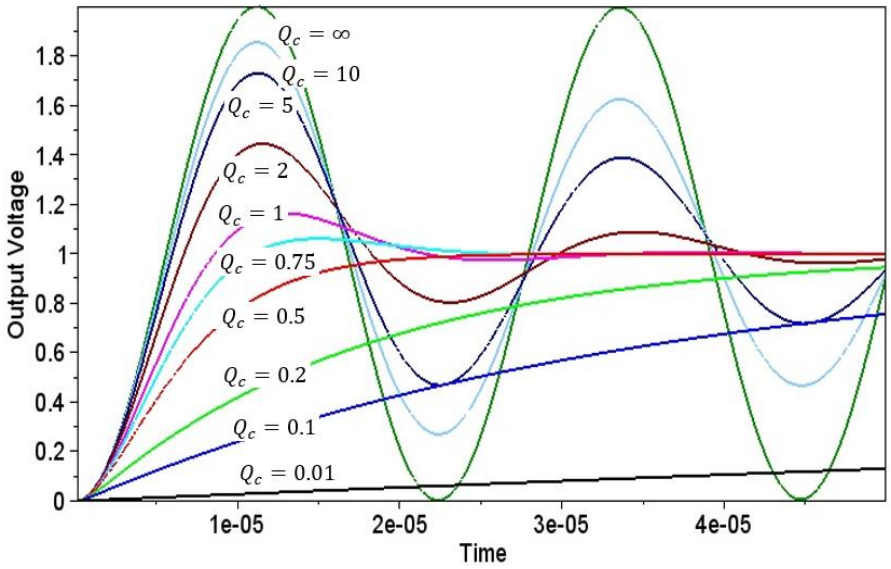


Fig. 3.6 Unit-step response of $G_{vr\_c}(s)$ with various values of Q_c

The unit-step responses of the second-order system $G_{vr\_c}(s)$ with various values of Q_c are plotted in Fig. 3.6. Obviously, the undamped system is undesired due to the continuous oscillation. However, the overdamped system without oscillation also is not a good choice, because the response is too slow to track the variation in reference signal. Therefore, we always hope that the system can be operated under critically damped or underdamped status. From Eq. (3.19b) we can see that the unit-step response of critically damped system has only one exponentially decay term. A large ω_c provides a fast response, but the condition $Q_c = 0.5$ is so rigorous that we cannot ensure our design just get this value and always keep it. Therefore, compared with critically damped, the discussion of underdamped system should be more significant.

The unit-response of underdamped system is given in Eq. (3.18b), and the decay term consists of a sinusoidal function multiplied by an exponentially decayed amplitude. Eq. (3.18b) is rewritten as

$$\hat{v}(t) = 1 - \mathrm{A}(t)\sin(\omega_d t + \varphi) \tag{3.21}$$

where $\omega_d = \sqrt{1-(1/2Q_c)^2}\omega_c$, $\varphi = \tan^{-1}\left(2Q_c\sqrt{1-(1/2Q_c)^2}\right)$, and the amplitude of the sinusoidal function is a time-function

$$\mathrm{A}(t) = \frac{e^{-\frac{\omega_c}{2Q_c}t}}{\sqrt{1-(1/2Q_c)^2}} \tag{3.22}$$

At $t = 0$, we have

$$\mathrm{A}(0) = \frac{1}{\sqrt{1-(1/2Q_c)^2}} \tag{3.23}$$

With a small Q_c, the initial value of amplitude also is small. It is beneficial to decrease the overshot voltage. At the same time, the exponential term $e^{-\frac{\omega_c}{2Q_c}t}$ can decay at fast speed. While, except for a small Q_c, a large ω_c also provides fast decay.

Summering the design principles for reference transient response in a buck converter: a small Q_c (but larger than 0.5) and a large resonant frequency ω_c can make the output rapidly track the reference signal, and the response has small overshot and short response time.

3.1.2.2 Line transient response

The closed-loop transfer function from the input voltage to the output voltage is given by

$$G_{vg\_c}(s) = G_{vg}(s)\frac{1}{1+T(s)} = \frac{D}{T_0}\frac{1}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c\omega_c} + 1} \tag{3.24}$$

The gain of $G_{vg\_c}(s)$ is plotted in Fig. 3.7.

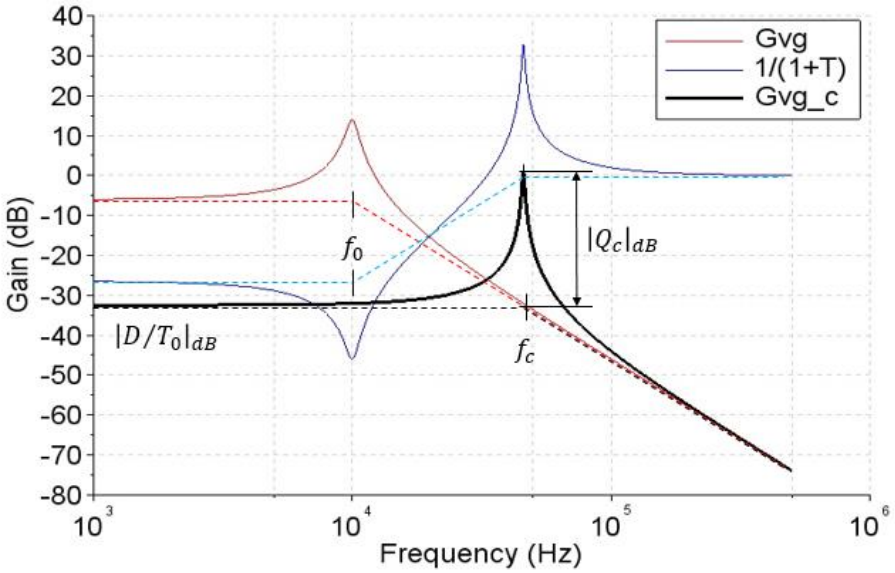


Fig. 3.7 Magnitude of the closed loop transfer function $G_{vg\_c}(s)$

In frequency-domain, the unit-step response of the voltage that is caused by the input voltage can be expressed as

$$\mathrm{V}(s) = G_{vg\_c}(s) \times V_g(s) = \frac{D}{T_0 s}\frac{1}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c\omega_c} + 1} \tag{3.25}$$

It is very similar to the unit-step response caused by the reference signal, except for the additional coefficient---D/T_0. The response in time-domain also can be classified into four forms for various values of Q_c, and the expression only need make every term to be multiplied by D/T_0. For example, when Q_c is larger than 0.5, the system is underdamped, and the unit-step response can be

expressed as

$$\hat{v}(t) = \frac{\boldsymbol{D}}{\boldsymbol{T_0}} - \frac{e^{-\frac{\omega_c}{2Q_c}t}}{\frac{\boldsymbol{T_0}}{\boldsymbol{D}}\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}} \sin\left(\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\,\omega_c t + \tan^{-1}\left(2Q_c\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\right)\right) \quad (3.26)$$

The unit-step responses of $G_{vg\_c}(s)$ are plotted in Fig. 3.8.

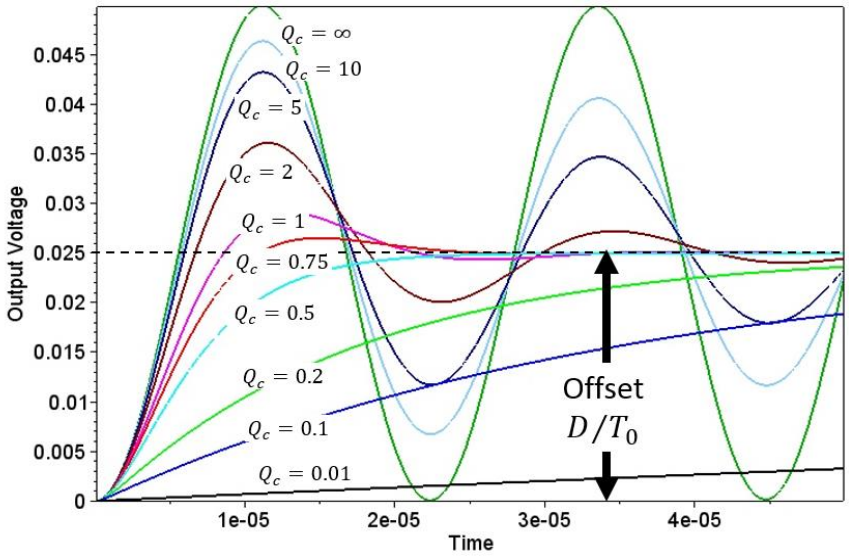


Fig. 3.8 Unit-step response of $G_{vg\_c}(s)$ with various values of Q_c

In reference transient response, the output voltage is desired to follow the changed reference signal. From the unit-step response of $G_{vr\_c}(s)$, we can see that except for the undamped system, the difference between the reference signal and the output voltage always can be decayed to zero regardless of how long the system returns to equilibrium. However, in line transient response, even if the system has returned to equilibrium, there still has an offset in the output voltage, and the magnitude of this offset equals to D/T_0. This offset is undesired. Hence, in order to get a good line transient response, not only we need a small Q_c and a large ω_c for small overshot and rapid response, but also need a large dc gain T_0 to reduce the offset and further decrease the overshot.

3.1.2.3 Load transient response

Load transient response is very special, and it is very difficult to analyze because that the load current change also means that the output resistor is changed. Therefore, the transfer function from the load current to the output

voltage ($Z_{out}(s)$) actually is time-varying. Even if we can ignore the variation in the output resistor R by utilizing the small-signal approximation principle, there is still a problem what need not consider in the reference transient response and the line transient response. This problem is caused by those power-loss elements (R_L, DR_{on} and $D'R_D$). Although they are very small and are always neglected during analysis process, they can affect the low-frequency characteristics of the output impedance Z_{out}.

For simplicity, first, we still ignore the effect of power-loss resistors. Then the closed-loop transfer function Z_{out_c} can be expressed as

$$Z_{out\_c}(s) = Z_{out}(s)\frac{1}{1+T(s)} = \frac{1}{T_0}\frac{Ls}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c\omega_c} + 1} \tag{3.27}$$

Setting $L = 1\mu H$, the gain of $Z_{out\_c}(s)$ is plotted in Fig. 3.9.

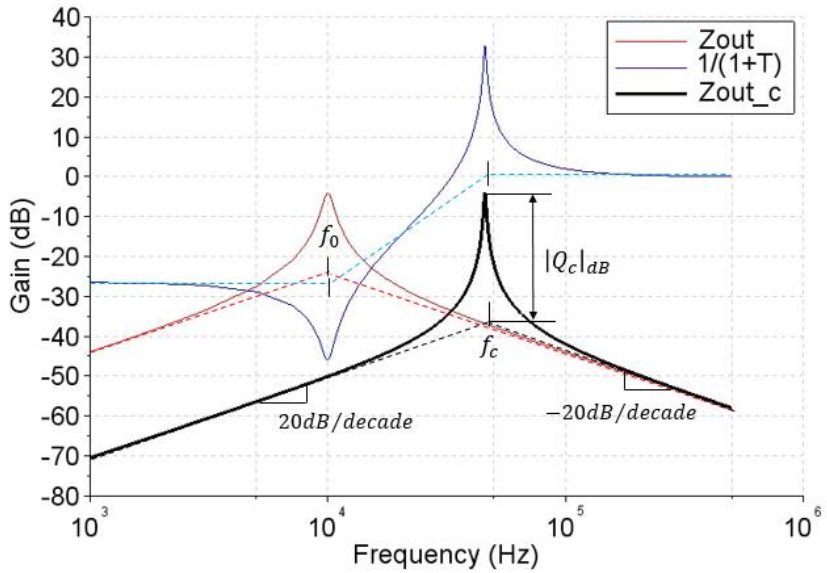


Fig. 3.9 Magnitude of the closed loop transfer function $Z_{out\_c}(s)$, ignoring the power-loss elements

In frequency-domain, the unit-step response that is caused by the input voltage can be expressed as

$$\mathrm{V}(s) = -Z_{out\_c}(s) \times I_{out}(s) = -\frac{L}{T_0}\frac{1}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c\omega_c} + 1} \tag{3.28}$$

According to different value of Q_c, the unit-step response of $Z_{out\_c}(s)$ are

(a) $Q_c = \infty$

$$\mathrm{V}(s) = -Z_{out\_c}(s) \times I_{out}(s) = -\frac{L}{T_0}\frac{{\omega_c}^2}{\mathrm{s}^2 + {\omega_c}^2} \tag{3.29a}$$

$$\hat{v}(t) = -\frac{L\omega_c}{T_0} \cdot \sin \omega_c t \tag{3.29b}$$

(b) $Q_c > 0.5$

$$\mathrm{V}(s) = -\frac{L}{T_0}\frac{\omega_c}{\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}}\frac{\omega_c\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}}{\left(s+\frac{\omega_c}{2Q_c}\right)^2+\left(\omega_c\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\right)^2} \tag{3.30a}$$

$$\hat{v}(t) = -\frac{L\omega_c}{T_0\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}} \cdot \mathrm{e}^{-\frac{\omega_c}{2Q_c}\mathrm{t}} \cdot \sin \omega_c\sqrt{1-\left(\frac{1}{2Q_c}\right)^2}\, t \tag{3.30b}$$

(c) $Q_c = 0.5$

$$\mathrm{V}(s) = -Z_{out\_c}(s) \times I_{out}(s) = -\frac{L}{T_0}\frac{{\omega_c}^2}{(s+\omega_c)^2} \tag{3.31a}$$

$$\hat{v}(t) = -\frac{L{\omega_c}^2}{T_0} \cdot \mathrm{e}^{-\omega_c \mathrm{t}} \cdot t \tag{3.31b}$$

(d) $0 < Q_c < 0.5$

$$\mathrm{V}(s) = -Z_{out\_c}(s) \times I_{out}(s) = -\frac{L}{T_0}\frac{{\omega_c}^2}{(s-s_1)(s-s_2)} \tag{3.32a}$$

$$\hat{v}(t) = -\frac{L\omega_c}{2T_0\sqrt{(1/2Q_c)^2-1}} \cdot (e^{s_1 t} - e^{s_2 t}) \tag{3.32b}$$

Where $s_1 = -\omega_c\left(1/2Q_c - \sqrt{(1/2Q_c)^2-1}\right), s_2 = -\omega_c\left(1/2Q_c + \sqrt{(1/2Q_c)^2-1}\right)$

The results of unit-step response are plotted in Fig. 3.10 respectively.

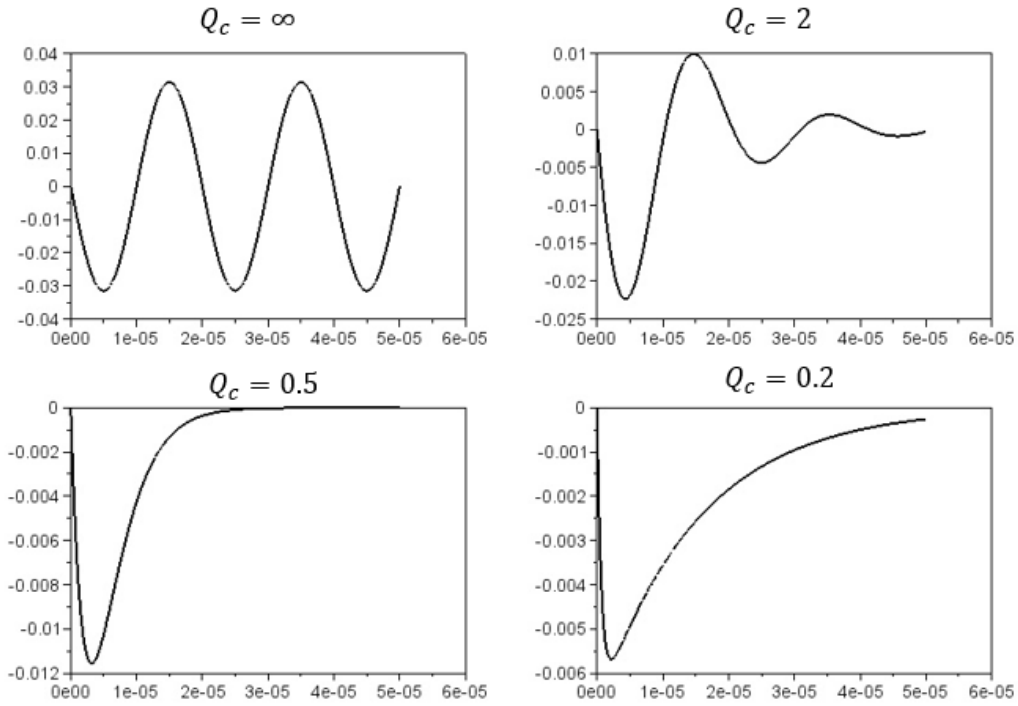


Fig. 3.10 Unit-step response of $Z_{out\_c}(s)$ with various values of Q_c

Above analysis is based on ignoring the power-loss elements. However, if the power-loss elements are considered, an actual description of the output impedance Z_{out} should be as shown in Fig. 3.11

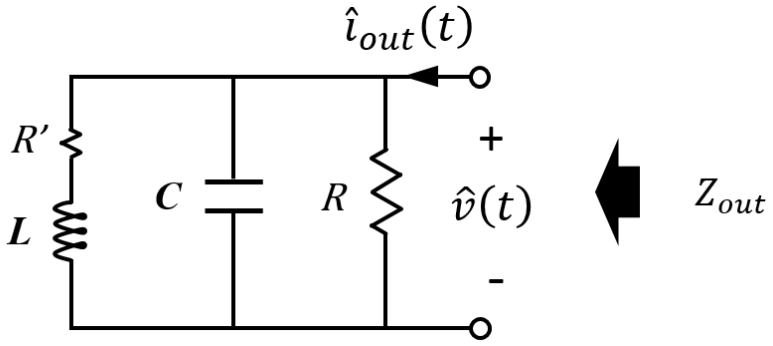


Fig. 3.11 Output impedances with power-loss elements

Where $R' = R_L + DR_{on} + D'R_D$. $Z_{out}(s)$ is rewritten

$$Z_{out}(s) = \frac{RR'\left(\frac{L}{R'}s + 1\right)}{(R + R')\left(\frac{LCR}{R + R'}s^2 + \frac{L + CRR'}{R + R'}s + 1\right)} \tag{3.33}$$

If $R' \ll R$, Eq. (3.33) can be approximated and simplified as

$$Z_{out}(s) \approx \frac{R'\left(\frac{s}{\omega_z} + 1\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0'\omega_0} + 1} \tag{3.34}$$

Where $\omega_z = R'/L,\ \omega_0 = 1/\sqrt{LC},\ Q_0' = R\sqrt{LC}/(L + CRR')$.

Notice that $Q_0' < R\sqrt{C/L}$, so that if power-loss elements are considered, the damping factor will smaller than Q_0.

The new closed-loop transfer function $Z_{out\_c}(s)$ that includes the power-loss elements is also rewritten as Eq. (3.35), and the gain is plotted in Fig. 3.12.

$$Z_{out\_c}(s) = Z_{out}(s)\frac{1}{1 + T(s)} = \frac{R'}{T_0}\frac{\left(\frac{s}{\omega_z} + 1\right)}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c'\omega_c} + 1} \tag{3.35}$$

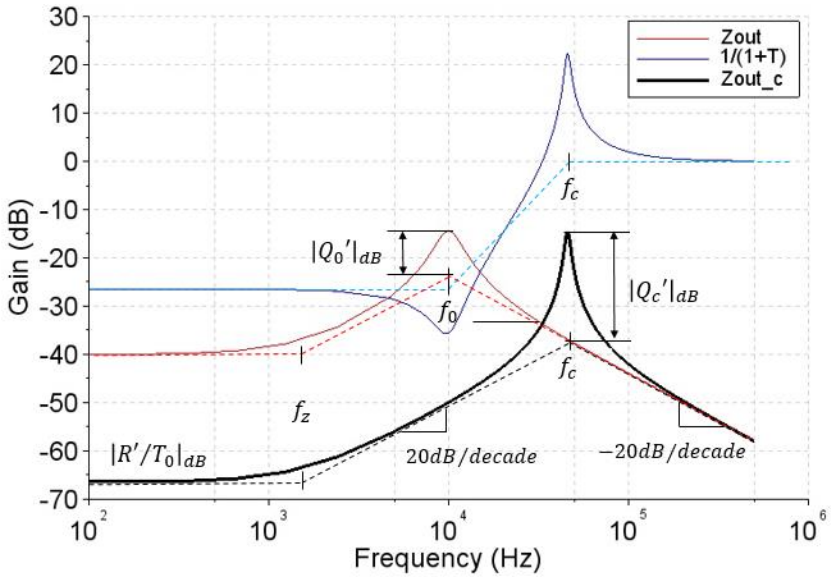


Fig. 3.12 Magnitude of the closed loop transfer function $Z_{out\_c}(s)$, including the power-loss elements

The frequency-domain expression of unit-step response is given by

$$\mathrm{V}(s) = -Z_{out_c}(s) \times I_{out}(s) = -\frac{R'}{T_0 s}\frac{\left(\frac{s}{\omega_z}+1\right)}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c{}'\omega_c}+1} \tag{3.36}$$

Eq. (3.36) can be separated into two parts as

$$\mathrm{V}(s) = -\frac{L}{T_0}\frac{1}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c{}'\omega_c}+1} - \frac{R'}{T_0 s}\frac{1}{\left(\frac{s}{\omega_c}\right)^2 + \frac{s}{Q_c{}'\omega_c}+1} \tag{3.37}$$

The first term on the right-hand side just is the expression in Eq. (3.28), but with a new damping factor $Q_c{}'$. The second term is similar to line unit-step response in Eq. (3.25), just replace the coefficient D/T_0 by R'/T_0 and replace Q_c by $Q_c{}'$.

According to the previous analysis, it is easy to deduce the time-domain expression of Eq. (3.37). The underdamped form is analyzed as an example. If $Q_c{}' > 0.5$

$$\hat{v}(t) = -\frac{R'}{T_0} + \mathrm{A}(t) \cdot (R' \cdot \sin(\omega_d t + \varphi) - L\omega_c \sin\omega_d t) \tag{3.38}$$

Where $\omega_d = \sqrt{1-(1/2Q_c{}')^2}\omega_c$, $\varphi = \tan^{-1}\left(2Q_c{}'\sqrt{1-(1/2Q_c{}')^2}\right)$, and the exponentially decayed amplitude $\mathrm{A}(t)$ is given by

$$A(t) = \frac{\mathrm{e}^{-\omega_c/2Q_c{}'\mathrm{t}}}{T_0\sqrt{1-(1/2Q_c{}')^2}} \tag{3.39}$$

Eq. (3.38) consists of three components: a constant term and two amplitude decayed sine terms. The two sine terms have the same frequency---ω_d and a phase difference---φ. This unit-step response is plotted in Fig. 3.13.

Unlike the reference transient response and the line transient response, in load transient response, the amplitude of decay terms is proportional to the frequency ω_c or ${\omega_c}^2$. As shown in Fig. 3.13, the decayed term--- $L\omega_c \mathrm{A}(t)\sin\omega_d t$ is dominant during the response process since the system is set as $L\omega_c \gg R'$. It seems a contradiction that we desire a large ω_c for the pursuit of rapid decay, but at the same time, the larger amplitude will causes larger overshoot. However, reviewing the Eq. (3.9), we can find the relation between ω_c and T_0. Since the resonant frequency ω_0 is decided by the output capacitor and the indicator, a

higher crossover frequency is realized by increasing the dc gain T_0. Again, consider the amplitude of $L\omega_c \mathrm{A}(t)\sin\omega_d t$ and replace ω_c by $\sqrt{T_0}\omega_0$

$$L\omega_c \mathrm{A}(t) = \frac{L\omega_0}{\sqrt{T_0}\cdot\sqrt{1-(1/2Q_c{}')^2}}\,\mathrm{e}^{-\omega_c/2Q_c{}'\mathrm{t}} \tag{3.40}$$

Hence, pursuing a larger ω_c will not cause bigger overshoot voltage, even it can suppress the overshoot phenomenon.

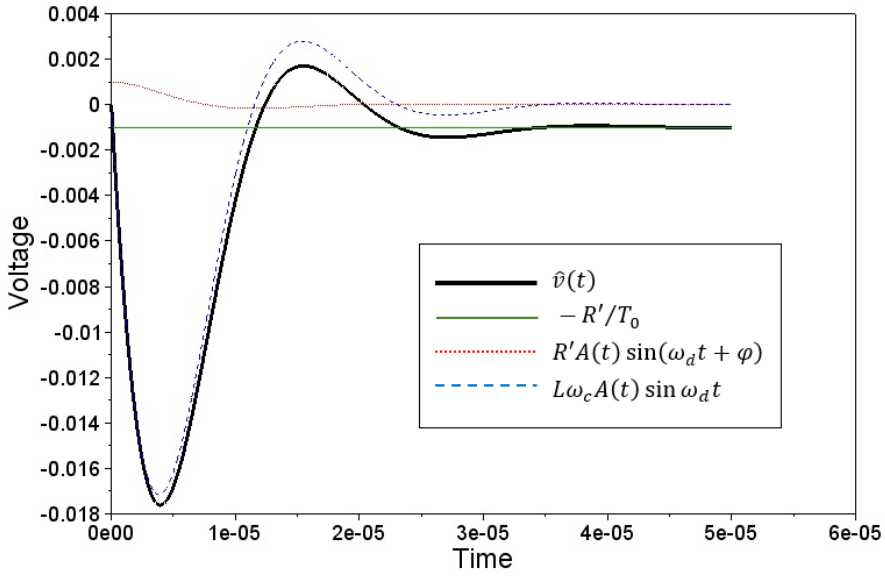


Fig. 3.13 Unit-step response of $Z_{out\_c}(s)$ @ $Q_c' = 1$, including power loss elements

3.1.2.4 Summary

By analyzing the relation between the transient response in time-domain and the system characteristics in frequency-domain, we can find some design principle to improve the dynamic performance of switching converter:

(1) Large dc gain can remove the offset and suppress the overshoot in line and load transient response.

(2) Large resonant frequency ω_c provides large attenuation time-factor, and it can shorten response time. (The resonant frequency of closed-loop gain just is the crossover frequency of loop gain)

(3) Setting the closed-loop damping factor Q_c around 0.5 should be a good

choice to balance the overshoot phenomenon and response time.

3.2 DESIGN THE FEEDBACK CONTROLLER

The elementary motivation of feedback controller design is the system stability. A stable open-loop system possibly becomes unstable after adding a feedback loop. Even if the loop gain contains no right half-plane poles (RHP), it is possible for the closed-loop transfer function to contain RHP. Then the feedback loop fails to regulate the system at the desired quiescent operation point, and oscillations are usually observed. It is important to avoid this situation.

Under the premise that the system is stable, we can change the system frequency characteristics by designing the feedback controller. A large dc gain, a large resonant frequency and an opportune damping factor all can be obtained.

3.2.1 System stability

As well known, the stability of a closed-loop system depends on whether the closed-loop transfer function contains right half-plane poles. According to the Nyquist stability criterion, if the number of closed-loop roots in the right half of the s-plane is Z, the number of open-loop roots in the right half-plane is P and the number of times that open-loop frequency characteristic curve (the frequency is from $-\infty$ to $+\infty$) encircles the point $(-1, j0)$ is N. the relation of the three numbers is: Z=N+P. The open-loop transfer function of any switching converter maybe has right half-plane zero, but absolutely not has right half-plane pole. Therefore, in any switching converter, P=0. If N=0, then Z equal to zero, no contain right half-plane pole in the closed-loop transfer function, the system is stable, otherwise unstable.

Fig. 3.14 shows the Nyquist plot of an open-loop transfer function. With an auxiliary unit circle, we can check whether the frequency characteristic curve encircles the point $(-1, j0)$.

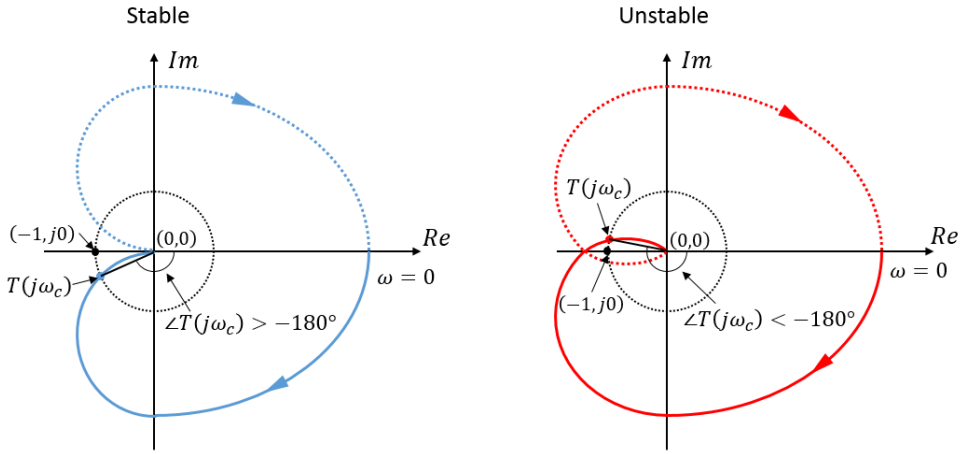


Fig. 3.14 Nyquist stability criterion for the system which no RHP is included in the loop transfer function

The frequency characteristic curve of the open-loop transfer function $T(s)$ can be expressed on a complex plane as

$$\|T(j\omega)\|\angle T(j\omega) \tag{3.40}$$

The crossover frequency ω_c is defined as the frequency where the magnitude of the loop gain is unity. As shown in Fig. 3.14, the intersection of the unit circle and the curve just is the point at ω_c. Then whether or not this curve encircles the point $(-1\,,\ j0\,)$ has a relation with the phase of the open-loop gain at crossover frequency: if $\angle T(j\omega_c)$ is higher than $-180°$, the curve will not encircle $(-1\,,\ j0\,)$. According to the Nyquist stability criterion, when the closed-loop transfer function will not include RHP, the system is stable. If $\angle T(j\omega_c)$ is lower than $-180°$, the curve encircles $(-1\,,\ j0\,)$ at least once, the system is unstable.

Therefore, to determine the stability of a closed-loop system (as the switching converter, there is not RHP in the open-loop transfer function) is simplified to check the phase of open-loop transfer function at the crossover frequency. Conventionally, we use the phase margin φ_m that is defined as

$$\varphi_m = 180° + \angle T(j\omega_c) \tag{3.41}$$

to evaluate the system stability: $\varphi_m > 0$, the system is stable. Otherwise, it is unstable.

3.2.2 Relationship between phase margin and closed-loop damping factor Q_c

Theoretically, even if the phase margin is only 1°, the system is stable. A good design should have adequate design margins. However, there is another important reason why additional phase is needed. The reason is the relationship between the phase margin and the closed-loop damping factor. In fact, we can express Q_c as a function of the phase margin

$$Q_c = \frac{\sqrt{\cos \varphi_m}}{\sin \varphi_m} \tag{3.42}$$

This function is plotted in Fig. 3.15, with Q_c expressed in dB.

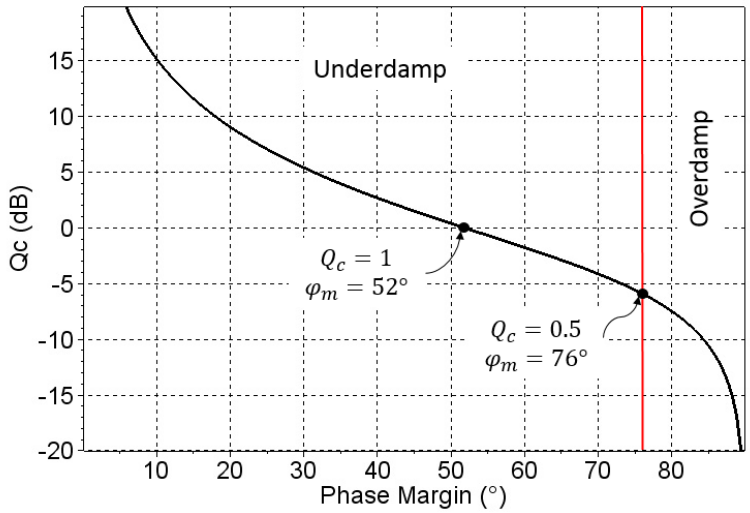


Fig. 3.15 Relationship between φ_m and Q_c

It can be seen that small phase margin causes large Q_c. When the phase margin is zero, Q_c is infinite. As mentioned in section 3.1.2, it means that the system is undamped. The oscillation caused by disturbance cannot be suppressed. This verifies the stability criterion from the other viewpoint.

We have known that a reasonably small Q_c is helpful for obtaining rapid response and small overshoot. In a practical design, the phase margin normally is chosen from 40° to 60° to get Q_c from 1.36 to 0.82.

3.2.3 Controller design

In order to get desired dynamic performance, the error amplifier that works as a controller must be designed. According to the transient response analysis in previous section, this controller only provides a dc gain to the system. This type is called proportional (P) controller. P control does not affect the phase of the open-loop gain. Except P control, there are the other two type controllers---integral (I) control and derivative (D) control. I control provides an infinitely large dc gain. D control can increase the phase. Since the I control and the D control both can regulate the phase, they are also called as phase compensator. Combining them to design the controller, we can obtain a large gain at low frequency and a high crossover frequency with a satisfactory phase margin.

3.2.3.1 Lead (PD) compensator

This type of compensator transfer function is used to improve the phase margin. A zero is added to the loop gain, at a frequency ω_z sufficiently far below the desired crossover frequency ω_c, such that the phase margin of the loop $T(s)$ is increased. The lead compensator is a combination of proportional control and derivative control, it is also called PD controller. It often finds application in the second-order system which originally contains a two-pole response. The effect of a zero is not only increase by $90°$ phase for the system, at the same time it causes the compensator gain to increase with the slope +20dB/decade. As we know, the original slope of second-order system is -40dB/decade at higher than the resonate frequency ω_0. After adding a zero into the system, the slope is increased from -40dB/decade to -20dB/decade when the frequency is higher than ω_z. The crossover frequency can be pushed to higher.

However, since the gain of any practical amplifier must tend to zero at high frequency, it cannot increase as +20dB/decade forever. Even if the amplifier is ideal, we hope the compensator gain is enough small at the switching frequency. If not, the switching harmonics are amplified by the compensator. It will disrupt the operation of the pulse-with modulator. Therefore the compensator transfer function $G_c(s)$ must contain a high frequency pole to attenuating high-frequency noise and combine with the low-frequency zero for a desired phase margin (as mentioned 40°~60°). If we consider the effect of equivalent series

resistance (ESR) in the output capacitor which provide an additional zero at the frequency $\omega_{ESR} = 1/Cr_{ESR}$, for the same reason, more than one high-frequency poles are required possibly.

A simplified example containing a single high-frequency pole is given in Eq. (3.43) and illustrated in Fig. 3.16

$$G_c(s) = G_{c0}\frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)} \tag{3.43}$$

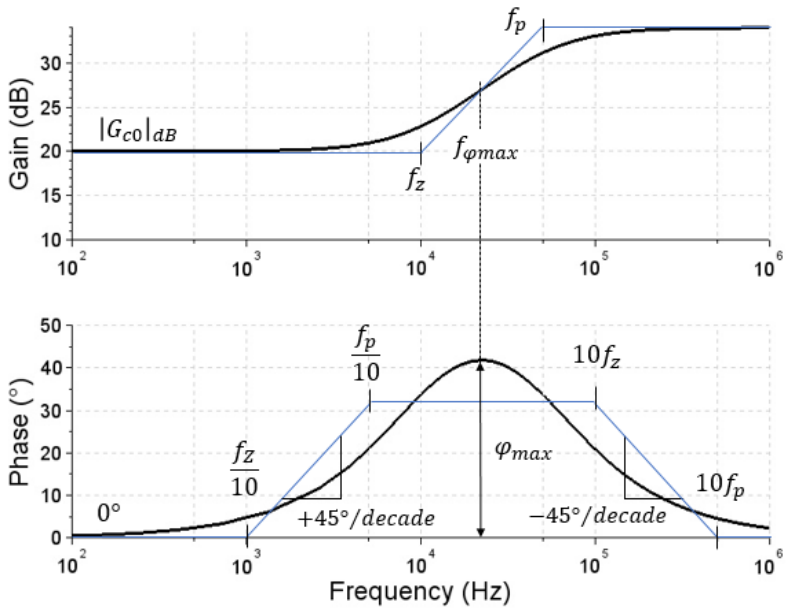


Fig. 3.16 Bode plot of the lead (PD) compensator

The maximum phase occurs at a frequency $f_{\varphi max}$ given by the geometrical mean of the pole and zero frequencies. This geometrical mean is in logarithmic, and $f_{\varphi max}$ can be found through

$$f_{\varphi max} = \sqrt{f_z f_p} \tag{3.44}$$

The maximum phase also can be expressed by the pole and zero frequency

$$\frac{f_p}{f_z} = \frac{1+\sin\varphi_{max}}{1-\sin\varphi_{max}} \tag{3.45}$$

As mentioned, this type compensator can increase the gain. At the frequency $f_{\varphi max}$, the compensator gain

$$G_c(s) = G_{c0}\sqrt{f_p/f_z} \tag{3.46}$$

Let us consider the case that this type compensator is applied in a practical second-order system. First, to determine the desired crossover frequency f_c and the phase margin φ_m. Then the maximum phase frequency $f_{\varphi max}$ is set at f_c, according Eqs. (3.44) and (3.45), the pole and zero frequencies are determined as

$$f_z = f_c\sqrt{\frac{1-\sin\varphi_m}{1+\sin\varphi_m}} \quad , \qquad f_p = f_c\sqrt{\frac{1+\sin\varphi_m}{1-\sin\varphi_m}} \tag{3.47}$$

Finally, according to the magnitude of the uncompensated system at f_c and Eq. (3.46), we determine the dc gain G_{c0}. By use of this type of compensator, the crossover frequency can be extended while maintaining an acceptable phase margin.

3.2.3.2 Lag (PI) compensator

This type of compensator is used to increase the low-frequency loop gain. A zero-pole provides an infinitely large gain at dc theoretically, such that the offset in output is removed. However, the $-90°$ initial phase must be compensated by a zero. If this compensator is applied in a second-order system, the zero frequency ω_L should be below the resonant frequency ω_0. If not, the magnitude of loop gain will decrease by -60dB/decade. The crossover frequency will not high enough and the phase margin is quite possibly lower than zero. The system is unstable. Therefore, the zero must be inserted at a frequency where well below the resonant frequency ω_0. The transfer function of this type compensator is given by

$$G_c(s) = G_{c\infty}\left(1+\frac{\omega_L}{s}\right) \tag{3.48}$$

Fig. 3.17 shows the Bode plot and asymptotes of the transfer function $G_c(s)$

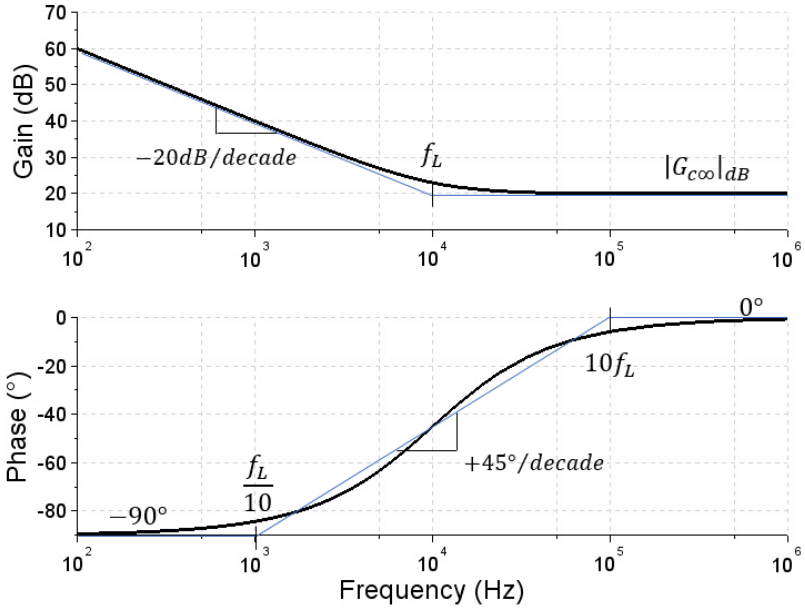


Fig. 3.17 Bode plot of the lag (PI) compensator

From Fig. 3.17, it can be seen that the phase is increased to $0°$ at the frequency $10f_L$. Therefore, a conservative design will set the zero at $f_L = f_0/10$. Of cause, in order to pursue a larger magnitude of the loop gain, the zero can be set just at f_0, but a large enough dc gain $G_{c\infty}$ is required to avoid the crossover frequency below $10f_L$.

3.2.3.3 Error amplifier design

The compensator (controller) is realized around the operational-amplifier (op-amp) which is used to amplify the deviation between the output voltage and the reference signal. To distinguish with the other op-amp in circuit, it is called error amplifier. According to the negative feedback principle of op-amp, we can insert appropriate resistors and capacitors into the inverting terminal and the feedback path (from the output terminal to the inverting terminal), then the zeros and poles are added to the op-amp transfer function $G_c(s)$. There are three common types for compensator design.

The configuration and the gain of Type 1 compensator is illustrated in Fig. 3.18.

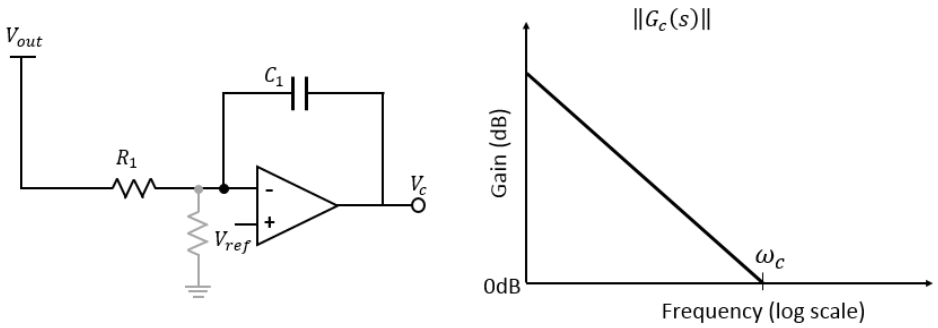


Fig. 3.18 Simplified transfer function plots of Type 1 compensator

The transfer function of Type 1 is given by

$$G_c(s) = \frac{\omega_c}{s} \tag{3.49}$$

Where $\omega_c = 1/C_1R_1$. It only has a zero-pole to provide large gain at low-frequency. It nearly cannot be used in switching converter.

Fig. 3.19 shows a Type 2 compensator.

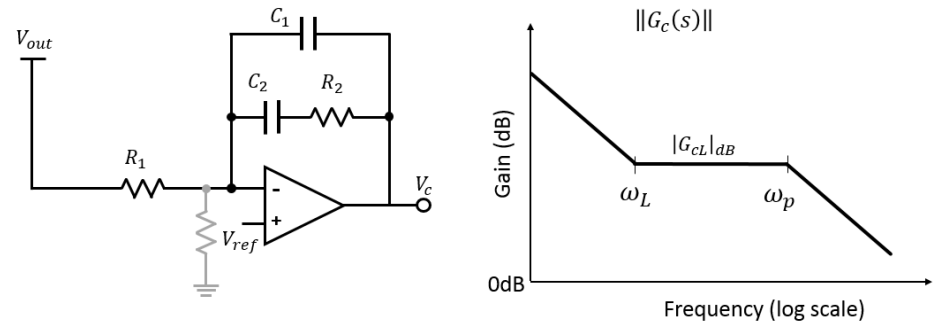


Fig. 3.19 Simplified transfer function plots of Type 2 compensator

The transfer function of Type 2 is given by

$$G_c(s) = G_{cL}\frac{1+\frac{\omega_L}{s}}{1+\frac{s}{\omega_p}} \tag{3.50}$$

Where $\omega_L = 1/C_2R_2$, $\omega_p = (C_1 + C_2)/C_1C_2R_2$ and $G_{cL} = C_2R_2/(C_1 + C_2)R_1$. It can be seen as inserting a high-frequency pole into a lag compensator. Type 2

compensator cannot increase the phase margin of loop gain; it normally is not applied in a second-order system. Nevertheless, for a first-order system as the switching converter with current mode control, Type 2 is a good choice. The zero frequency ω_L is set at the single pole of the original system---ω_τ. In switching converter application, the high-frequency pole at ω_p is set at ESR zero. The gain G_{cL} is determined by the desired crossover frequency ω_c, given by

$$G_{cL} = \frac{\omega_c}{\omega_\tau} \tag{3.51}$$

The configuration and the gain of Type 3 compensator are illustrated in Fig. 3.20

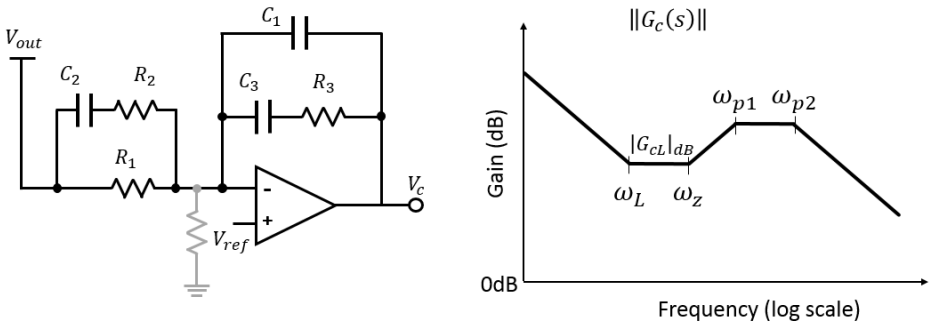


Fig. 3.20 Simplified transfer function plots of Type 3 compensator

The transfer function of Type 3 is given by

$$G_c(s) = G_{cL}\frac{\left(1+\frac{\omega_L}{s}\right)\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{3.52}$$

Where $\omega_L = 1/\big(C_2(R_1+R_2)\big)$, $\omega_z = 1/C_3R_3$, $\omega_{p1} = (C_1+C_3)/C_1C_3R_3$, $\omega_{p2} = 1/C_2R_2$ and $G_{cL} = \big(C_2(R_1+R_2)\big)/\big((C_1+C_3)R_1\big)$. It can be seen as a lag compensator combining with a lead compensator that has two high-frequency poles. Type 3 compensator provides large dc gain and extends crossover frequency to a desired high frequency while maintaining an acceptable phase margin. It always finds application in a second-order system. The first zero is conservatively set at one-tenth of the two-poles resonant frequency, $\omega_L = \omega_0/10$. According to the desired crossover frequency and phase margin to set the second zero at ω_z and the first pole at ω_{p1}. The second pole is used to eliminate the ESR zero. The gain G_{cL} is determined by the magnitude of uncompensated system at the crossover frequency, given by

$$G_{cL} = \frac{1}{G_{un}(\omega_c)}\sqrt{\frac{\omega_z}{\omega_{p1}}} \tag{3.53}$$

Where $G_{un}(s)$ is the transfer function of uncompensated system. In a switching converter, it is the transfer function $H(s)G_{vd}(s)/V_p$.

3.2.4 Design example

A dc-dc buck converter as example is used to illustrate the design procedure for the compensator. Both of voltage-mode control and current-mode control are considered. The parameters of the buck converter are listed in Table. 3.1.

Table. 3.1 Parameters of a dc-dc buck converter

V_g	5V	L	10μH	R_{ESR}	2mΩ
V_{out}	3.5V	C	50μF	R'	50mΩ
f_s	1MHz	R	35Ω		

f_s is the switching frequency, R_{ESR} is the equivalent-series-resistance of the output capacitor, and all of the power-loss elements as a resistance R′ in series with the inductor, $R' = R_L + DR_{on} + D'R_D$. From these parameters, we can work out that the quiescent operating point of duty cycle is $D = 0.7$, and the load current is $I_{out} = 100mA$.

The compensator should be designed for voltage-mode control and current-mode control respectively. After a demo of design procedure, comparison of transient response with various crossover frequencies and phase margins should be shown.

3.2.4.1 Compensator design for VMC

In voltage-mode control, there are two other parameters need to be set; voltage sensor's transfer function H(s) and the peak value of the triangular wave V_p. For

simplicity, $\mathrm{H}(s)$ is set as 1 and V_p is set as 3V. Then the transfer function without compensation is given

$$T_{un}(s) = \frac{1}{V_p} H(s) G_{vd}(s) = \frac{V_g}{V_p} \frac{\frac{s}{\omega_{ESR}} + 1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0 \omega_0} + 1} \tag{3.54}$$

Where

$\omega_{ESR} = \frac{1}{CR_{ESR}}$

$\omega_0 = \sqrt{\frac{1+R\prime/R}{LC}}$

$Q_0 = \frac{R\sqrt{1+R\prime/R}}{\sqrt{L/C}+R(R_{ESR}+R\prime)\sqrt{C/L}}$

Substituting the parameters, the resonant frequency at $\omega_0 = 4.48 \times 10^4 rad/s$, ESR zero occurs at $\omega_{ESR} = 1 \times 10^7 rad/s$ and the damping factor is $Q_0 = 7.75$.

The uncompensated transfer function describes a second-order system. Type 3 compensator will be design. The two poles at resonant frequency cause the phase $180°$ decrease, and make the phase margin is nearly zero. As the example, set the desired phase margin at $\varphi_m = 50°$ to obtain a closed-loop damping factor with $Q_c \approx 1$. In order to attenuate the switching frequency harmonics, the crossover frequency must be below half of f_s. A typically design of crossover frequency is $f_c = f_s/10$, in this example

$$f_c = f_s/10 = 100\mathrm{kHz} \tag{3.55}$$

According to Eq. (3.47), the zero and pole besides the crossover frequency in Fig. 3.20 is given by

$$\omega_z = 2\pi f_c \sqrt{\frac{1-\sin\varphi_m}{1+\sin\varphi_m}} = 2.29 \times 10^5 rad/s$$

$$\omega_{p1} = 2\pi f_c \sqrt{\frac{1+\sin\varphi_m}{1-\sin\varphi_m}} = 17.25 \times 10^5 rad/s \tag{3.56}$$

The second pole is set at ESR zero frequency, $\omega_{p1} = \omega_{ESR}$. The magnitude of G_{cL} is decided by the magnitude of uncompensated transfer function at the crossover frequency

$$G_{cL} = \frac{1}{T_{un}(\omega_c)}\sqrt{\frac{\omega_z}{\omega_{p1}}} = 42.85 \tag{3.57}$$

By now, the lead compensation part of Type 3 compensator is completed. Then consider the lag compensation at low frequency. The zero is set at

$$\omega_L = \omega_0/5 = 8.95 \times 10^3 \ \ rad/s \tag{3.58}$$

The complete Type 3 compensator transfer function in Eq. (3.52) becomes

$$G_c(s) = 42.85 \times \frac{\left(1 + \frac{8.95 \times 10^3}{s}\right) \times \left(1 + \frac{s}{2.29 \times 10^5}\right)}{\left(1 + \frac{s}{17.25 \times 10^5}\right) \times \left(1 + \frac{s}{1 \times 10^7}\right)} \tag{3.59}$$

Then, calculate the values of resistances and capacitors around the error amplifier for the determined zeros and poles of compensator. The relationships are reviewed as

$$G_{cL} = \frac{C_2(R_1 + R_2)}{(C_1 + C_3)R_1}$$

$$\omega_L = \frac{1}{C_2(R_1 + R_2)}, \qquad \omega_z = \frac{1}{C_3 R_3} \tag{3.60}$$

$$\omega_{p1} = \frac{C_1 + C_3}{C_1 C_3 R_3}, \qquad \omega_{p2} = \frac{1}{C_2 R_2}$$

First let us fix a value, set $R_1 = 10k\Omega$, and then the calculation procedure is as follow

(1) From ω_z and ω_{p1}, the relationship between C_1 and C_3:

$C_3 = (\omega_{p1}/\omega_z - 1)C_1$

(2) G_{cL} is multiplied by ω_L to get an equation which only includes R_1, C_1 and C_3. R_1 is fixed, and then substitute the relation in (1). The values of C_1 and C_3 are obtained

(3) Use C_3 and ω_z to calculate R_3: $R_3 = 1/C_3\,\omega_z$

(4) Substitute $C_2R_2 = 1/\omega_{p2}$ into ω_L to calculate C_2:

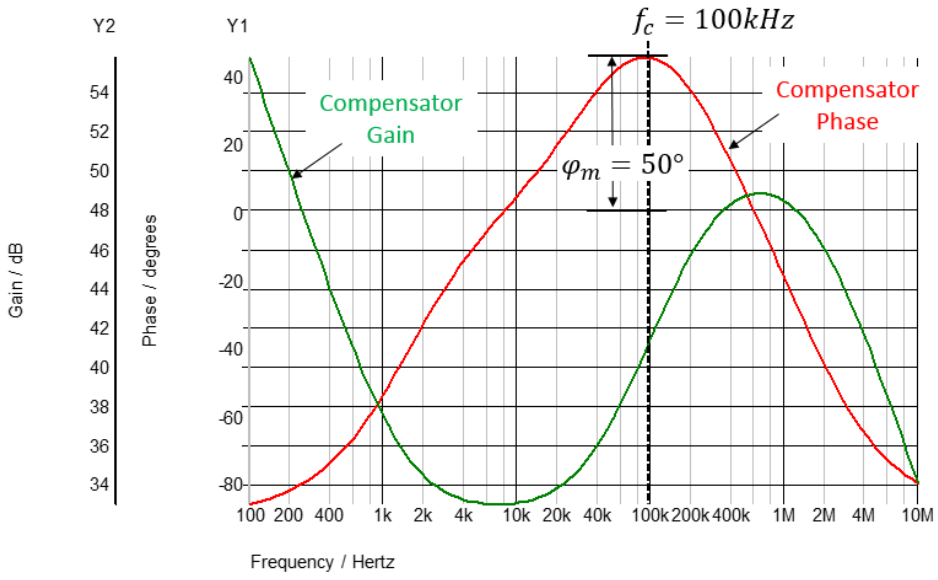
$C_2 = \left(1/\omega_L - 1/\omega_{p2}\right)/R_1$

(5) Use C_2 and ω_{p2} to calculate R_2: $R_2 = 1/C_2\,\omega_{p2}$

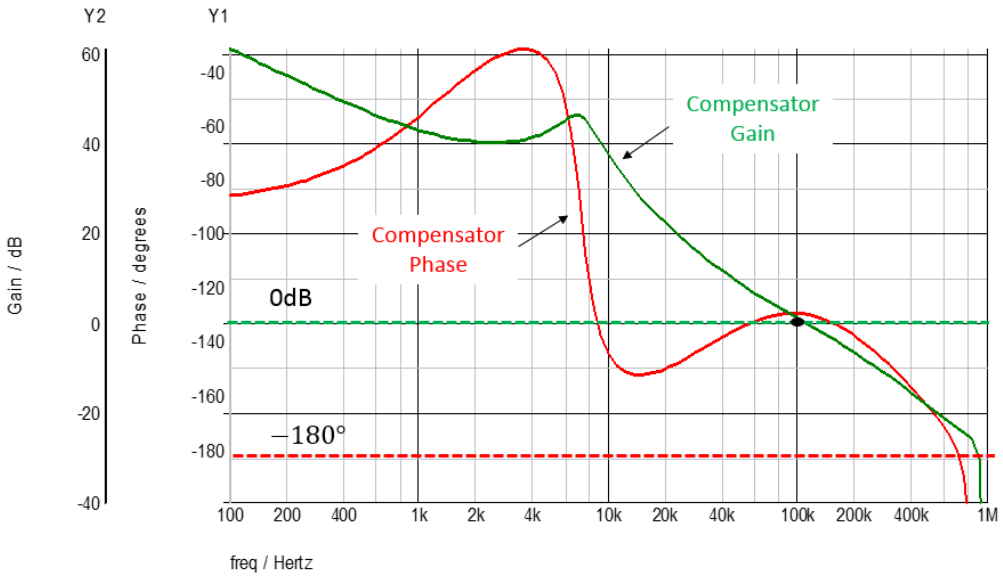
For this example, the results are:

$R_1 = 10k\Omega$, $R_2 = 8.96\Omega$, $R_3 = 1.93k\Omega$, $C_1 = 34.6p\text{F}$, $C_2 = 11.2n\text{F}$ and $C_3 = 226p\text{F}$.

The Bode plots of compensator and compensated loop gain are sketched by SIMetix and shown in Fig. 3.21



(a) $G_c(s)$



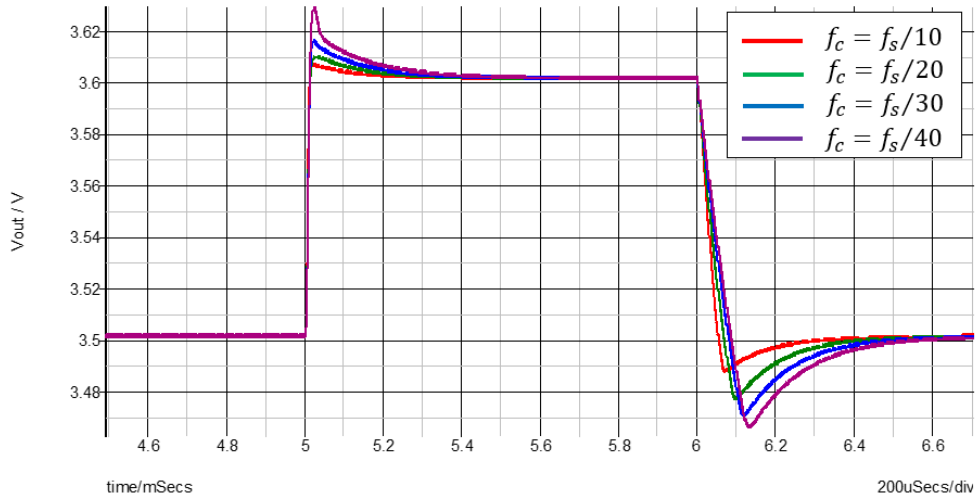
(b) $\mathrm{T}(s) = H(s)G_c(s)G_{vd}(s)/V_p$

Fig. 3.21 Bode plots of compensator design.

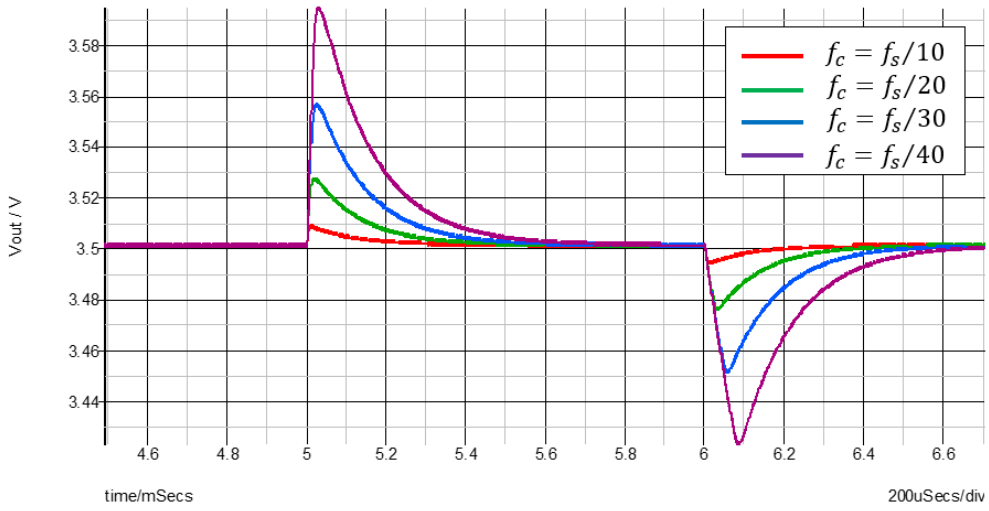
(a) Designed compensator transfer function $G_c(s)$

(b) Compensated loop gain transfer function $T(s)$

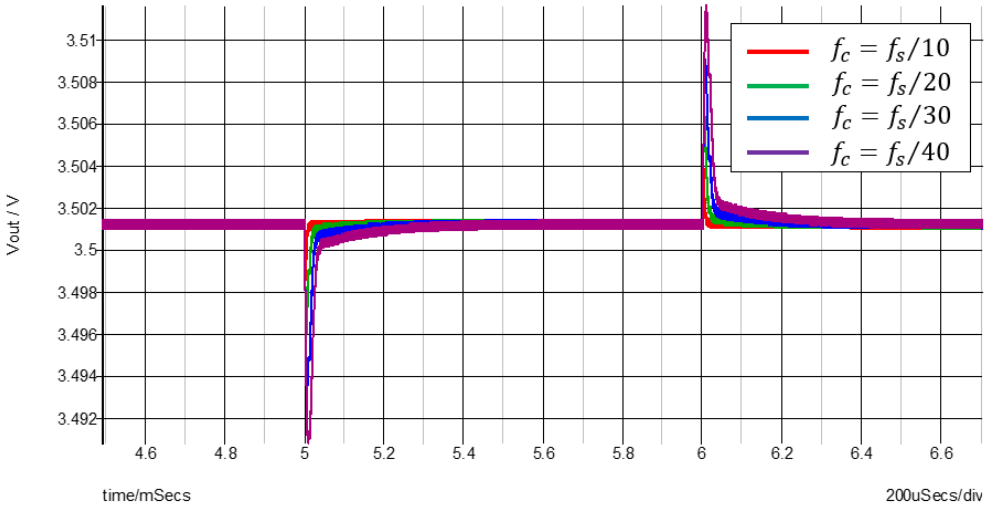
Following the design procedure, various values of loop gain crossover frequency and phase margin can be obtained by Type 3 compensator. The transient responses with different crossover frequencies are compared in Fig. 3.22. The transient responses with different phase margins are compared in Fig. 3.23.



(a) Reference transition response. V_{ref}: 3.5V ↔ 3.6V



(b) Line transition response. V_g: 5V ↔ 6V

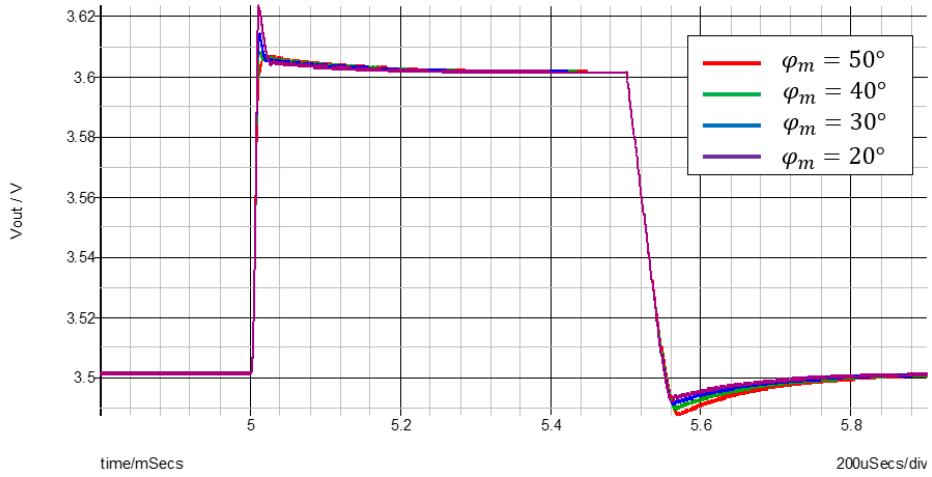


(c) Load transition response. I_{out}: 100mA ↔ 200mA

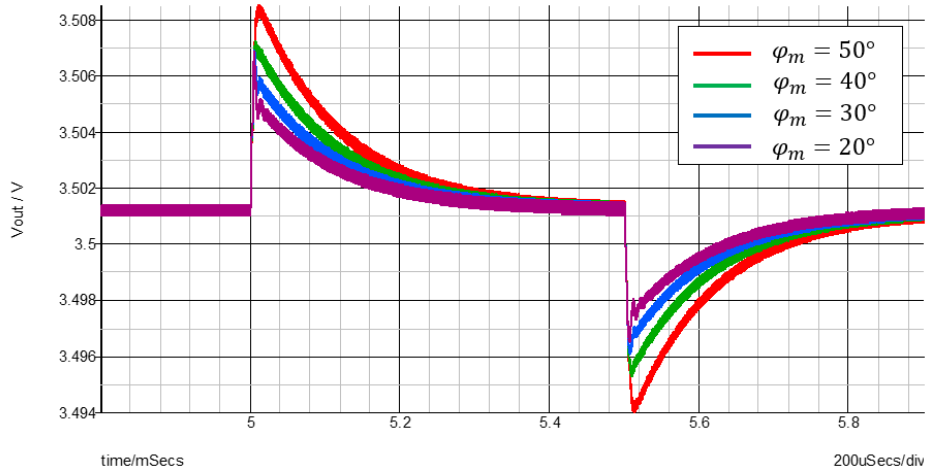
Fig. 3.22 Transient responses with different crossover frequencies @$\varphi_m = 50°$

The results shown in Fig. 3.22 verify the analysis that higher crossover frequency (also be called closed-loop bandwidth) can improve the transient response, no matter the transient response is caused by the reference signal, or the input voltage or the load current.

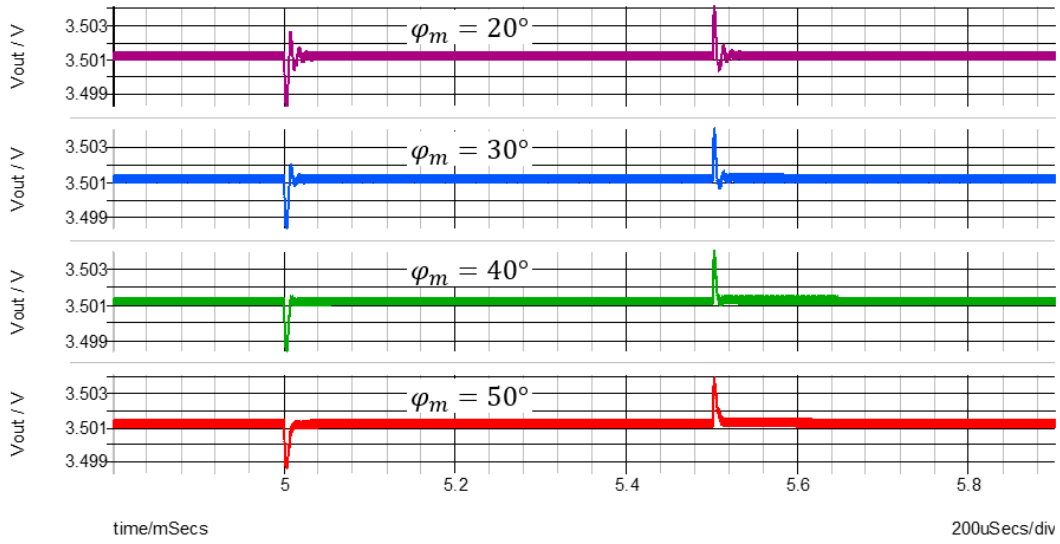
The comparison of transient responses with different phase margin shows us visual results that how phase margin affects the transient response. In some case, a small phase margin (large closed-loop damping factor Q_c) can suppress the overshoot in output voltage, for example, in the line transient response. However, at the same time, oscillation appears on the output voltage. For example, in the load transient response, the oscillation caused by the small phase margin, $\varphi_m = 20°$, prolongs the response time. We need a compromise choice. Only for the example buck converter, setting the phase margin at $40°$ can avoid the osillation phenomenon and suppress the overshoot.



(a) Reference transition response. V_{ref}: 3.5V ↔ 3.6V



(b) Line transition response. V_g: 5V ↔ 6V



(c) Load transition response. I_{out}: 100mA ↔ 200mA

Fig. 3.23 Transient responses with different phase margin $@f_c = f_s/10$

3.2.4.2 Compensator design for CMC

In current-mode control, we still need an output voltage sensor, and the transfer function is set as $H(s)=1$. However, the triangular wave what compares to the control variable is derived from the inductor current. Which is required is a current sensor, instead of the peak value of triangular wave. The triangular wave is proportional to the inductor current, and triggers the latch to turn off the switch element when it rises up to the control variable. Therefore, only the inductor current waveform when the switch turns on. In consideration of power loss, the current sensor resistance R_s is always placed between the input voltage source and the switch element. This current sensor resistance should also be considered to the amount of power-loss elements

$$R'_{cmc} = R' + R_s D \tag{3.61}$$

If $R_s = 100\text{m}\Omega$, the amount of power-loss elements in this example becomes $R'_{cmc} = 120m\Omega$. Sometimes since the inductor current is small, we need amplify the voltage signal $i_L(t)R_s$ to get a triangular waveform that is in the same order to magnitude with the control variable signal. Here, I use a transform with $1:n_t$ turns ratio. Supposing $n_t = 100$, the current sensor transfer function

in the current loop becomes a constant $n_t R_s = 10\Omega$.

The transfer functions from the duty cycle to the inductor current and from the inductor current to the output voltage are given

$$G_{ld}(s) = \frac{V_g}{R} \frac{\frac{s}{\omega_\tau} + 1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0 \omega_0} + 1} \tag{3.62a}$$

$$G_{vl}(s) = R \frac{\frac{s}{\omega_{ESR}} + 1}{\frac{s}{\omega_\tau} + 1} \tag{3.62b}$$

Where

$\omega_{ESR} = \frac{1}{CR_{ESR}}$

$\omega_0 = \sqrt{\frac{1+R\prime_{cmc}/R}{LC}}$

$\omega_\tau = \frac{1}{C(R+R_{ESR})}$

$Q_0 = \frac{R\sqrt{1+R\prime_{cmc}/R}}{\sqrt{L/C}+R(R_{ESR}+R\prime_{cmc})\sqrt{C/L}}$

Let us consider to close the current loop. The closed current loop is as a part of the voltage loop. Before designing compensator for the voltage loop, suppose $G_c(s) = 1$, then the current loop gain and the uncompensated voltage loop $T_{un}(s)$ can be expressed as

$$T_{iloop}(s) = n_t R_s \frac{f_s}{m} G_{ld}(s) \tag{3.63}$$

$$T_{un}(s) = H(s) G_{iloop} G_{vl}(s) \tag{3.64}$$

Where

$\mathrm{m} = \frac{V_g(1-D)}{L}$

$$G_{iloop} = \frac{T_{iloop}(s)}{n_t R_s\left(1+T_{iloop}(s)\right)}$$

The current loop, the closed current loop and the uncompensated voltage loop are sketched in Fig. 3.24

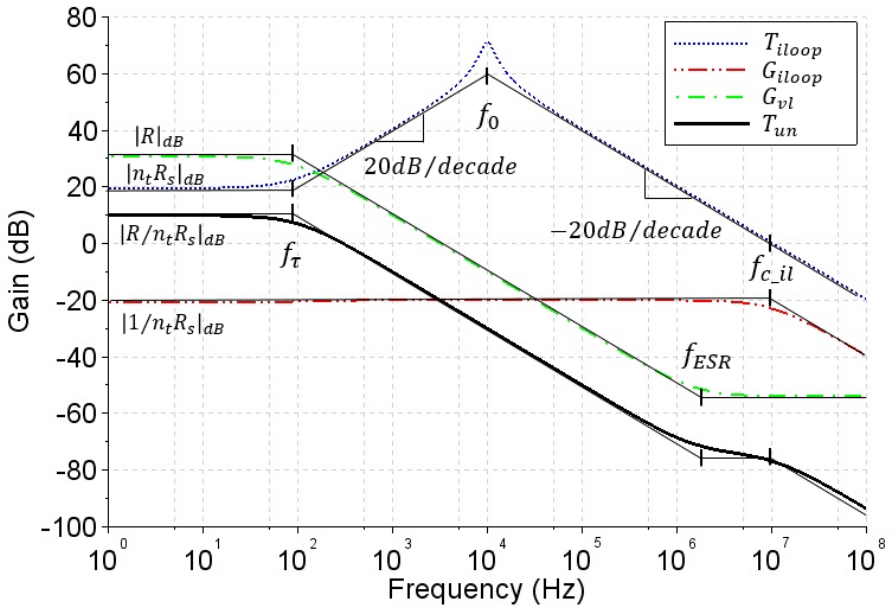


Fig. 3.24 Loop gains in current-mode control

The closed current loop can be seen as a constant in the range below the current loop crossover frequency f_{c_il}. The original LC two-poles at f_0 are separated into a low-frequency pole at f_τ and a high-frequency pole at f_{c_il}. If f_{c_il} is very high, even higher than the switching frequency, we can ignore its effect. The uncompensated voltage loop becomes a first-order system with a low-frequency pole. As the previous introduction, Type 2 compensator is good enough in this case.

Review the transfer function of Type 2 compensator

$$G_c(s) = G_{cL}\frac{1+\frac{\omega_L}{s}}{1+\frac{s}{\omega_p}} \tag{3.65}$$

Where $\omega_L = 1/C_2R_2$, $\omega_p = (C_1+C_2)/C_1C_2R_2$ and $G_{cL} = C_2R_2/(C_1+C_2)R_1$. The zero is set at CR pole frequency, $\omega_L = \omega_\tau$. The pole at ω_p is often used to eliminate the ESR zero, but in this case, the ESR zero is at a very high frequency, and can be neglect. Therefore, we can use the pole at ω_p to decrease the phase

around the desired crossover frequency. The relationship between the phase margin and the pole frequency is given by

$$\omega_p = \frac{\omega_c}{\cot \varphi_m} \tag{3.66}$$

The dc gain G_{cL} has two different expression, corresponding to $\varphi_m \geq 45°$ and $\varphi_m < 45°$ respectively.

$$G_{cL} = \begin{cases} \dfrac{\omega_c n_t R_s}{\omega_\tau R} & \varphi_m \geq 45° \\ \dfrac{{\omega_c}^2 n_t R_s}{\omega_p \omega_\tau R} & \varphi_m < 45° \end{cases} \tag{3.67}$$

Calculating the values of resistances and capacitors, the procedure is simpler than Type 3 compensator.

(1) R_1 is fixed as a reference.

(2) From ω_L and ω_p, the relationship between C_1 and C_2 is obtained:

$C_2 = \left(\omega_p/\omega_L - 1\right)C_1$

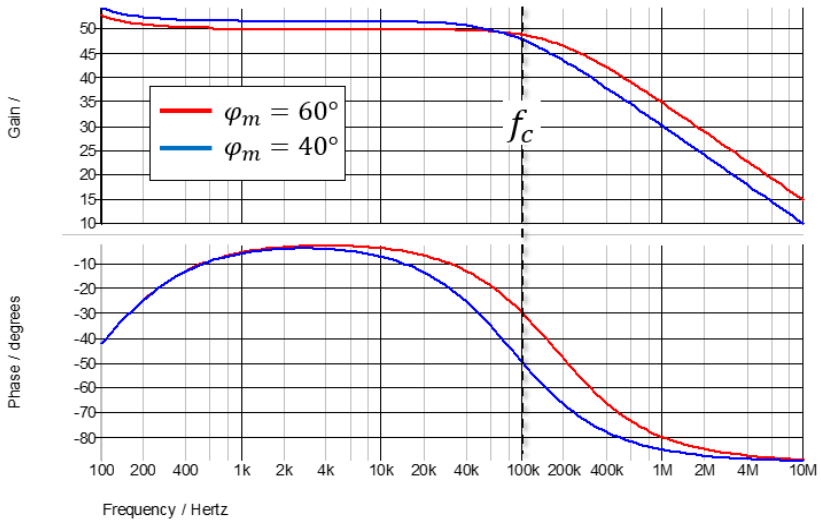
(3) G_{cL} multiplies by ω_p to get an equation only include R_1 and C_1.

$G_{cL}\omega_p = 1/C_1 R_1$

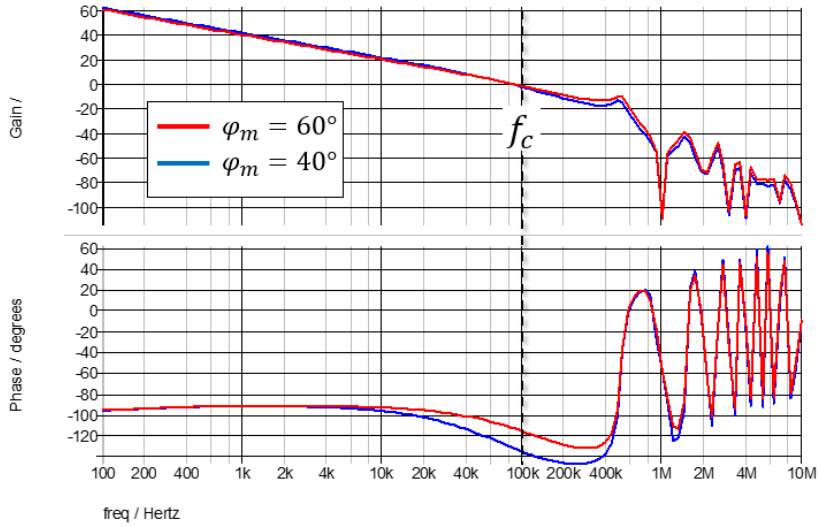
Since R_1 is fixed, the value of C_1 can be calculated, and then substitute the relation in (2), the value of C_2 can also be calculated.

(4) Use C_2 and ω_L to calculate R_2: $R_2 = 1/C_2\,\omega_L$

Two compensator designs as the example, the crossover frequencies both are set at $f_c = f_s/10$, while the phase margins are $40°$ and $60°$. The compensator gain and the compensated loop gain are shown in Fig.3.25.



(a) $G_c(s)$



(b) $T(s) = H(s)G_c(s)G_{iloop}(s)G_{vl}(s)$

Fig. 3.25 Bode plots of compensator design for current-mode control.

(a) Compensator transfer function $G_c(s)$

(b) Compensated loop gain transfer function $T(s)$

@ $f_c = f_s/10$, $\varphi_m = 40°$ and $60°$

3.3 PRACTICAL CHALLENGE

In previous introduction, we can design the feedback control system to get well dynamic performance. However, several practical issues must be considered. Because of these issues, we cannot design the system directly as the theoretically method.

3.3.1 Gain-bandwidth product of op-amp

There is a maximum value of gain in a practical op-amp. This maximum gain is called open-loop gain at low-frequency. At high-frequency, the open-loop gain deceases with frequency. It is because op-amp is designed to have a simple one-pole frequency response. The product of the op-amp's bandwidth and the gain at which the bandwidth is measured is called gain-bandwidth product (GBP). Fig. 3.26 is the loop gain and phase of a practical op-amp with open-loop gain=100k, GBP=20MHz.

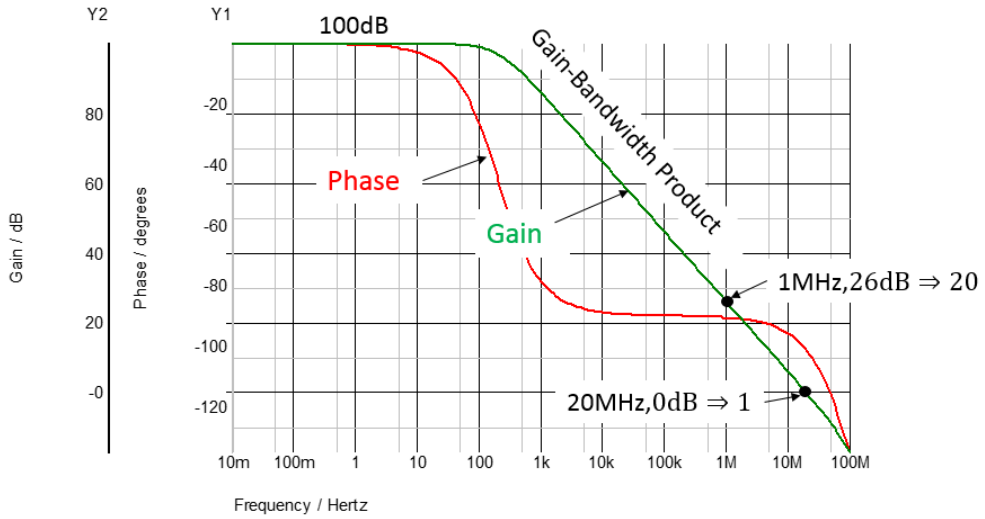


Fig. 3.26 Loop gain and phase of a practical op-amp

For an amplifier in which negative feedback reduces the gain to below the open-loop gain, the gain-bandwidth product of the closed-loop amplifier will be approximately equal to that of the open-loop amplifier. When we use op-amp to realize a compensator for switching converter, the GBP is a constraint in the high-frequency. Once the compensator's gain reaches this constraint, the gain will be

forced to decrease by slope -20dB/decade at higher frequency, no matter the original designed gain is 0dB/decade or 20dB/decade. It means that undesired single pole or two poles appear at the frequency where the designed compensator gain intersects with GBP. These undesired pole/poles will decrease the compensator's phase. Therefore, if these pole/poles appear around the designed crossover frequency, the phase margin is decreased. Especially, for the switching converter with voltage-mode control that uses Type 3 compensator, the phase margin is possibly decreased to less than zero, system unstable. To avoid the GBP effect, the crossover frequency can be designed at a very high frequency.

The op-amp in Fig. 3.26 is utilized to realize the Type 3 compensator in last section. Phase margin is designed as 50°, crossover frequency is designed at $f_s/10$ and $f_s/20$. Comparing to the compensator realized by ideal op-amp, the comparison result of compensator gain is shown in Fig. 3.27

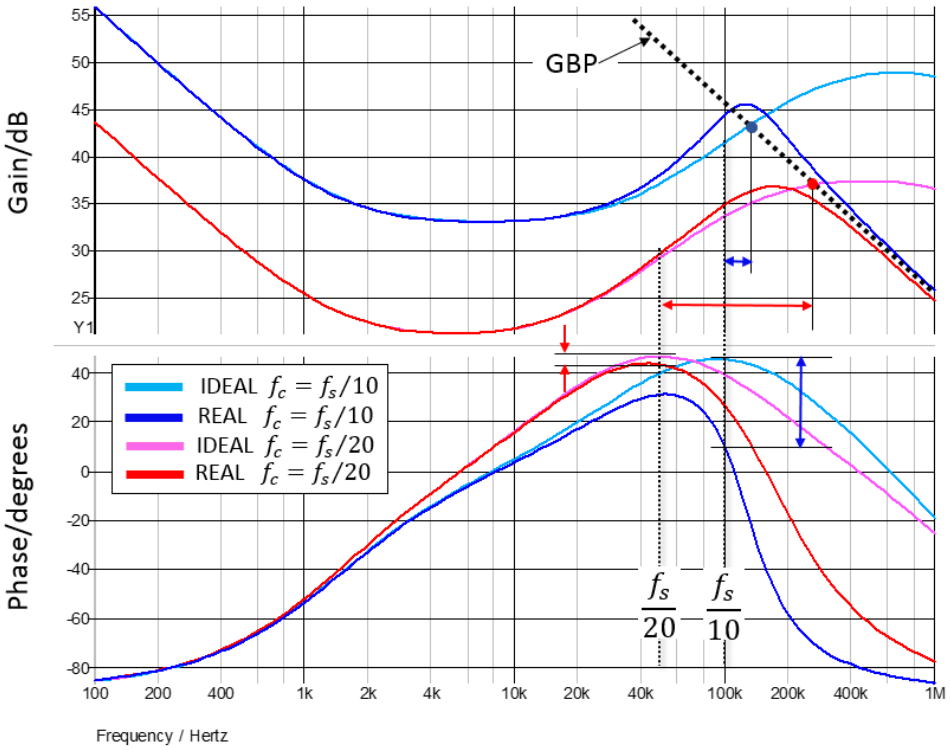


Fig. 3.27 Effect of GBP constraint for Type 3 compensator

In order to get high crossover frequency, not only the zero ω_z and the pole ω_{p1} in Type 3 should be pushed to higher frequency, but also the dc gain G_{cL} is also increased. This makes that the GBP caused two-poles are very close to the crossover frequency in the case of $f_c = f_s/10$. The phase is decreased near 30°

at $f_s/10$. By contrast, the GBP caused pole is far away from the crossover frequency in the case of $f_c = f_s/20$, and the effect on phase is small. Hence, considering the GBP, we cannot set the crossover frequency at theoretically high-frequency to guarantee the system stability.

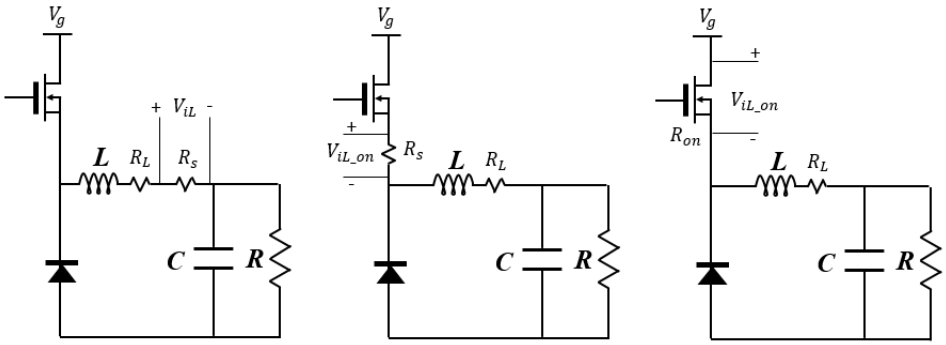
The GBP constraint also appears in Type 2 compensator, but not as severe as in Type 3 compensator; the gain of Type 2 compensator is not easy to reach that constraint. Even if the Type 2 gain reaches the constraint and the phase is decreased, the uncompensated loop gain originally has $90°$ phase margin. In the worst case, the loop gain does not have enough phase margin, but the system is stable at least. Hence, the current-mode control always has wider band than voltage-mode control.

3.3.2 Current sensor in current-mode control

Current sensing is one of the most important functions in switching converter. Regardless of the control type, the inductor current needs to be sensed for over-current protection. Not to mention in current-mode control, the inductor current is sensed for loop control. There are several current sensing techniques in switching converter. Here, we only discuss the ones that are appropriate for loop control.

The series sense resistor is the most common inductor current sensor. There are three realizing methods as shown in Fig. 3.28. The conventional way is simply inserts a sense resistor in series with the inductor, as shown in Fig. 3.28(a). Obviously, the power loss in sense resistor reduces the efficiency. Since only the inductor current during switch turn on is utilized for loop control, the sense resistor can be place forward in series with the switch element, as shown in Fig. 3.28(b). Therefore, power loss on the sense resistor only occurs when the switch is turned on. Further reducing power loss, the MOSFET switch acts as sense resistor when the switch turns on and the MOSFET is biased in triode region as shown in Fig. 3.28(c). By this way, no additional resistor to add power loss is required. However, R_{on} of MOSFET is inherently nonlinear and varies across temperature. Low accuracy is the main drawback. Comparing to be utilized for

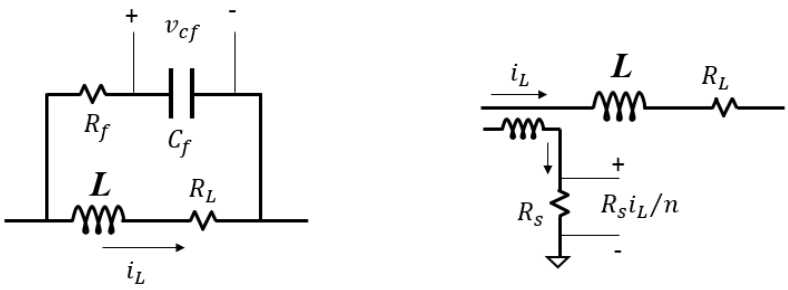
loop control, this method is more appropriate for over-current protection.



(a) (b) (c)

Fig. 3.28 Use series resistor as current sensor for CMC

Except for the series sense resistor, there are two other lossless current sensor techniques shown in Fig. 3.29.



(a) (b)

Fig. 3.29 Two lossless current sensor techniques

Filter sensor, shown in Fig. 3.29(a), uses a simple low-pass RC network to filter the voltage across the inductor and sense the current through the ESR of the inductor. When we carefully match the RC network to force $R_f C_f = L/R_L$, the voltage across the filter capacitor $v_{cf} = R_L i_L$, is directly proportional to inductor current. However, due to the tolerances of all the components, the matching equation is very difficult to satisfy. Fig. 3.29(b) shows a current transformer that senses a fraction of the inductor current flowing through a sense resistance. The voltage across R_s is proportional to the inductor current. The transformer cannot transfer the dc component which makes this method inappropriate for over-current protection. Both of these two current sensors are not appropriate

for integrated circuits.

However, not only an ideal current sensor with lossless and high-accuracy is the issue of sensing inductor current, CMC also suffers from high PCB sensitivity. A lot of noise is generated when the switch turns on. This make the waveform which proportional to the inductor current often contains leading-edge noise spikes caused by parasitic capacitance and diode recovery. We usually need to introduce a blanking time to avoid triggering the comparator for at least 50-200ns after the switch turns on. For high switching frequencies, this blanking time leads a minimum duty cycle that cannot be ignored for transient response or low conversion ratio.

3.3.3 Subharmonic instability and slope compensation

For CMC, the GBP constraint is not such rigorous as in voltage-mode control, however, there is another practical limit for CMC to prevent us to get wide closed-loop band (high crossover frequency of loop gain). It is the phenomenon of subharmonic instability which occurs only in current-mode control and duty cycles greater than 0.5 when inductor current is under continuous conduction mode (CCM).

The transfer function we use in Fig. 3.24 is very simplified. We ignore something that is relevant to understanding the practical limit of CMC. We can find a peaking in the gain plot at exactly half the switching frequency, as shown in Fig. 3.25(b). Therefore, CMC should model two-poles at this frequency, and the peaking in gain is a quality factor Q_s. If we do not limit this quality factor and push crossover frequency to a high-frequency close to the half switching frequency, Q_s possibly causes the gain to intersect the 0dB axis once again. Since any phase lower than $-180°$ at any crossover frequency can provoke full instability. The subharmonic instability phenomenon is illustrated as Fig. 3.30. Supposing a small perturbation δ which might occur in inductor current during the switch turn on. With less than 0.5 duty cycle, the perturbation effect will be reduced by the time when the next period start and eventually dies out. However, with more than 0.5

duty cycle, the perturbation effect will be larger at the start of the next period, resulting system unstable. The cure for this phenomenon is adding a ramp on top of the current waveform. This method is called slope compensation.

The relationship between the additional ramp and the quality factor Q_s is given by [28]

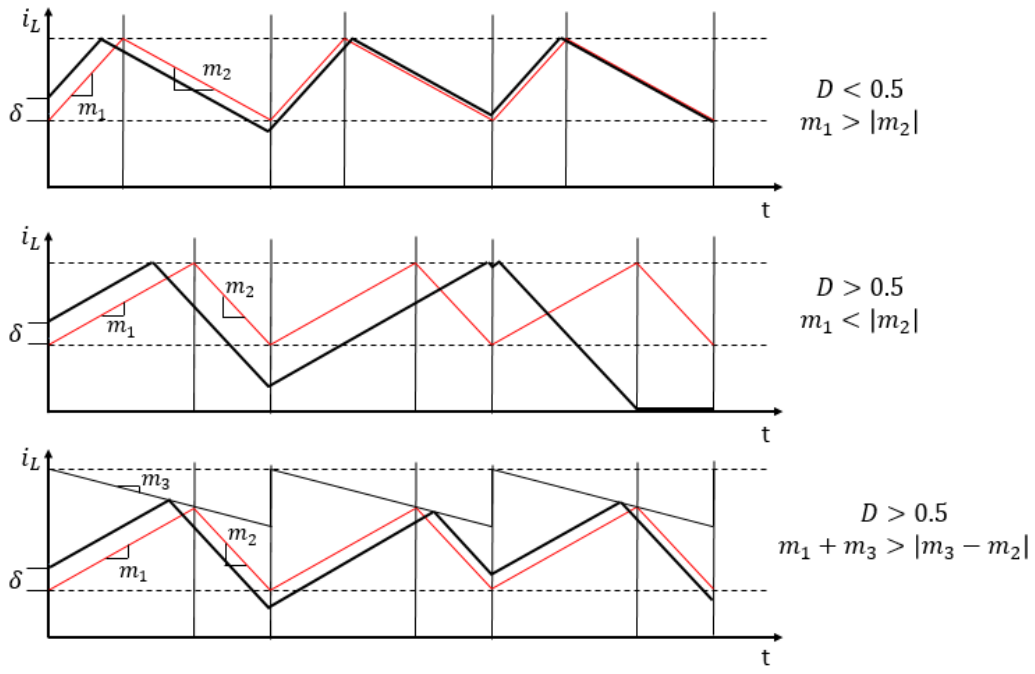


Fig. 3.30 Subharmonic instability and slope compensation

$$Q_s = \frac{1}{\pi(\gamma D' - 0.5)} \tag{3.68}$$

Where $\gamma = 1 + m_3/m_1$, is called slope compensation factor. In order to reduce Q_s, we need to apply greater slope compensation. However, the slope compensation can reduce the gain of current loop and voltage loop, and too much slope compensation makes the system more and more like VMC, LC two-poles will reappear potentially. But we have only considered to use Type 2 compensator for CMC, and the system still is unstable potentially.

CHAPTER IV

TRIANGULAR WAVE SLOPE MODULATION

Through the analysis in last chapter, we can see that in order to get well dynamic performance, we need:

a. A large dc gain for reducing offset in the output voltage.

b. A high gain bandwidth for shorten the response time.

c. A moderate phase margin for suppressing the oscillation in output voltage, but not overdampe too much.

Designing compensator for VMC and CMC respectively, under ideal conditions, a large dc gain is obtained by a low-frequency zero-pole (PI control); to place zeros and poles at advisable frequency, we can get the desired phase margin at the desired crossover frequency. Unfortunately, there are several practical limits always prevent us to design the compensator as we had thought initially. Except for those limitations, there are both the advantages and disadvantages of each control mode. Comparing to CMC, VMC does not require an accurate current sensor what causes additional power loss; no require slope compensation to guarantee the system stability when duty cycle is more then 0.5; no require blanking time to avoid the noise caused by the leading edge current spike when switch turns on; the single feedback loop is easier to design and analyze; even it has better cross-regulation with multiple outputs. [29]. Although VCM has so many advantages, it also has two main drawbacks that make more designer to have partiality for CMC. One is the LC two-pole force to employ Type 3 compensator which is limited by GBP of op-amp. Unless using an expensive high bandwidth op-amp to realize the Type 3 compensator, we have to set a low

bandwidth for VMC. The other disadvantage is that the change in line must first be sensed as an output change and then corrected by the feedback loop. This usually means bad line transient response.

Inspired from CMC, use an adjustable triangular wave to replace the conventional fixed triangular wave in VMC, and make the peak value of triangular wave proportional to the input voltage. By this way, a VMC buck converter (only for buck converter) can get a line feed-forward control function [30]. While how about load transient response? Is there a triangular wave modulation method which can improve the load transient response? In this chapter, we will introduce a novel triangular wave generator with which the slope of triangular wave is adjustable, and the dynamic performances of dc-dc buck converter with voltage-mode control are improved.

4.1 SLOPE ADJUSTABLE TRIANGULAR WAVE GENERATOR

4.1.1 Triangular wave slope modulation

Fig. 4.1 supposes a constant control variable and the slope of triangular wave is changed from m_1 to m_2. The relationship between the peak value and the slope is proportional, which is given by

$$V_{p1} = m_1 T_s,\ \ V_{p2} = m_2 T_s \quad \Longrightarrow \quad V_{p1}/V_{p2} = m_1/m_2 \tag{4.1}$$

The relationship between the duty cycle and the slope is inversely proportional, which is given by

$$D_1 = \frac{V_c}{m_1 T_s},\ \ D_2 = \frac{V_c}{m_2 T_s} \quad \Longrightarrow \quad \Delta \mathrm{d} = \left(\frac{1}{m_2} - \frac{1}{m_1}\right) V_c f_s = \Delta \frac{1}{m} V_c f_s \tag{4.2}$$

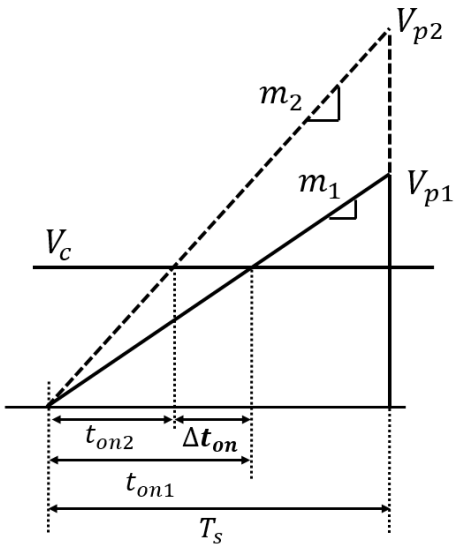


Fig. 4.1 Relationship between duty cycle, peak value and slope of triangular wave

Also supposing that the control variable V_c keeps on a constant value, the duty cycle modulation only depends on the changed slope. Let us consider how to regulate the slope to get line feed-forward control and deal with load transient response.

First, the line feed-forward control in buck converter means a control scheme that can build a proportional relationship between the input voltage and the peak value of triangular wave V_p. As we know, V_p is proportional to the slope. Therefore, in order to get line feed-forward control, the relationship between the input voltage and the slope should also be proportional.

In conventional VMC, the deviation in the output voltage $\Delta v = v_{out} - V_{ref}$, causes a proportional variation in the duty cycle. According to Eq. (4.2), in order to remove the deviation in the output voltage (no matter this deviation is caused by reference signal, input voltage or load current), the relationship between this deviation and the variation in the inverse of slope should be proportional. Hence, the ideal triangular wave modulations required to meet two conditions

$$v_g \propto m\,, \qquad \Delta v \propto \Delta\frac{1}{m} \tag{4.3}$$

We should design a triangular wave generator with which the triangular wave slope can be regulated as Eq. (4.3), and then use the adjustable triangular wave to replace the fixed triangular wave in the conventional VMC. Fig. 4.2 illustrates a dc-dc buck converter with the proposed method.

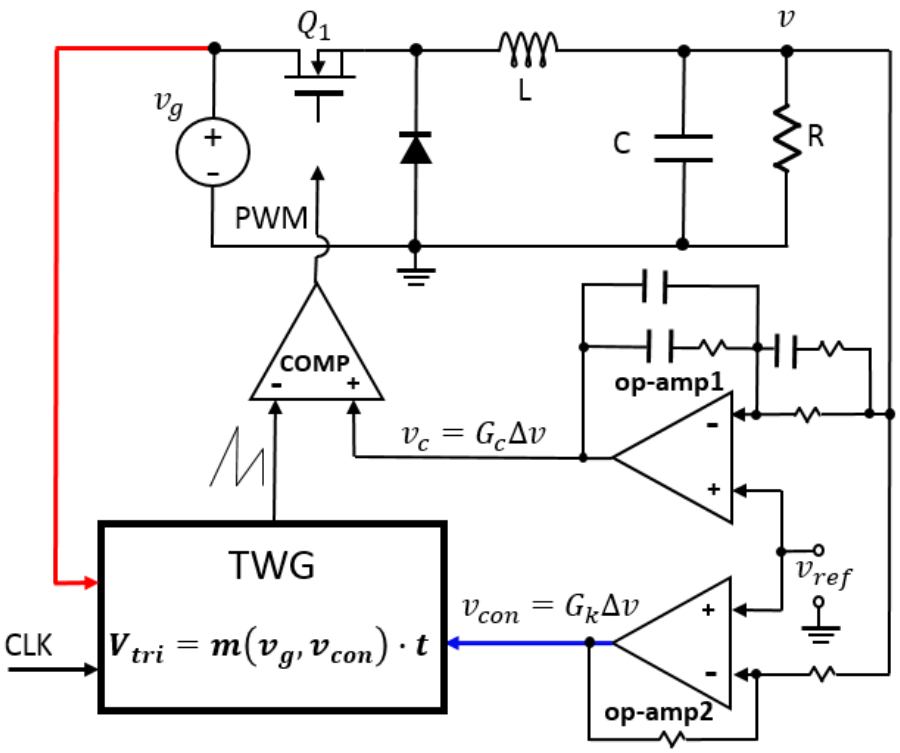


Fig. 4.2 Dc-dc buck converter with slope adjustable triangular wave generator

There are two op-amps utilized in feedback loop. Op-amp1 is used to generate a control variable voltage v_c which is compared to triangular wave and connected to the positive terminal of comparator. It is just the error amplifier in the conventional VMC. Of course, Type 3 compensator is realized around op-amp1. The gain of op-amp1 is denoted as $G_c(s)$. The function of op-amp2 is sensing and amplifying the deviation in the output voltage, and its output works as the other control variable for the TWG. To distinguish with the control variable v_c, the control variable generated from op-amp2 is denoted as v_{con}. And the gain of op-amp2 is denoted as $G_k(s)$. By now, $G_k(s)$ is only set as a constant to amplify the difference between the inputs of op-amp2. The TWG has three input ports and one output port. Except for the control variable v_{con}, the input voltage and a fixed frequency CLK signal are introduced into the TWG. The TWG generates a ramp voltage signal where the slope is relevant to v_{con} and v_g. A slope adjustable triangular wave appears at the output port of TWG and is

connected to the negative terminal of comparator. Whether the input voltage is changed or the output voltage deviates from the reference signal, the triangular wave will be correspondingly regulated. Combining with the conventional VMC, it provides a better dynamic performance.

4.1.2 Triangular wave generator design

Fig. 4.3 shows the slope adjustable triangular wave generator.

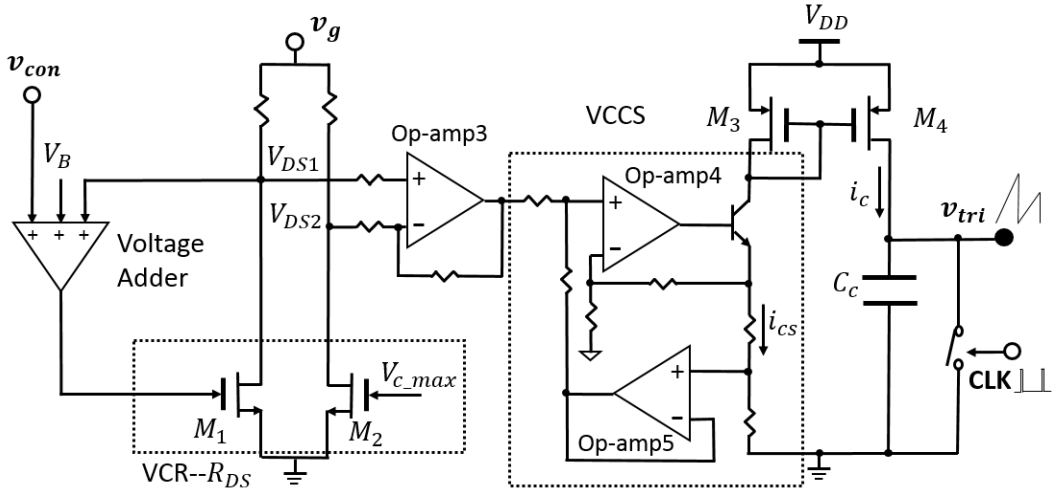


Fig. 4.3 Slope adjustable triangular wave generator

In this generator, two NMOS M_1 and M_2 are operated in triode region and used as voltage controller resistance (VCR)---R_{DS}. M_1 is controlled by the control variable v_{con}. Then these VCRs combine with a large constant resistance to divide the input voltage v_g. By this way, the drain voltage of NMOS is relevant to v_{con} and v_g, the variation in these two variations can be detected and expressed by V_{DS1}. Since the voltage V_{DS1} and its swing both are small, it is compared to V_{DS2} and the difference is amplified by op-amp3. V_{DS2} is similar to V_{DS1}, the difference is the M_2 controlled by a constant voltage. The output voltage of op-amp3 is transformed into current i_{CS} through a voltage controlled current source. The current i_{CS} is copied by a current mirror to generate i_C which charges the capacitor C_C. The capacitor is reset by CLK pulse signal every period. Finally, the voltage across the capacitor C_C is a triangular wave signal and the slope depends on v_g and v_{con}.

4.1.2.1 Voltage controller resistance

In triode region, the drain current of n-channel MOSFET transistor can be expressed as

$$I_D = K_n\left((V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right) \tag{4.4}$$

Where the transconductance parameter $K_n = \mu_n C_{ox} W/L$, μ_n is the mobility of the carrier, C_{ox} is the gate capacitance per-unit area. W is the effective channel width, L is the effective channel length, V_{th} is the threshold voltage of NMOS, V_{GS} and V_{DS} are the gate-to-source voltage and the drain-to-source voltage, respectively. The both sides of Eq. (4.4) are divided by V_{DS}, and the equation is rewritten as

$$\frac{I_D}{V_{DS}} = K_n\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right) \tag{4.5}$$

The drain current divided by the drain-to-source voltage can be seen as a reciprocal of resistance which connects the drain and the source. This equivalent resistance can be expressed as

$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{1}{K_n\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)} \tag{4.6}$$

We see from Eq. (4.6) that the resistance R_{DS} can be controlled by V_{GS}, but the component term $V_{DS}/2$ causes non-linear current/voltage relationship. This non-linear term should be eliminated. Therefore, to obtain a linear equivalent voltage controlled resistance, the gate-source voltage of NMOS transistor should be

$$V_{GS} = V_{th} + \frac{V_{DS}}{2} + V_{con} \tag{4.7}$$

The equivalent resistance R_{DS} can be rewritten as

$$R_{DS} = \frac{1}{K_n\left(\left(V_{th} + \frac{V_{DS}}{2} + V_{con}\right) - V_{th} - \frac{V_{DS}}{2}\right)} = \frac{1}{K_n V_{con}} \tag{4.8}$$

R_{DS} becomes linear, and only controlled by the control variable. To obtain a VCR as Eq. (4.8), a voltage adder is required. The voltage adder is realized by op-amp, as shown in Fig. 4.4

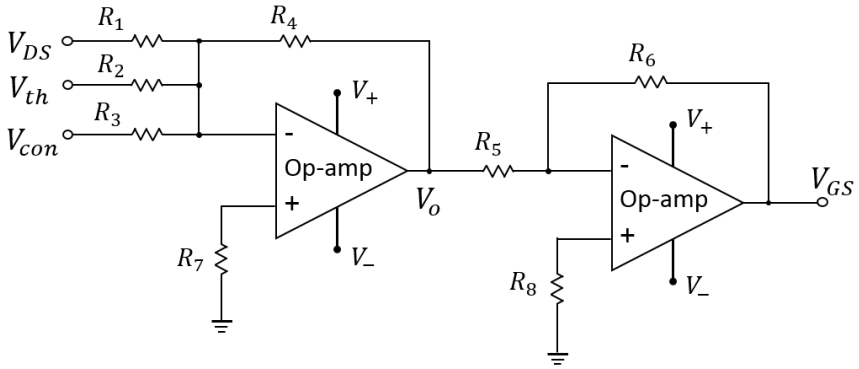


Fig. 4.4 voltage adder realized by operational amplifier

Set $R_1 = 20k\Omega$, $R_2 = R_3 = R_4 = R_5 = R_6 = 10k\Omega$ and $R_7 = R_8 = 1\text{k}\Omega$. From the left op-amp, we can get the relationship

$$\frac{-V_o}{R_4} = \frac{V_{DS}}{R_1} + \frac{V_{th}}{R_2} + \frac{V_{con}}{R_3} \quad \Longrightarrow \quad V_o = -(V_{DS}/2 + V_{th} + V_{con}) \tag{4.9}$$

The sum of $V_{DS}/2$, V_{th} and V_{con} is obtained at the op-amp output port, but the value is negative. The right op-amp is used to invert the voltage V_o. Finally, the voltage as expressed in Eq. (4.7) is obtained, and then this voltage drives the gate of NMOS transistor.

The obtained VCR is series with a resistance R_b to constitute a simple voltage divider for V_g. If R_b is far larger than the VCR R_{DS}, the drain voltage can be expressed as

$$V_{DS1} = \frac{R_{DS}}{R_b + R_{DS}} V_g \approx \frac{R_{DS}}{R_b} V_g = \frac{1}{R_b K_n} \cdot \frac{1}{V_{con}} \cdot V_g \tag{4.10}$$

Supposing an NMOS with $V_{th} = 0.9V$, $K_n \approx 1.4$, and $R_b = 1k\Omega$, V_g: 2V~7V, V_{con}: 10mV~5V. The curves of V_{DS}/V_{con} and V_{DS}/V_g are shown in Fig. 4.5

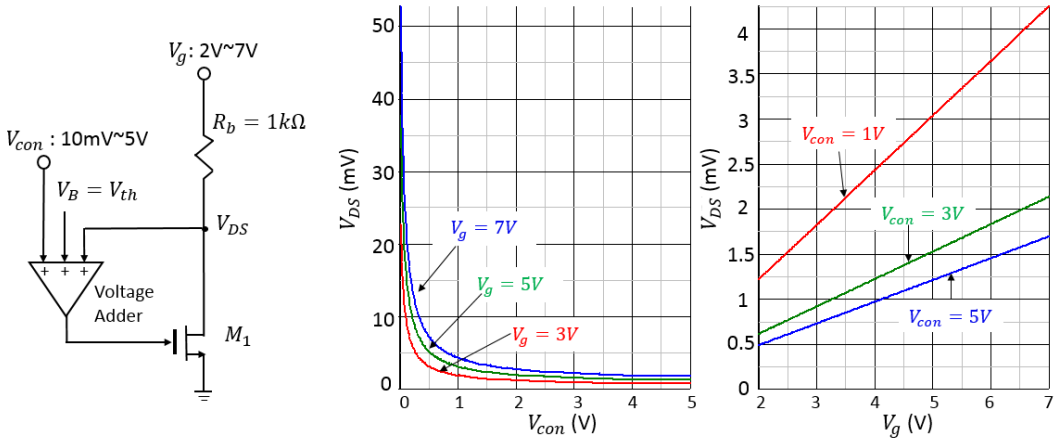


Fig. 4.5 Drain voltage with various V_g and V_{con}

The NMOS M_1 must be operated in triode region, which means that $V_{GS} - V_{th}$ must be larger than V_{DS}. Therefore, in order to get the mentioned linear VCR, the control variable V_{con} must satisfy

$$V_{con} > \frac{V_{DS}}{2} \tag{4.11}$$

Fortunately, V_{DS} is always very small, and then Eq. (4.11) condition is very easy to meet. However, because V_{DS} is too small to drive the following devices, it needs to be amplified. For larger dynamic range, the dc bias at the maximum V_{con} should be removed. A similar path is established in parallel with the circuit in Fig. 4.5. This path consists of identical R_b and NMOS transistor M_2, while the difference is the gate drive voltage of M_2 is constant. As shown in Fig. 4.3, the gate of M_2 is drive as follows

$$V_{c\_max} = V_{th} + \frac{V_{DS}}{2} + V_{con\_max} \tag{4.12}$$

Where V_{con_max} is the maximum value of control variable V_{con}. Therefore, M_2 can be seen as a constant resistance.

The difference between V_{DS1} and V_{DS2} is amplified by op-amp3 whose gain is denoted as $G_3(s)$. The output of op-amp3 can be expressed as

$$G_3(s)\Delta V_{DS} = \frac{G_3(s)V_g}{R_b K_n} \cdot \left(\frac{1}{V_{con}} - \frac{1}{V_{con\_max}} \right) \tag{4.13}$$

4.1.2.2 Voltage controlled current source

The voltage signal $G_3(s)\Delta V_{DS}$ is transformed into current by a voltage controlled current source (VCCS) which is shown in Fig. 4.6.

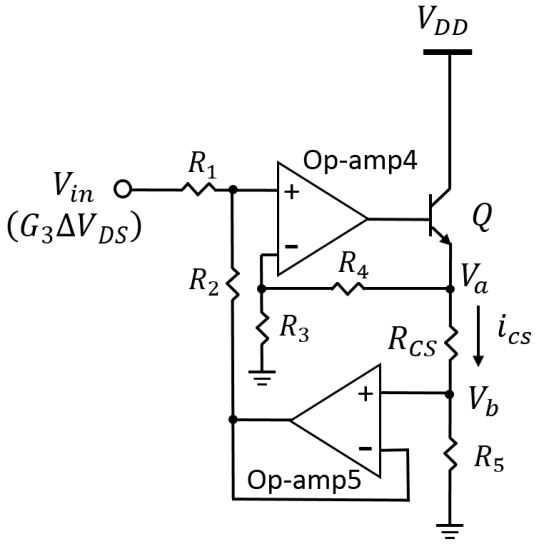


Fig. 4.6 Voltage controller current source transforms voltage signal $G_3\Delta V_{DS}$ into current signal i_{CS}

Set $R_1 = R_2 = R_3 = R_4 = 10k\Omega$, then the op-amp4 adds the input voltage, which is $G_3\Delta V_{DS}$ in this case, with the output of op-amp5 which buffers the voltage V_b. The voltage V_a equals to $(G_3\Delta V_{DS} + V_b)$. The applied voltage on the resistor R_{CS} is $(V_a - V_b)$, therefore, the current through R_{CS} will be

$$i_{CS} = \frac{(G_3\Delta V_{DS} + V_b) - V_b}{R_{CS}} = \frac{G_3\Delta V_{DS}}{R_{CS}} \tag{4.14}$$

If R_{CS} is a constant value with low thermal coefficient, the current i_{CS} can be seen as a linear function of the input voltage. Limited supply voltage V_{DD} causes a limited maximum i_{CS}. The transistor Q amplifies the output current of op-amp4, and can handle the maximum current when large i_{CS} increases V_b much.

4.1.2.3 Generate triangular wave

The VCCS current i_{CS} is copied by current mirror and $i_C = i_{CS}$ is obtained. The capacitor C_C is charged by i_C and reset by the fixed frequency CLK signal.

The voltage across C_C is given

$$V_{tri} = \frac{i_C}{C_C} \cdot t = \frac{i_{CS}}{C_C} \cdot t \tag{4.15}$$

Substituting Eqs. (4.13) and (4.14) into Eq. (4.15), we have

$$V_{tri} = \frac{G_3}{C_C R_{CS} R_b K_n} \cdot V_g \cdot \left(\frac{1}{V_{con}} - \frac{1}{V_{con\_max}} \right) \cdot t = M(V_g, V_{con}) \cdot t \tag{4.16}$$

The triangular wave is a voltage signal that increases with time. The slope is denote as $M(V_g, V_{con})$, and it is a function of V_g and V_{con}, proportional to V_g and inversely proportional to V_{con}.

4.1.3 Transient response improvement

4.1.3.1 Line feed-forward control

For a buck converter with conventional VMC, the transfer function from the error signal between the output voltage and the reference signal to the output voltage is given by

$$v = \frac{v_g}{V_p} \cdot \frac{G_c(s) v_e}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q_0 \omega_0} + 1} \tag{4.17}$$

Under the steady state, we have

$$\frac{V}{V_g} = \mathrm{D} = \frac{G_c(s) V_e}{V_p} \tag{4.18}$$

In conventional VMC, the triangular wave is fixed, and the variation in the input voltage only can be eliminated by the error signal. Of course, the output voltage will deviate from the reference signal. Until the error signal is regulated to the right value for the new duty cycle, the output voltage returns to the reference signal.

With the proposed slope adjustable TWG, the peak value of triangular wave is

directly related to V_g, and this relationship is proportional to

$$V_p = M(V_g, V_{con}) \cdot T_s = \frac{\left(\frac{1}{V_{con}} - \frac{1}{V_{con\_max}}\right) G_3 T_s}{C_C R_{CS} R_b K_n} \cdot V_g \tag{4.19}$$

Therefore, the variation in V_g is eliminated by V_p. This elimination happens as soon as V_g is changed, without need to wait to detect the variation in output voltage. This is line feed-forward control and the principle is similar to CMC.

4.1.3.2 Non-linear duty cycle modulation

In Fig. 4.1, we assume a constant control variable V_c to explain the effect of slope change. While, the proposed TWG establishes a relationship between the triangular wave slope and the variation in output voltage. Fig. 4.7 illustrates the duty cycle modulation with the proposed TWG, if the output voltage is changed.

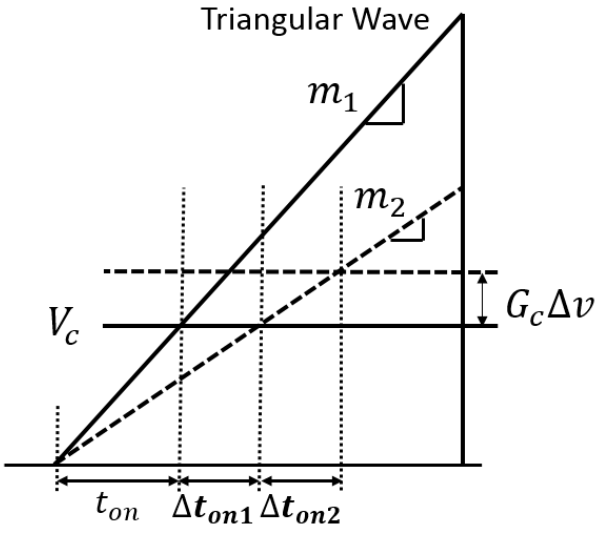


Fig. 4.7 Duty cycle modulation caused by the variation in output voltage

There are two elements which cause the variation in the duty cycle---the variation in the control variable V_c and the variation in the triangular wave slope. However, if we further explore the root causes of this duty cycle modulation, we can find only the reason that the output voltage deviates from the reference signal. The difference is that the control variable V_c is the output of op-amp1, while the

triangular wave slope is controlled by the output of op-amp2, in Fig. 4.2. These two op-amps have the same input---Δv.

From Fig. 4.7, we can separate the duty cycle modulation into two parts---$\Delta d_1 = \Delta t_{on1}/T_s$, caused by the changed slope; $\Delta d_2 = \Delta t_{on2}/T_s$, caused by the changed slope and the changed control variable V_c. They can respectively be expressed as

$$\Delta d_1 = \frac{V_C}{T_s} \cdot \left(\frac{1}{m_2} - \frac{1}{m_1}\right) = \frac{V_C}{T_s} \cdot \Delta\frac{1}{m} \tag{4.20a}$$

$$\Delta d_2 = \frac{G_c \Delta v}{T_s} \cdot \frac{1}{m_2} = \frac{G_c \Delta v}{T_s} \cdot \left(\frac{1}{m_1} + \Delta\frac{1}{m}\right) \tag{4.20b}$$

Supposing that m_1 is the triangular wave slope under steady state, and m_2 is the slope after the output voltage changing. Then the whole variation in the duty cycle is

$$\Delta d = \Delta d_1 + \Delta d_2 = \frac{V_C + G_c \Delta v}{T_s} \cdot \Delta\frac{1}{m} + \frac{G_c \Delta v}{V_{p\_ss}} \tag{4.21}$$

Where $V_{p\_ss} = m_1 T_s$, is the peak value of triangular wave under steady state. As we know, the second term---$G_c \Delta v / V_{p\_ss}$, just is the duty cycle modulation in conventional VMC. Now, besides this conventional modulation, we get an additional modulation effect---$((V_C + G_c \Delta v)/T_s) \cdot \Delta(1/m)$. Therefore, comparing to conventional VMC, the proposed TWG provides faster and stronger modulation to the duty cycle.

Substituting Eq. (4.16) into Eq. (4.21), and notice that V_{con} equals to V_{ref} under steady state and equals to $\left(V_{ref} - G_k \Delta v\right)$ during the transient response. Then duty cycle variation becomes a function of Δv

$$\Delta d(\Delta v) = \frac{(V_C + G_c \Delta v) G_k}{T_s \cdot a\left(b\left(V_{ref} - G_k \Delta v\right) - 1\right) \cdot \left(bV_{ref} - 1\right)} \Delta v + \frac{G_c \Delta v}{V_{p\_ss}} \tag{4.22}$$

Where

$$a = \frac{G_3 V_g}{C_C R_{CS} R_b K_n}, \qquad b = \frac{1}{V_{con\_max}}$$

We might still consider Eq. (4.22) as two parts, the first term in the right of equation is the additional modulation and the second term is the conventional

modulation. Moreover, the first term can be seen as Δv multiplied by a gain. The special place is that the gain depended on Δv itself, and can be expressed as

$$\mathrm{A}(\Delta v) = \frac{(V_C + G_c \Delta v) G_k}{T_s \cdot a\big(b\big(V_{ref} - G_k \Delta v\big) - 1\big) \cdot \big(bV_{ref} - 1\big)} \tag{4.23}$$

When Δv is large, this gain will also become large. Along with Δv decreasing, this gain will non-linearly decrease, and gradually tends to be a constant. Finally, when $\Delta v = 0$,

$$\mathrm{A}(0) = \frac{V_C G_k}{T_s \cdot a \cdot \big(bV_{ref} - 1\big)^2} \tag{4.24}$$

Now, Eq. (4.22) can be rewritten as a simplified form

$$\Delta d(\Delta v) = \mathrm{A}(\Delta v)\Delta v + \frac{G_c \Delta v}{V_{p\_ss}} \tag{4.25}$$

If the output voltage deviates largely from the reference signal, the loop gain becomes large, which enables fast transient response. If the output voltage is close to the reference signal, the loop gain becomes a constant, which is desirable for the loop stability. While, even if the loop gains decrease to constant, but the loop gain with proposed TWG is still larger than the conventional loop gain. It means that the crossover frequency should be pushed to a higher frequency, we can get wider band. This increase in loop gain bandwidth is not realized through op-amp1, so that, it is not limited by the GBP of op-amp.

Notice: unlike the line-feed-forward control which only can improve line transient response, the slope regulated by Δv can improve any transient response as long as the output voltage deviates from the reference. Including line transient response, although the line feed-forward control has already substantial improved the line transient response, there is still a small variation in the output voltage. While, the small variation can further be reduced by the proposed TWG.

4.2 STABILITY ANALYSIS

The additional duty cycle modulation makes the buck converter to timely respond to the variation in the output voltage. However, if this modulation is too large and strong, is it possible to cause instability? We need analyze the system stability after the proposed TWG is applied.

According to Eqs. (4.24) and (4.25), and supposing that the output voltage variation is very small, then the gain of additional duty cycle $A(\Delta v)$ can be approximated as the constant $A(0)$. The system block diagram is shown in Fig. 4.8

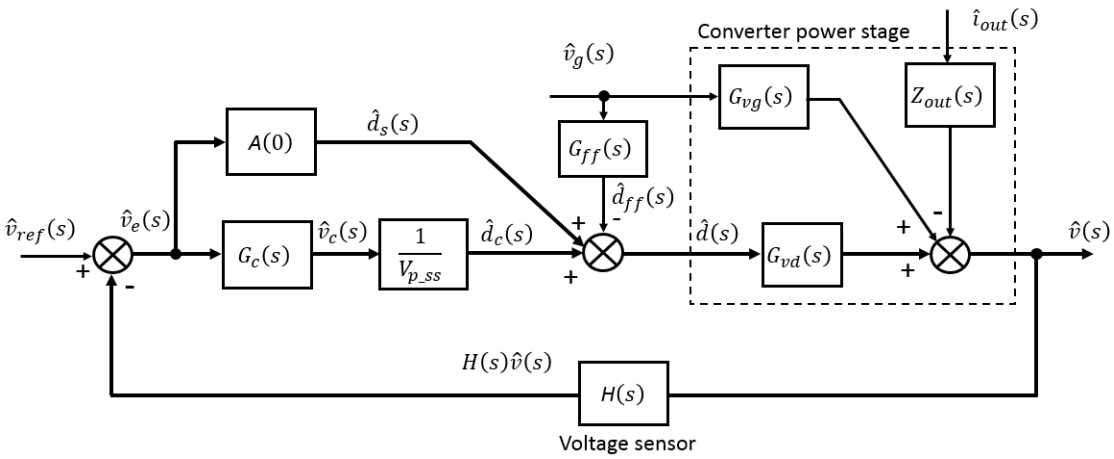


Fig. 4.8 System block diagram of buck converter with slope adjustable TWG

In this figure, $\hat{d}_c(s)$ is the duty cycle variation caused by the changed control variable $\hat{v}_c$, $\hat{d}_s(s)$ is the variation caused by the changed triangular wave slope, and $\hat{d}_{ff}(s)$ is caused by the input voltage variation through the line feed-forward path $G_{ff}(s)$ which is similar to CMC---$G_{ff}(s) = D/V_g$. The feedback loop gain can be expressed as

$$T(s) = \left(A(0) + \frac{G_c(s)}{V_{p\_ss}}\right) \cdot H(s) \cdot G_{vd}(s) \tag{4.26}$$

Eq. (4.26) also can be seen as the sum of two feedback loops as

$$T(s) = A(0) \cdot H(s) \cdot G_{vd}(s) + \frac{H(s)G_c(s)G_{vd}(s)}{V_{p\_ss}} \tag{4.27}$$

The example in Section 3.2.4 is utilized to analyze the system stability. Considering the GBP limitation and better dynamic performance, Type 3 compensator is designed for $50kHz$ ($f_s/20$) crossover frequency and 40° phase margin. The parameters of TWG are given by $G_{\mathrm{k}} = 100$ $G_3 = 200$, $C_C = 300pF$, $R_{CS} = 330\Omega$, $R_b = 1k\Omega$, $K_n \approx 2$, $V_{con\_max} = 1V$. Since V_c and V_{p_ss} are the control variable and the peak value of triangular wave under steady state, $V_c = 2.1V$ and $V_{p\_ss} = 3V$. With the known V_{g} and V_{ref}, $A(0)$ can be calculated, and the result is

$$A(0) \approx 6.65 \tag{4.28}$$

The Bode plot is sketched in Fig. 4.9

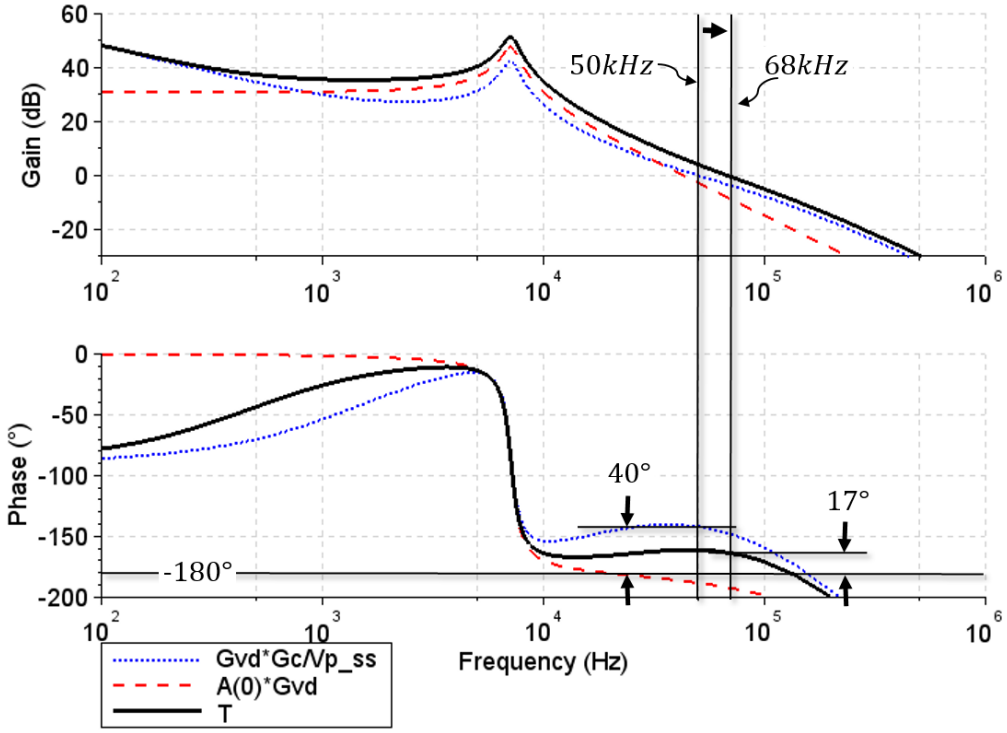


Fig. 4.9 Bode plot of buck converter with slope adjustable TWG

The loop gain is separated into two parts: $G_c(s)G_{vd}(s)/V_{p\_ss}$ ($H(s)$ is set as 1) is the loop gain before using the proposed TWG, its crossover frequency and phase margin are compensated at $50kHz$ and 40°; $A(0)G_{vd}(s)$ is the loop gain when only considering the slope modulation effect which has a lower crossover frequency than $50kHz$ with negative phase margin. Obviously, only considering $A(0)G_{vd}(s)$, it is unstable. But the sum of these two loop gains, as the black curve in Fig. 4.9, we can find that the crossover frequency is higher than $50kHz$. It is a

good phenomenon that wider band is obtained. However, the bad phenomenon is that although the phase margin is positive, it only has 17°. This system is stable in theory, but even if we neglect the other environmental factors that may reduce the phase, with this such small phase margin, there will be oscillation which occurs in the output during transient response and longer response time is required.

To better understand the relationship among the loop gain, $G_c(s)G_{vd}(s)/V_{p\_ss}$ and $A(0)G_{vd}(s)$, and trying to solve the problem of the small phase margin, Fig. 4.10 shows the Nyquist plot of these three loop gain. Only consider the part from $50kHz$ to $1MHz$.

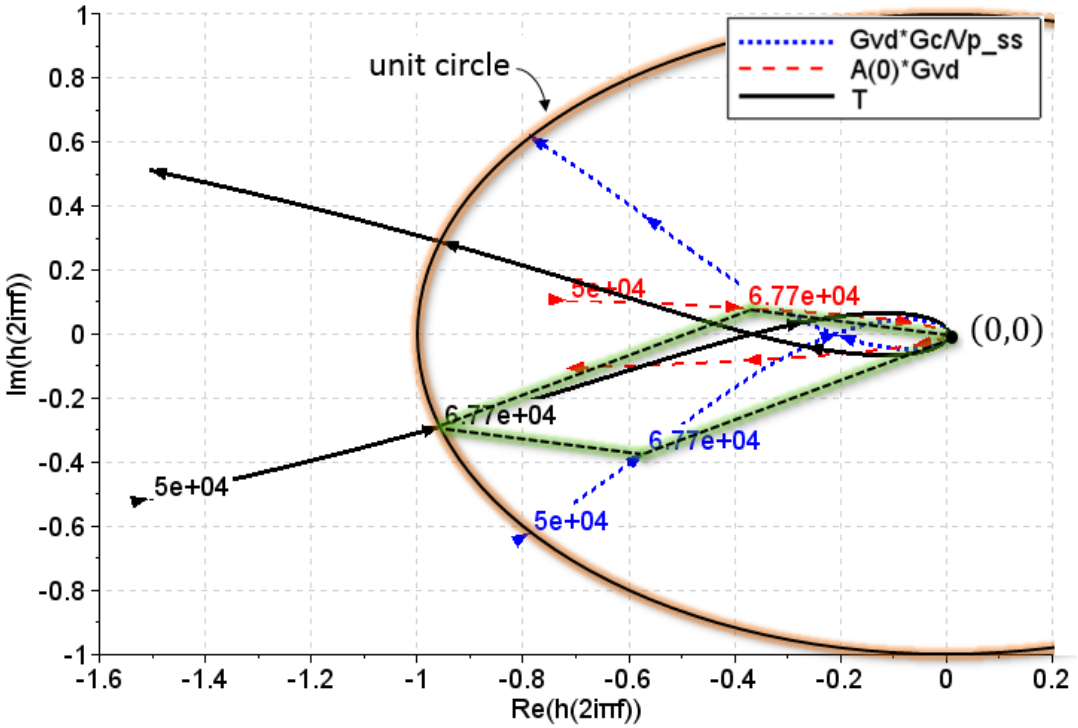


Fig. 4.10 Nyquist plot of buck converter with slope adjustable TWG

With a unit circle and a parallelogram, we can better understand the loop gain and the reason of small phase margin. There are two possible ways to increase the phase margin. Increasing the phase of $A(0)G_{vd}(s)$ or increasing the phase of $G_c(s)G_{vd}(s)/V_{p\_ss}$ at the frequency around $50kHz$. Fig. 4.11 shows these two ways. Although it is not an accurate expression for the loop gain, but we can roughly estimate the trend in loop gain.

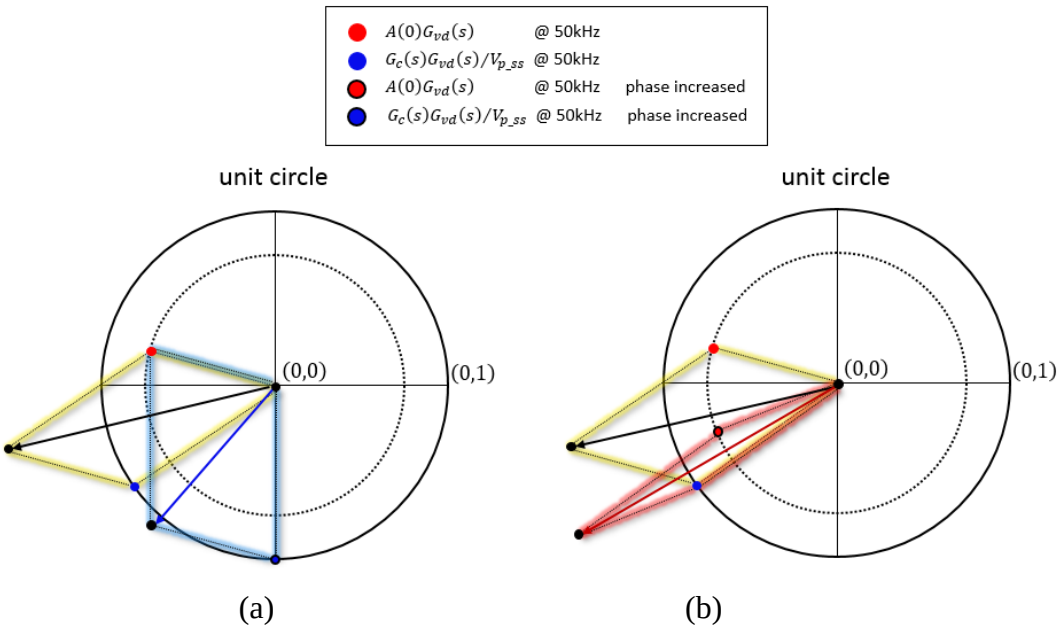


Fig. 4.11 Two ways to increase the phase margin of loop gain

(a) Increase of the phase of $G_c(s)G_{vd}(s)/V_{p\_ss}$

(b) Increase of the phase of $A(0)G_{vd}(s)$

Only from the perspective of geometry, if we increase the phase of $G_c(s)G_{vd}(s)/V_{p\_ss}$, as Fig. 4.11(a), the angle between the two vectors becomes large, the magnitude of the vector sum is reduced. In this example, although the crossover frequency still is higher than $50kHz$, but if it continues to increase the phase of $G_c(s)G_{vd}(s)/V_{p\_ss}$, the crossover frequency finally will be lower than $50kHz$. The other way, increasing the phase of $A(0)G_{vd}(s)$ causes the angle of the two vectors to become small. When the two vectors have the same phase, the magnitude of the sum is maximum. It means that a higher crossover frequency and an acceptable phase margin both are obtained.

Additional, for buck converter, it is difficult to compensate so much high-frequency phase of $G_c(s)G_{vd}(s)/V_{p\_ss}$, not to mention the GBP limitation should be considered. It is almost impossible. While, increasing the phase of $A(0)G_{vd}(s)$ is a simple and feasible solution. We can call it as the phase compensation of TWG.

By now, $A(\Delta v)$ only is a gain changed with Δv, it cannot change the loop phase in frequency domain. In order to increase the phase of $A(0)G_{vd}(s)$, we can insert a high-frequency zero in $A(\Delta v)$. In the proposed TWG, there are two components which can be utilized, the op-amp2 in Fig. 4.2 and the op-amp3 in Fig. 4.3. However, these two op-amps have been used to amplify the small signals,

so that their gains are large. Considering the GBP limitation of op-amp, they are not good choices. We can connect a new op-amp in series with op-amp3 and realize the high-frequency zero around the new op-amp, as shown in Fig. 4.12

The gain of op-amp6 is given by

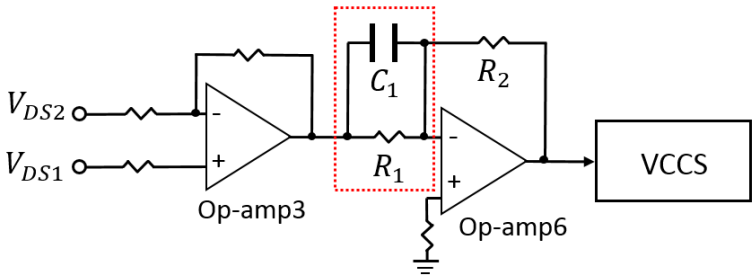
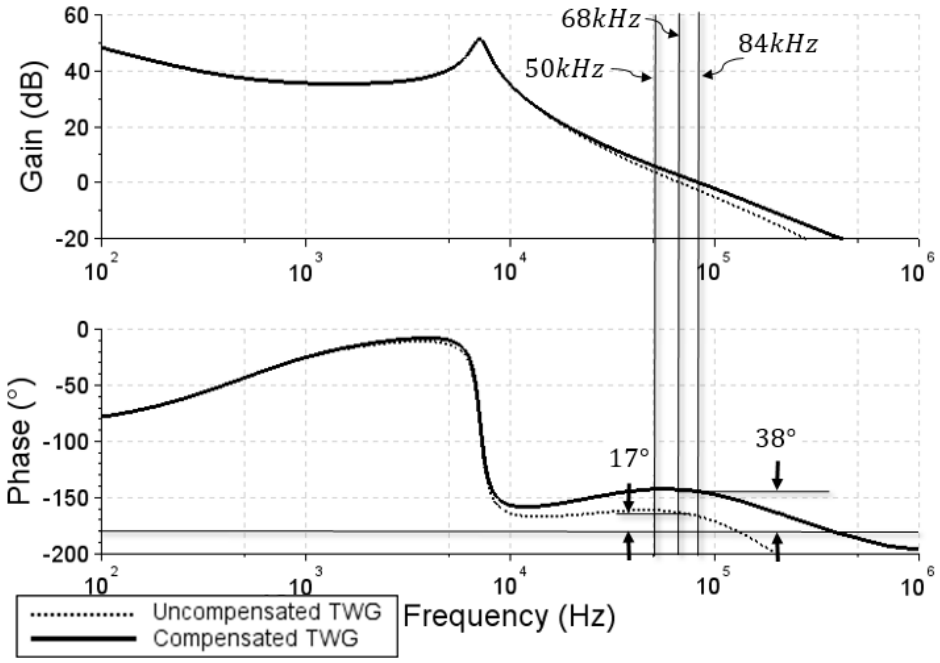


Fig. 4.12 Addition of high-frequency zero into the TWG

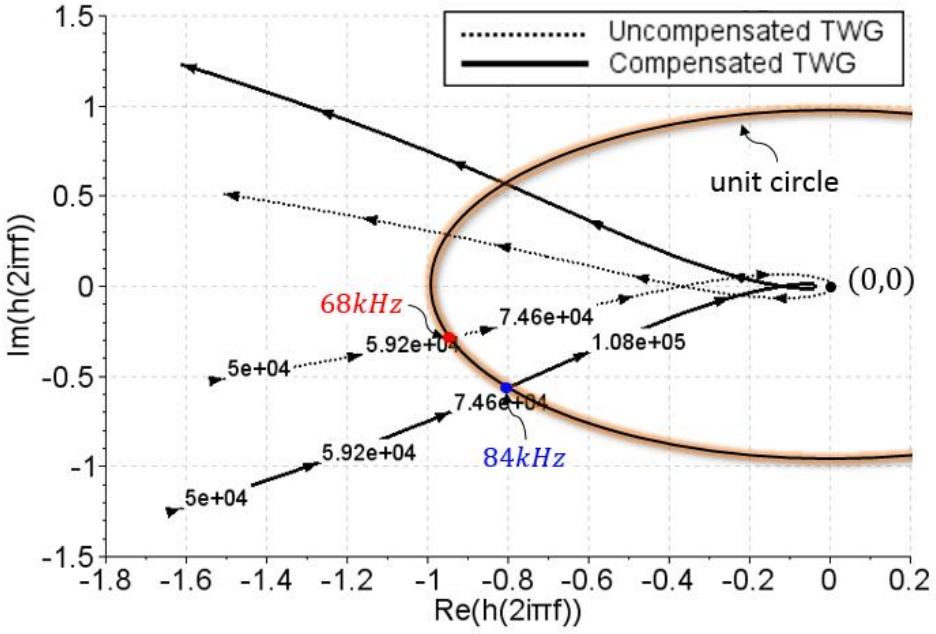
$$G_6(s) = \frac{R_2}{R_1}(C_1R_1s + 1) \tag{4.29}$$

The gain provides a zero at $\omega_{hz} = 1/C_1R_1$. With the setting of $R_1 = R_2 = 1k\Omega$, the zero will be placed at $50kHz$ for a $45°$ phase increasing of $A(0)G_{vd}(s)$ at the same frequency. By calculating, the value of C_1 is about $3.2nF$. The Bode plot and Nyquist plot of the buck converter with the phase compensated TWG are shown in Fig. 4.13. Comparing to the previous system, the compensated TWG not only provides an acceptable phase margin, about $38°$, but also further increases the crossover frequency to $84kHz$.

Now, the buck converter with compensated TWG is stable and has wider band. Since the wider band is not obtained by changing the design of Type 3 compensator, we do not need to worry about the GBP limitation of op-amp.



(a) Bode plot



(b) Nyquist plot

Fig. 4.13 Loop gain with phase compensated TWG

4.3 SIMULATION

SIMetrix simulation results will prove the feasibility of the proposed TWG. The line transient response and the load transient response of VMC buck converter are considered. Before showing the simulation results, let us review the simulation conditions, and the detail parameters are listed in Table. 4.1.

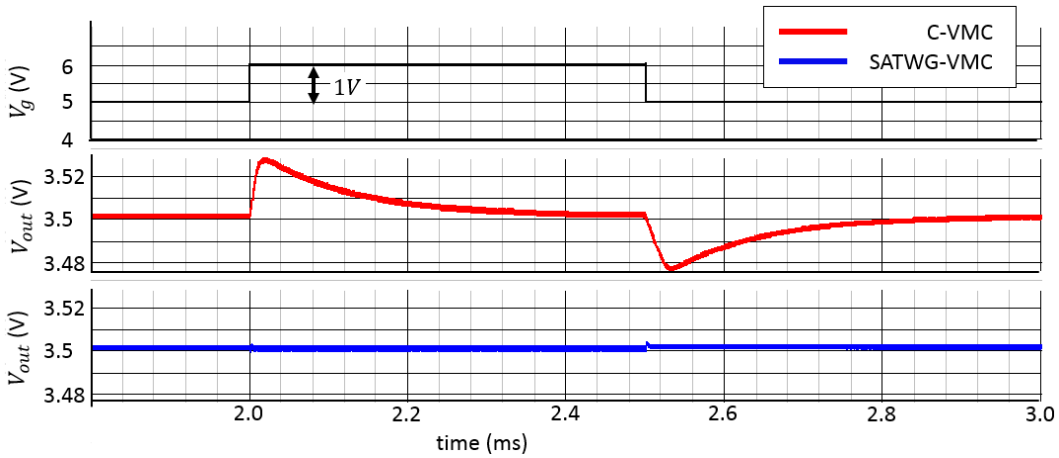
Table. 4.1 Simulation Conditions

Buck Converter	$V_g = 5V$	$V_{out} = 3.5V$	$V_{p\_ss} = 3V$
	$L = 10\mu H$	$C = 50\mu F$	$R = 35\Omega$
	$f_s = 1MHz$	$R_{ESR} = 2m\Omega$	$R' = 50m\Omega$
Type 3 Compensator	Compensation Goal	$f_c = \frac{f_s}{20} = 50kHz$	$\varphi_m = 40°$
	Error Amplifier Design	$G_{open\_loop} = 100k$	$GBP = 20MHz$
		$R_1 = 10k\Omega$ $R_2 = 9\Omega$	$R_3 = 10.6k\Omega$
		$C_1 = 180pF$ $C_2 = 11.2nF$	$C_3 = 647pF$
TWG	$G_k = 100$	$G_3 = 200$	$K_n \approx 2$
	$R_b = 1k\Omega$	$R_{CS} = 330\Omega$	$C_C = 300pF$
	$V_{th} = 0.9V$	$V_{con\_max} = 1V$	$\omega_{hz} = 2\pi \cdot 100kHz$

ω_{hz} is the zero which is used to compensate the phase of TWG.

4.3.1 Line transient response

First, supposing that the input voltage is stepwise changed between 5V and 6V, the variation is 1V. The simulation results will compare to conventional VMC as shown in Fig. 4.14.



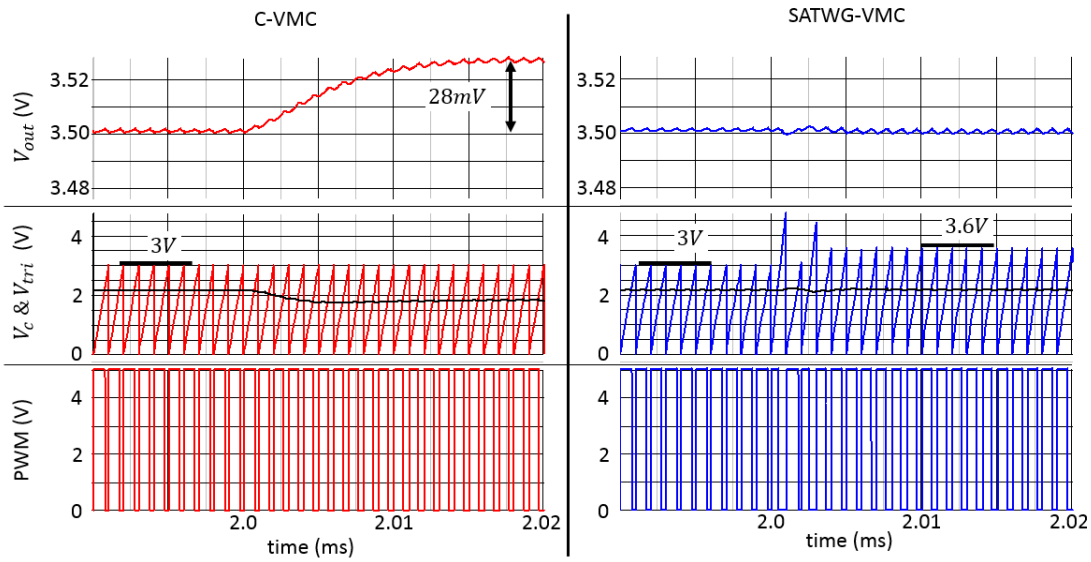
C-VMC: conventional voltage-mode control

SATWG-VMC: voltage-mode control with slope adjustable triangular wave generator

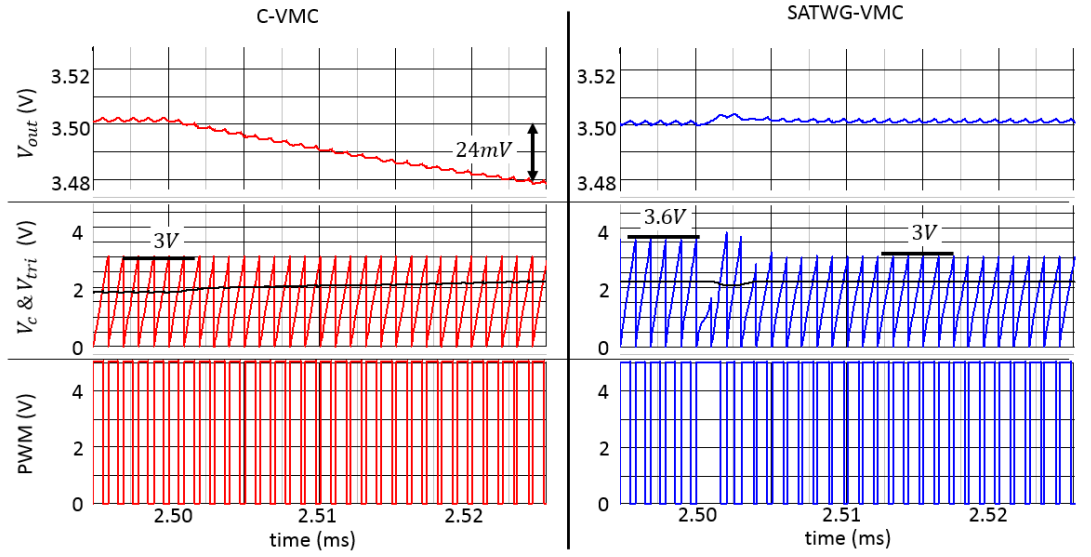
Fig. 4.14 Line transient response simulation, V_g: $5V \leftrightarrow 6V$

From the simulation results we can see that there are distinct overshoot and undershoot in the output voltage of buck converter with conventional VMC. When the input voltage increases from $5V$ to $6V$, the overshoot voltage is $28mV$, and response time is about $400\mu s$. When the input voltage decreases from $6V$ to $5V$, the undershoot voltage is $24mV$, and the response time is about $350\mu s$. While, with the proposed slope adjusatable triangular wave generator, the line transient response is improved by the line feed-forward control. Hence, there is not distinct change happened in the output voltage, whether the input voltage increases or decreases. The variation in the input voltage is eliminated by the changed triangular wave slope. The comparison of duty cycle modulation is shown in Fig. 4.15. With conventional VMC, the control variable V_c modulates the duty cycle, and there is variation appeared in the output voltage. The proposed method modulates the duty cycle by changing the triangular wave slope. Since the slope is proportional to the input voltage, the peak value of the triangular wave is also proportional to the input voltage. According to Eq. (4.18), the control variable V_c

can is constant, regardless of the input variation. It also means the output voltage keeps at the desired value.



(a) V_g: 5V → 6V

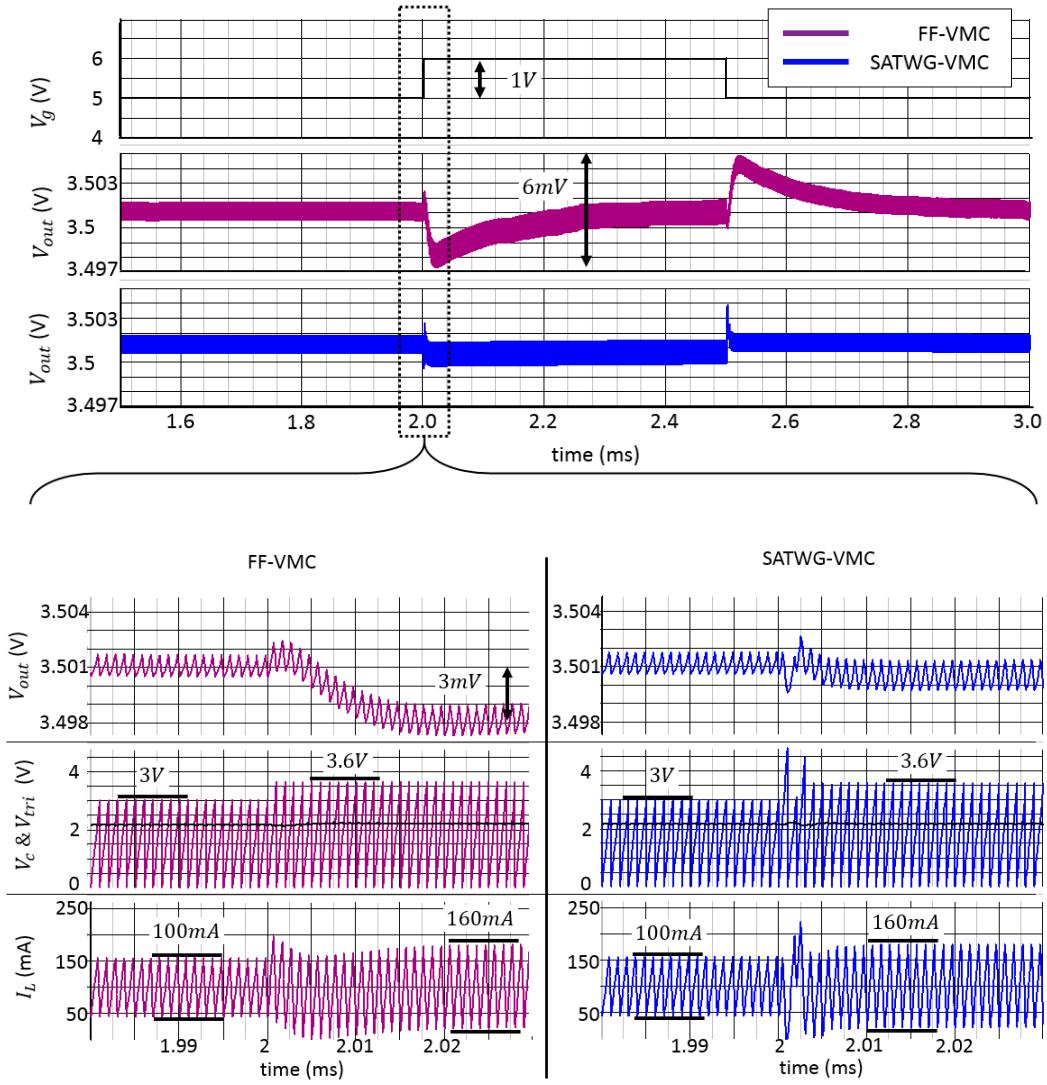


(b) V_g: 6V → 5V

Fig. 4.15 Duty cycle modulation during line transient response

We should notice that the peak value of triangular wave is not immediately regulated to the steady state after the input voltage changed. It is because the slope is also controlled by the variation in the output voltage, and this is the advantage of proposed method compared to the previous line feed-forward control in VMC. Considering an ideal conventional line feed-forward control, the

peak value is perfectly proportional to the input voltage immediately, but the peak value only depends on the input voltage. Comparing to this ideal conventional line feed-forward control, the simulation results are shown in Fig. 4.16



FF-VMC: voltage-mode control with conventional line feed-forward control

Fig. 4.16 Comparison between the proposed control scheme and the conventional line feed-forward control

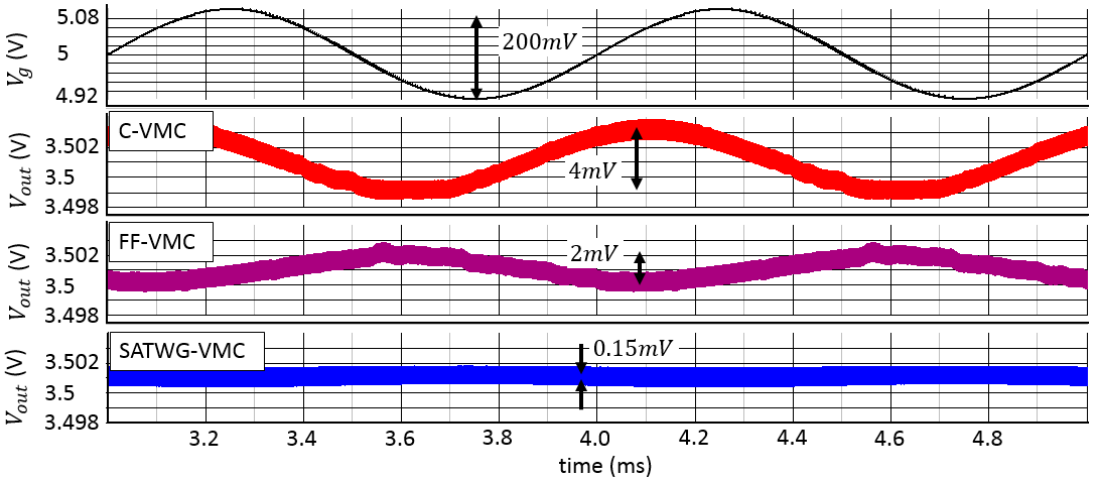
Although the line feed-forward control has improved the line transient response for VMC buck converter, the peak-to-peak variation is only $6mV$ (without line feed-forward control, it should be $52mV$), it is still larger than the buck converter with the proposed control method, and more response time is

required to reach the new steady state. The reason is that the inductor current ripple is also changed during line transient response. Before the inductor current ripple increases or decreases to the steady state, the inductor average current is not equal to the load current. This phenomenon is similar to load transient response, and the output voltage will deviate from the reference signal. As mentioned, the conventional line feed-forward control only concerns the variation in the input voltage. It can do nothing for the variation in the output voltage. However, the proposed method can detect the variation in the output voltage, and further regulate the slope based on the line feed-forward function. It makes the inductor current to reaches steady state rapidly, and the result is the negligible response time and output variation.

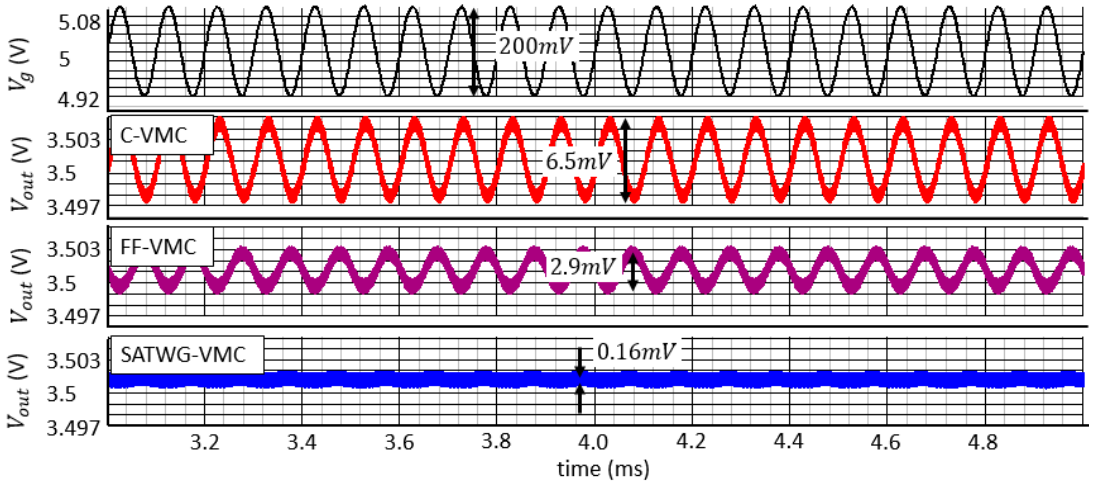
The other common variation in the input voltage is periodic change. Supposing an low-frequency AC component which is sinusoidal and has $200\text{m}V$ amplitude, but at different frequency, the output voltage comparisons of conventional VMC, VMC with line feed-forward control and VMC with the proposed TWG are shown in Fig. 4.17.

From the simulation results, we can see that the ac component of input voltage affects the output voltage. In conventional VMC buck converter, there should be an ac component which has the same frequency appearing in the output voltage. The amplitude of output ac component increases with the frequency. The conventional line feed-forward control can suppress the low-frequency ripple. For example, when the frequency of ac component is $10kHz$, line feed-forward control can decreases the output ripple from $6.5mV$ to $2.9mV$. However, it is still a distinct ripple. While, with the proposed TWG, the ripple is almost eliminated. In the twice simulations, the low-frequency ripples are neglectable $0.15mV$ only.

The conclusion is that the slope adjustable triangular wave generator can improve the line transient response of VMC buck converter, and the improvement is better than the conventional feed-forward control which only considers the input voltage variation.



(a)$V_g = 5 + \mathbf{0.1}\sin(2\pi \cdot \mathbf{1kHz} \cdot t)$



(b)$V_g = 5 + \mathbf{0.1}\sin(2\pi \cdot \mathbf{10kHz} \cdot t)$

Fig. 4.17 Periodic line transient responses

4.3.2 Load transient response

Supposing that the load current is stepwise changed between $100mV$ and $400mV$. Compareing to the conventional VMC, the simulation results are shown in Fig. 4.18.

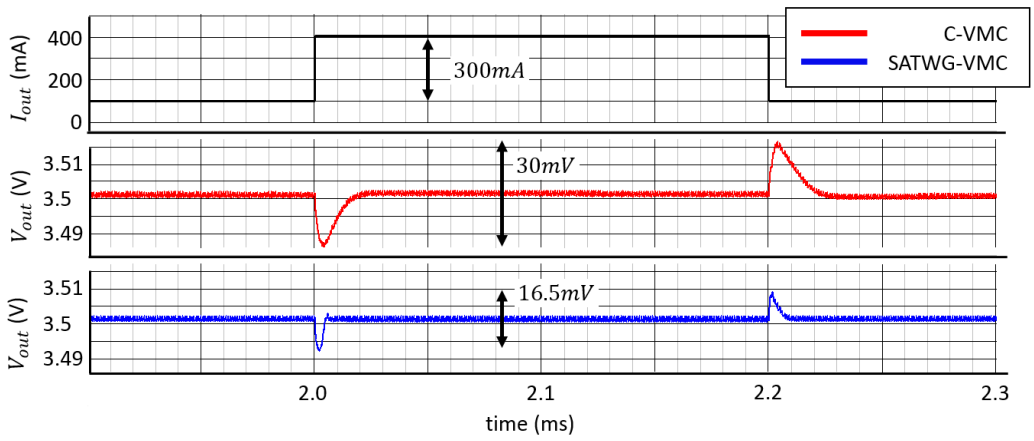
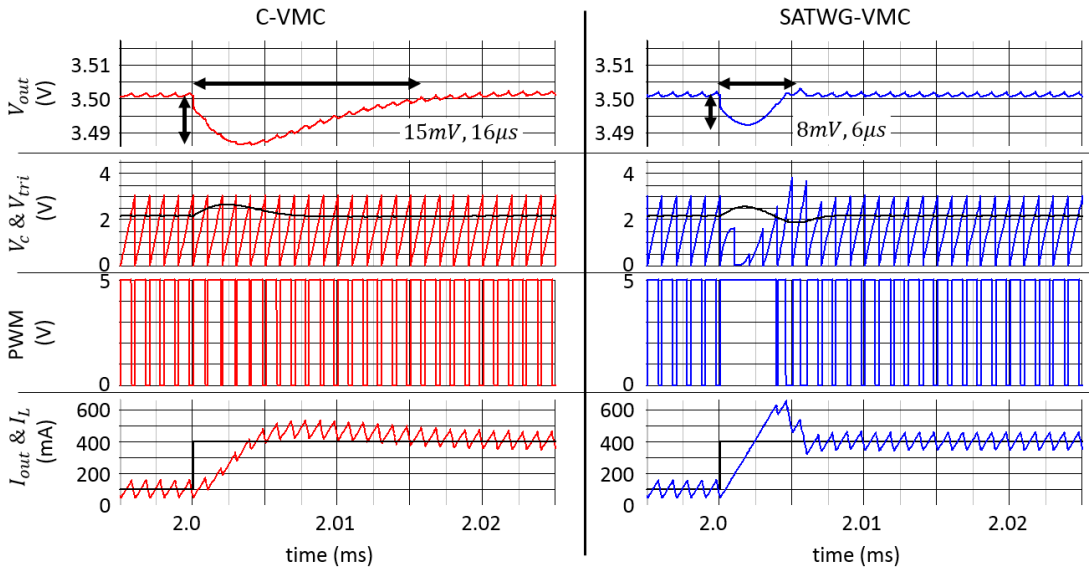


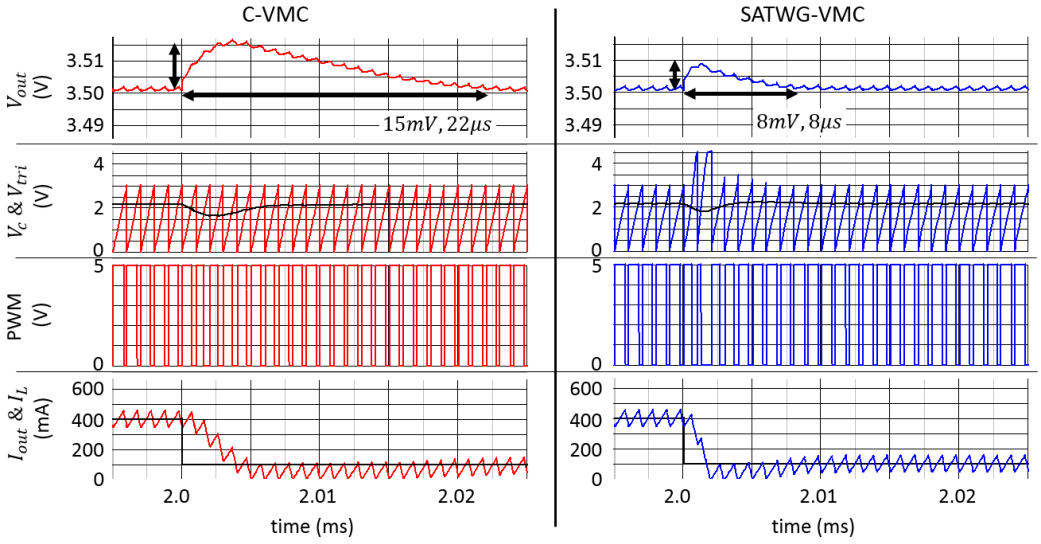
Fig. 4.18 Periodic line transient responses

The red curve in Fig. 4.18 is the output voltage of conventional VMC buck converter which has $50kHz$ bandwidth and $40°$ phase margin. During the load transient response, there are overshoot and undershoot in the output voltage and the peak-to-peak voltage is about $30mV$. The blue curve is the output voltage of VMC buck converter with the proposed TWG. There are also overshoot and undershoot phenomena occur, but the peak-to-peak voltage is $16.5mV$, smaller than the red curve, and the response time is shorter. More details at the moment when load current stepwise changed are shown in Fig. 4.19. The triangular wave, the control variable voltage V_c, the PWM signal and the inductor current are added to compare and analyze.

The conventional VMC modulates the duty cycle only through the changed control variable V_c. Although the V_c is increased when $V_{out} < V_{ref}$ to increase the inductor current I_L and is decreased when $V_{out} > V_{ref}$ to decrease I_L, the duty cycle modulation is not enough, the result is that I_L slowly increases or decreases, and then more overshoot and undershoot appear in V_{out}. It take a long time to make V_{out} to return V_{ref}.



(a) I_{out}: 100mA → 400mA



(b) I_{out}: 400mA → 100mA

Fig. 4.19 Duty cycle modulation during load transient response

The control variable V_c in the proposed method is also regulated corresponding to duty cycle modulation, at the same time the triangular wave is also regulated for the same purpose. The duty cycle gets more modulation, I_L rapidly increases or decreases. In this simulation, after I_{out} increasing from 100mA to 400mA, the duty cycle is increased to 100% during 4 periods. This makes I_L to keep rising and reach the level of changed I_{out} as soon as possible. Since the peak values of overshoot and undershoot depend on the load current variation, the ESR of output capacitor and the time how long I_L takes to reach

the new I_{out}, the relationships are as shown in Fig. 4.20. Once the parameters of buck converter have been decided, in order to reduce the overshoot and undershoot, the control system should try to maximize or minimize the duty cycle before the inductor current crosses the changed load current. For the blue curves in Fig. 4.19(a), the duty cycle always is 100% before $I_L \geq I_{out}$, therefore, $8mV$ is the minimum undershoot theoretically. For the blue curves in Fig. 4.19(b), the duty cycle cannot decrease to 0% due to the unrealistic infinity slope. However, the inductor current decreases still much faster than the red curve and smaller overshoot voltage is obtained.

Although it seems that the triangular wave modulation is too intense when V_{out} deviates far away from V_{ref}, as V_{out} gradually approaches V_{ref}, the triangular wave can timely retrun to its stead state, and the system is stable.

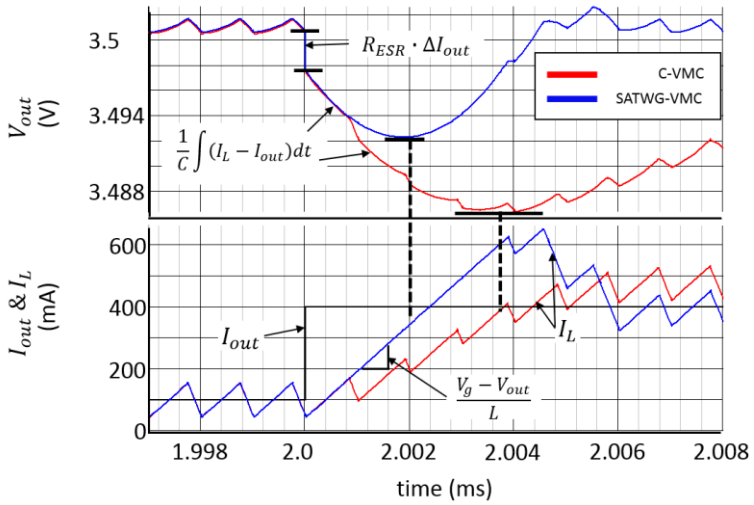


Fig. 4.20 Determination of undershoot and overshoot

As mentioned, the VMC buck converter with the proposed TWG has wider band, even though the Type 3 compensator is designed for only $50kHz$ bandwidth since the GBP limitation of op-amp. Now, let us consider a wideband op-amp, for example, the GBP is $1GHz$. Comparing to the op-amp that is utilized in the proposed method, the parameter setting of op-amps is shown in Fig. 4.21. For the buck converter with $1MHz$ switching frequency, the dreamy op-amp allows the Type 3 compensator is designed for $200kHz$, also is fifth switching frequency. Designing compensator for conventional VMC buck converter, the crossover frequencies are set at $f_s/20$, $f_s/10$ and $f_s/5$ respectively and the phase marigns are all 50°. The Bode plots of compensator gains and loop gains are

shown in Fig. 4.22

The load transient response of these three buck converters are simulated, the load current is still stepwise changed between $100mV$ and $400mV$, and then compared to the simulation result which is gotten through the proposed method. The comparison result is shown in Fig. 4.23

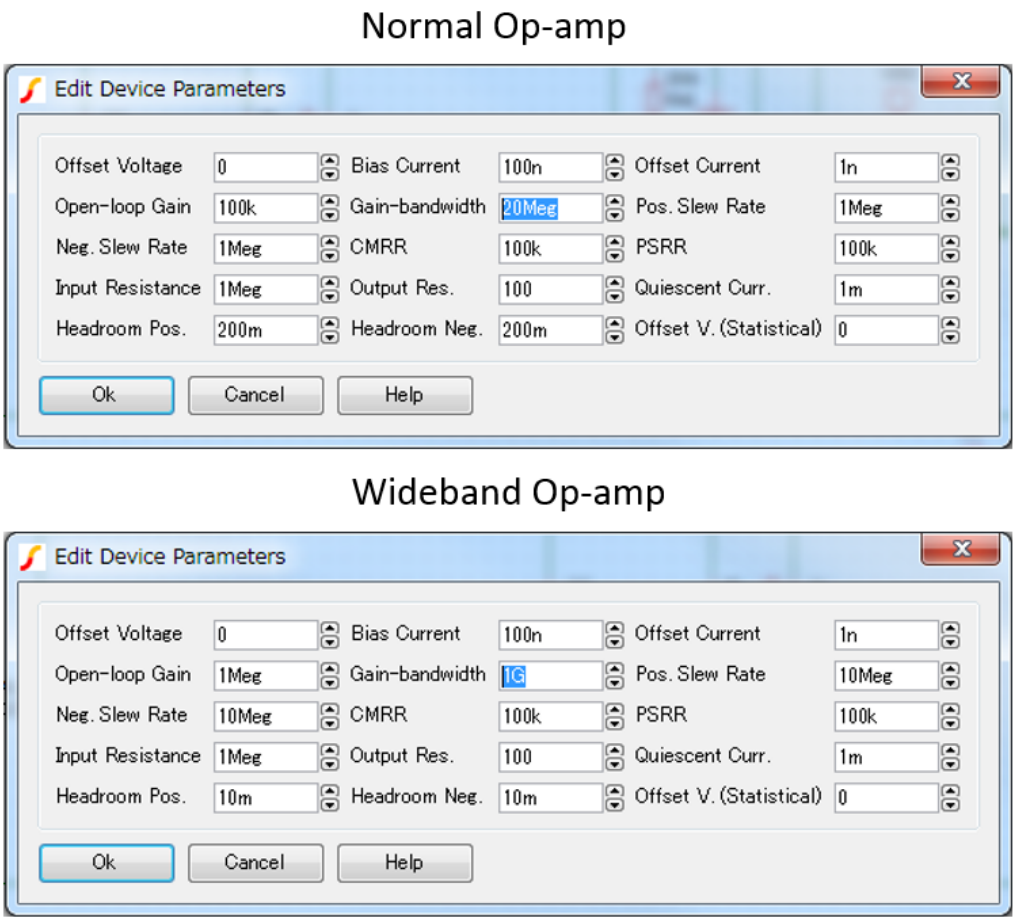
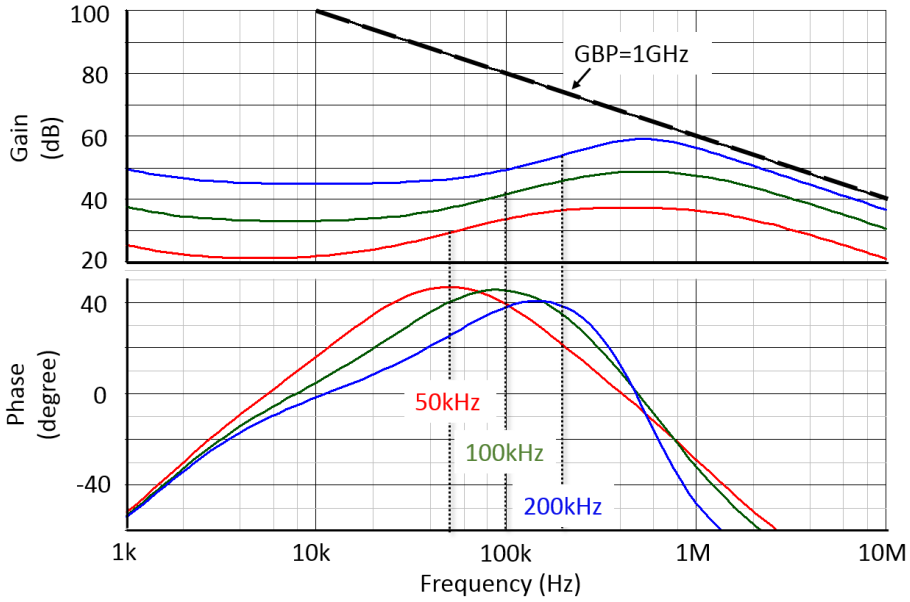
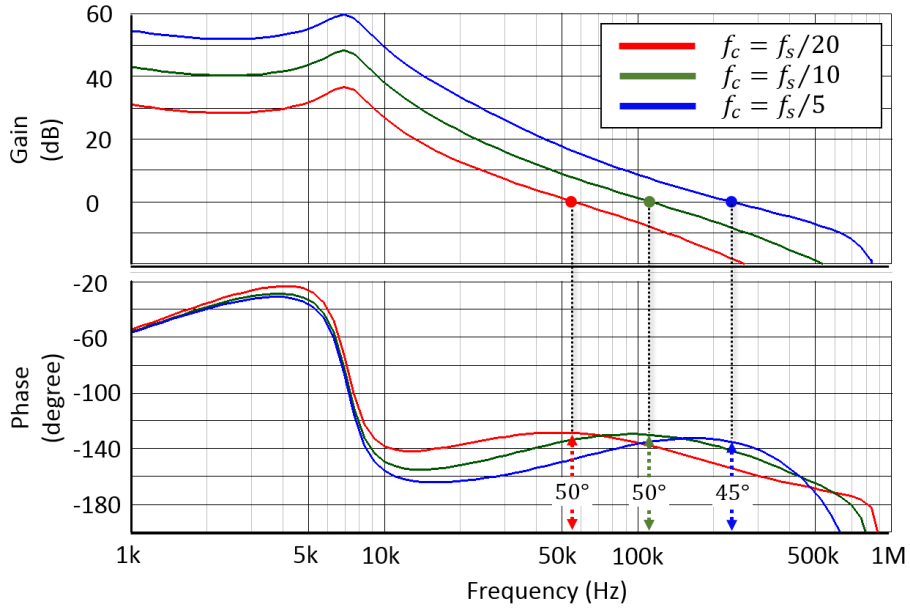


Fig. 4.21 Parameter setting of normal op-amp and wideband op-amp



(a) Type 3 compensator gain



(b) Loop gain

Fig. 4.22 Gain of compensator and loop realized by wideband op-amp

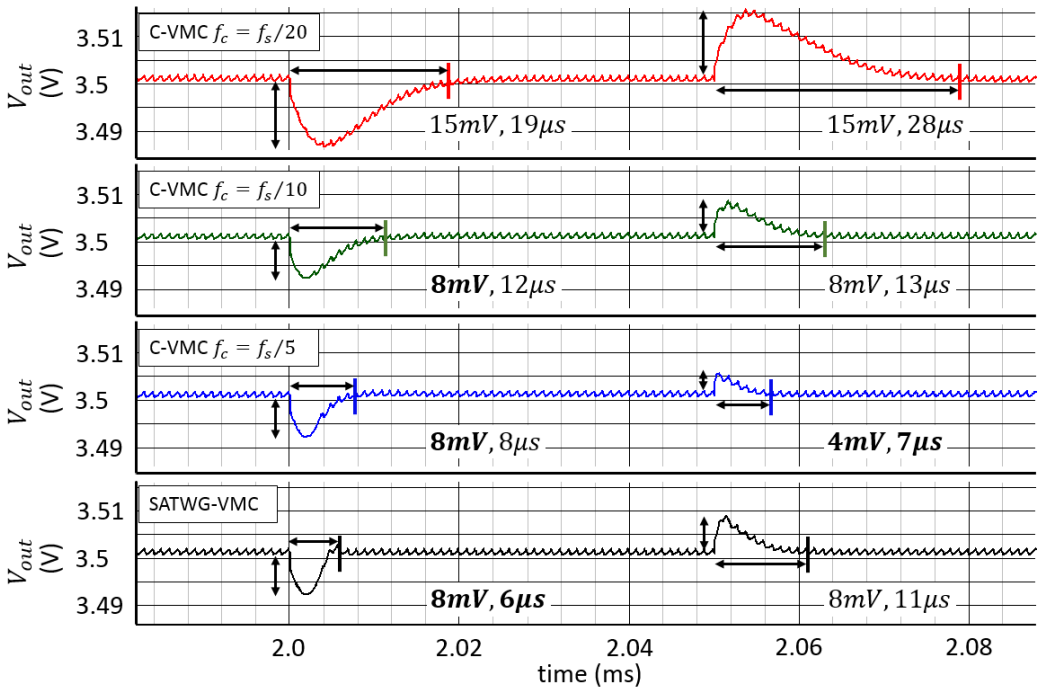
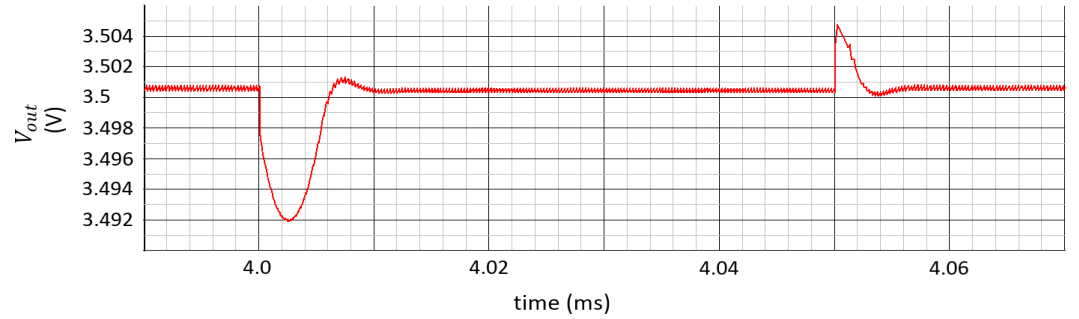


Fig. 4.23 Comparing to wideband buck converter with conventional VMC

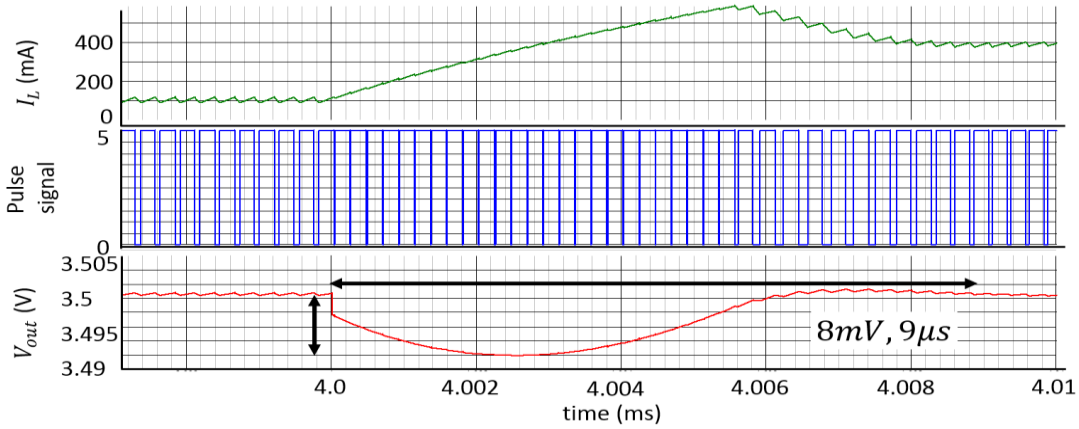
From these four times simulations, we can see that when the load current increases from $100mV$ to $400mV$, the buck converter whose crossover frequency is $f_s/10$ ($f_s/10$ buck converter for short), the $f_s/5$ buck converter and the SATWG buck converter have the minimum undershoot, $8mV$. But the SATWG buck is the fastest one that returns to reference signal, where the response time takes only $6\mu s$. While, in the case that load current decreases from $400mV$ to $100mV$, the $f_s/5$ buck converter has the minimum overshoot and the shortest response time, $4mV$ takes $7\mu s$. After it, the SATWG buck converter and the $f_s/10$ buck converter have almost the same overshoot voltage, $8mV$. However, the SATWG buck vonerter is faster than the $f_s/10$ buck. If ranking their performance of load transient response, in the current step-down case, the SATWG buck converter is the best; in the current step-up case, it is the second-best. Hence, we can know that the SATWG buck converter gets a comparable load transient response to the buck converter which has $f_s/5$ bandwidth. However, only a normal op-amp is required in the propose method.

The next comparison is between the proposed control method and the hysteretic control. The improved hysteretic control topology in reference [26] is introduced in Chapter Ⅱ, and the system configuration is shown in Fig. 2.34. The

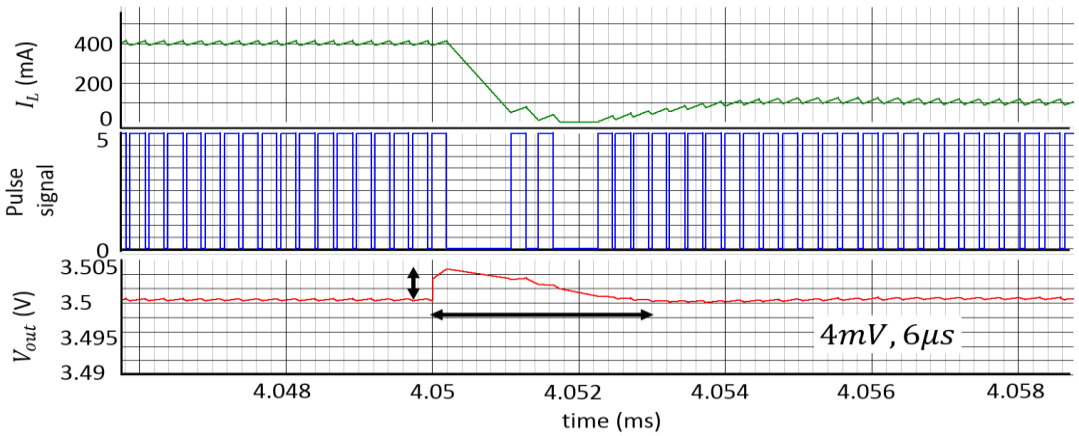
parameters of buck converter are the same as Table 4.1, and the other parameters are set as $R_f = 500k\Omega$, $C_f = 2nF$, $C_b = 1nF$, the fixed ON-time $T_{on} = 200ns$ and the minimum off time $T_{off\_min} = 1ns$. The load current also stepwise changes between 100mA and 400mA, the simulation result is shown in Fig. 4.24.



(a) I_{out}: $100mA \leftrightarrow 400mA$



(b) I_{out}: $100mA \rightarrow 400mA$



(c) I_{out}: $400mA \rightarrow 100mA$

Fig. 4.24 Load transient response of buck converter with hysteretic control

When the load current increases, the under-shoot voltage is 8mV and response time is $9\mu s$. It is nearly the same with the proposed triangular wave slope modulation (8mV, $6\mu s$). When the load current decreases, the load transient response is 4mV with $6\mu s$, is faster than the proposed method (8mV, $11\mu s$). The switching frequency of hysteretic control with fixed ON-time is almost constant under steady state. In this case, the frequency is about 3.5MHz. But during the transient response, the switching frequency variation range becomes larger. The variation range is 3.1~5MHz when the load current increases, and is 1~3.8MHz. However, the proposed method is based on voltage-mode control, the switching frequency always keeps at constant.

4.3.3 Summary

In this section, SIMetrix simulations are used to prove the effective of proposed slope adjustable triangular wave generator for improving the dynamic performance of dc-dc buck converter.

For line transient response, since the triangular wave slope is proportional to the input voltage, the proposed TWG provides a line feed-forward control function for VMC buck converter. Not only that, the slope regulation also depends on the variation in the output voltage. Unlike the conventional line feed-forward control, the output variation that is caused by the changed inductor current ripple is also considered, and then the further improvement of the line transient response is obtained. With the proposed method, We almost cannot find the output variation during line transient response.

For load transient response, an additional duty cycle modulation that is caused by the changed slope is added to the conventional duty cycle modulation that only depends on the control variable V_c. When the ouput voltage deviates far away from the reference signal, the effect of additional duty cycle modulation is large, which enables fast transient response; when the output voltage close to the reference, the effect becomes small, which is desirable for system stability. The load transient response of the proposed method is comparable with the buck converter that has a very wide band. As we know, the wideband buck converter requires an expensive wideband op-amp. While, the requirement of the proposed method is only a normal op-amp for low gain Type 3 compensator. It is cost-efficient and easy to realize.

Speaking of simple and fast switching converter control topology, the hysteretic control seems to be the best choice. However, the proposed triangular wave slope modulation can get comparable result to hysteretic control. Although hysteretic control is simpler, the advantage of the proposed method is keeping constant switching frequency, whether it is under steady state or during transient response.

CHAPTER V
SINGLE-INDUCTOR DUAL-OUTPUT BUCK CONVERTER

5.1 INTRODUCTION

In a portable device, some different DC supply voltages are required for different function modules. Multiple-supply implementations are required for getting high performance and reducing power loss. Among existing techniques, single-inductor dual-output (SIDO) switching converters are cost-effective solution. In SIDO converter, two outputs share a unique off-chip inductor that helps reducing system volume and saving chip area [31-34]. However, the converters are independently regulated if they work at CCM, which leads to cross-regulation problem: if the load of one sub-converter changes, the output voltage of the other sub-converter is affected.

In recent years, some techniques of improving cross-regulation have been proposed. The reference [35] employs time multiplexing control. Sub-converters are isolated by a zero current period. However, this converter has large current ripple, especially when the load is heavy. Since the inductor current should be zero at the end of each period, a pseudo-continuous conduction mode is proposed in the reference [36]. This mode integrates the advantages of both CCM and DCM. When the load is light, the converter works at DCM. When load increases, a freewheel switching control keeps the inductor current above zero as CCM, but sub-converters are isolated by a DC current. However if the load is large enough, the converter may turn to CCM.

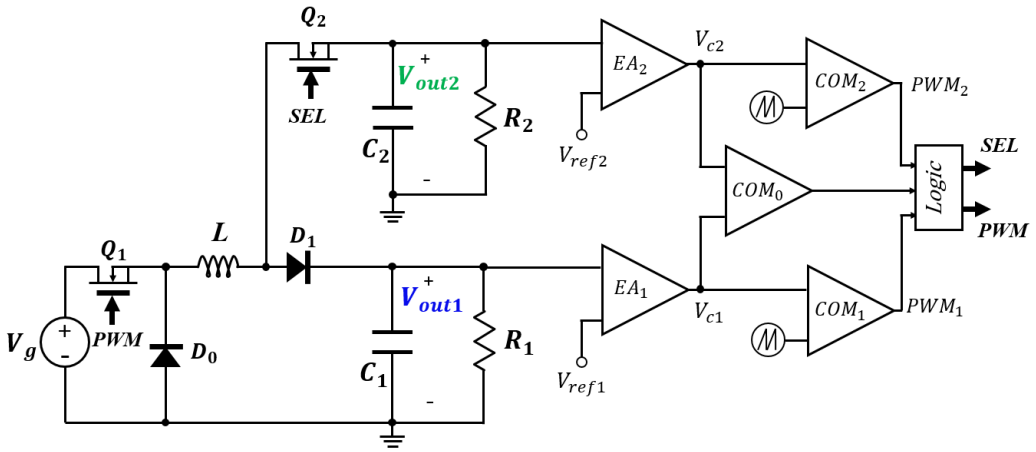
Essentially, the cross-regulation problem is caused by load transient response. Therefore, a fundamental solution to the cross-regulation is to improve load

transient response for each sub-converters. The proposed slope adjustable triangular wave generator is utilized for a simple-yet-effective SIDO buck converter with exclusive control [37] in this chapter.

5.2 SIDO BUCK CONVERTER WITH EXCLUSIVE CONTROL

5.2.1 Configuration and principle

The SIDO buck converter with exclusive control is shown in Fig. 5.1

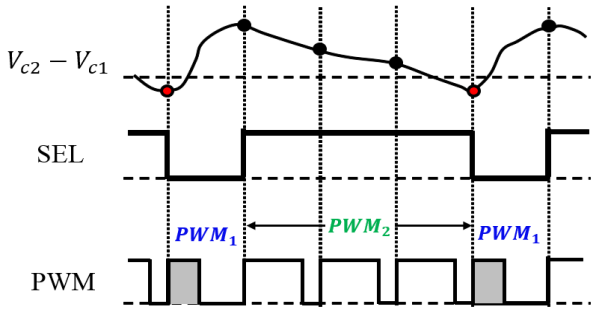


EA---error amplifier COM---comparator

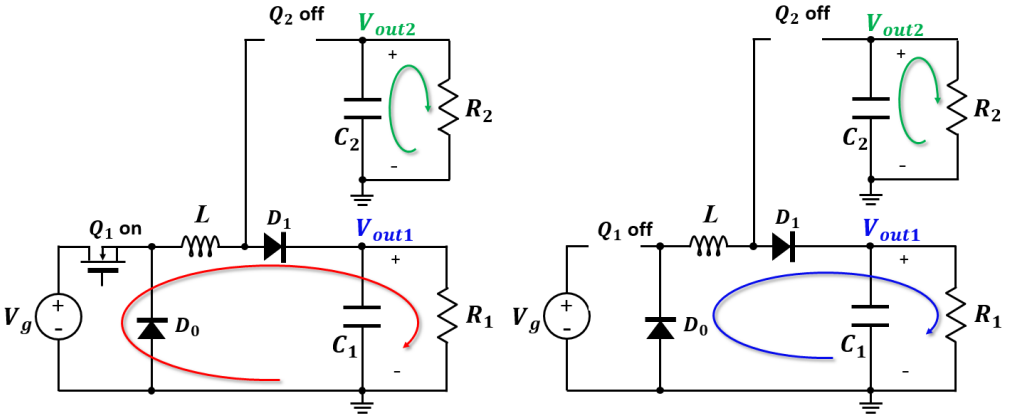
Fig. 5.1 SIDO buck converter with exclusive control

The two output voltages are compared to respective reference signal on the error amplifiers and generate control variables V_{c1} and V_{c2}. Similar to single-inductor single-output (SISO) buck converter, the control variables are compared with triangular wave to get PWM signal, where PWM signal is used to drive the switch Q_1 depends on the comparison between the two control variables. The state of switch Q_2 also depends on this comparison. If $V_{c1} > V_{c2}$, it means the deviation of V_{out1} is larger than V_{out2}, and sub-converter 1 requires to be served.

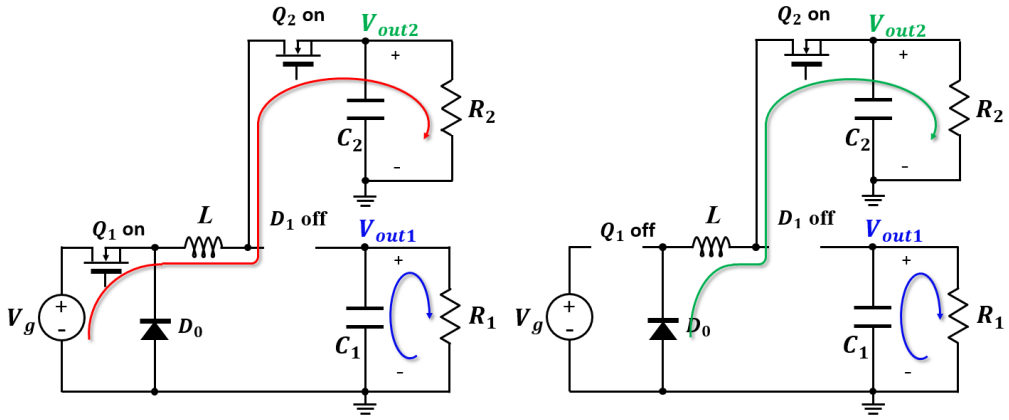
This time, a select signal---SEL is low, Q_2 turns off and PWM_1 drives Q_1 until the start of next period. Sub-converter 1 takes the power from input alone during this period. Whereas, if $V_{c1} < V_{c2}$, the SEL signla is high, Q_2 turns on and PWM_2 drives Q_1. Since the output voltages are set as $V_{out1} > V_{out2}$, when Q_2 turns on, the diode D_1 reverse bias. Sub-converter 2 takes all of the power from input



(a) Timing chart



(b) $V_{c1} > V_{c2}$



(c) $V_{c1} < V_{c2}$

Fig. 5.2 Timing chart and circuit states

alone. The timing chart and the circuit states are shown in Fig. 5.2

5.2.2 SEL switching frequency

The comparison of two control variables determines the state of SEL signal that decides which sub-converter should be served. Let us consider a SIDO buck converter without phase compensation. The error amplifier only provides a dc gain. Then the control variables are proportional to the deviation of output voltage. It means that the rate of control variable change depends on the load current, because

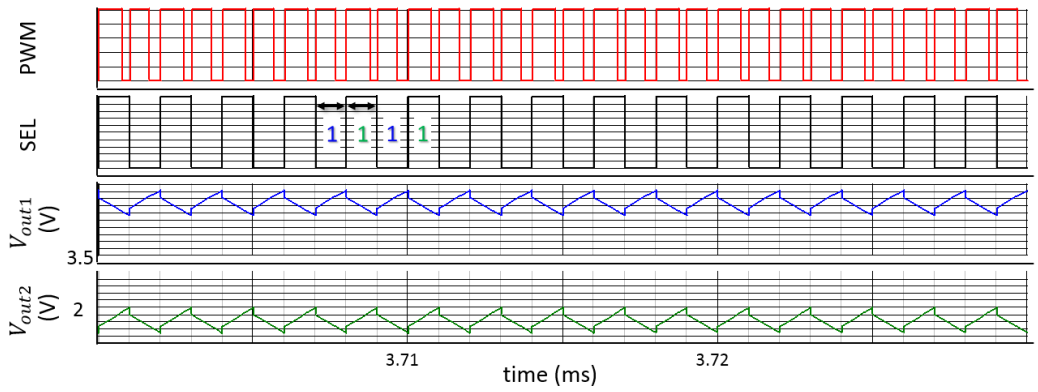
$$\Delta V_c = K\Delta V_{out} = \frac{I_{out}}{C}\Delta t \tag{5.1}$$

Where K is the DC gain of the error amplifier.

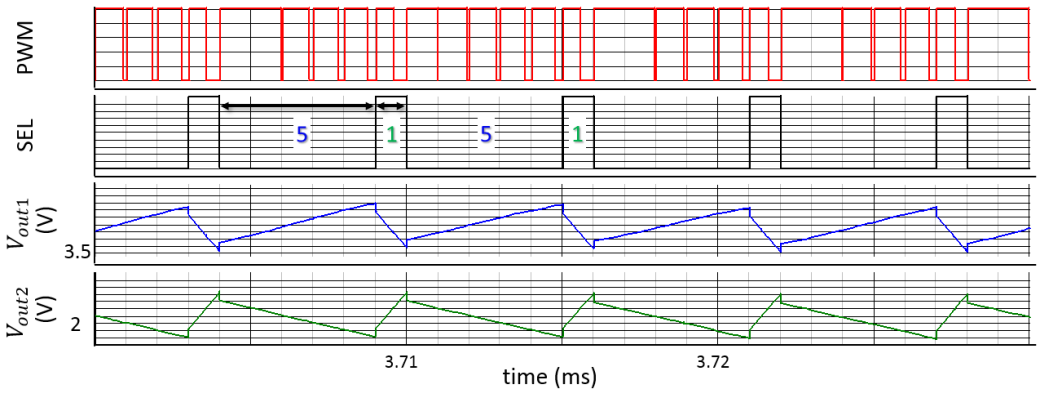
Therefore, the served interval of each sub-converter depends on the ratio of their load currents. If this load current ratio is small, for example, the load currents are the same, the served interval may be only one period. If the load current ratio is large, the light load sub-converter must wait for several periods before it is served by the inductor.

In Fig. 5.3, a SIDO buck converter which has 5V input voltage and two output voltages 3.5V and 2V as an example are used to show the relationship between the load currents ratio and the SEL signal. The error amplifiers provide only a DC gain. From Fig. 5.3, we can see that the inductor occupancy rate of each sub-converter is proportional to their load current ratio.

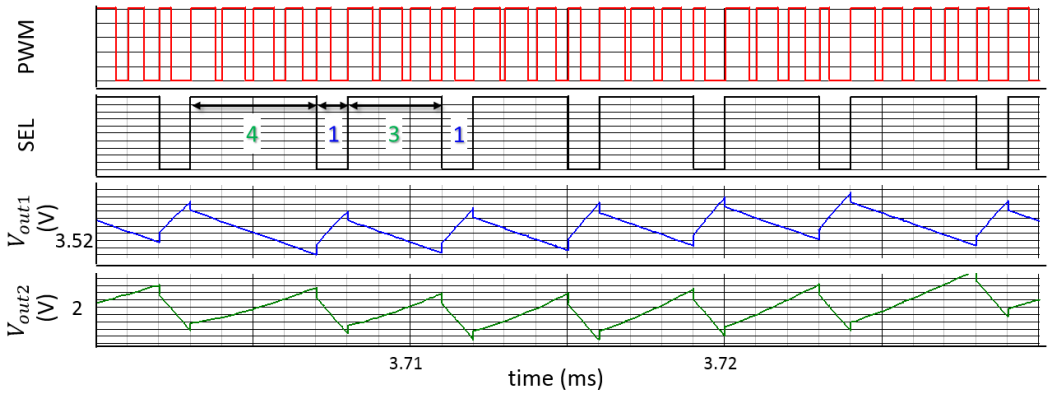
The SEL signal introduces a lower switching frequency into sub-converter, It is called SEL switching frequency, f_{SEL}. The maximum SEL switching frequency is half of the main switching frequency, $f_s/2$, as Fig. 5.3(a). As the difference between the two load current increasing, f_{SEL} will decrease. In Fig. 5.3(b), $f_{SEL} = f_s/6$. In (c), $f_{SEL} = f_s/4 \sim f_s/5$.



(a) $I_{out1}/I_{out2} = 500mA/500mA$



(b) $I_{out1}/I_{out2} = 1A/200mA$



(c) $I_{out1}/I_{out2} = 300mA/1A$

Fig. 5.3 Relationship between SEL and load current

5.2.3 Compensator design

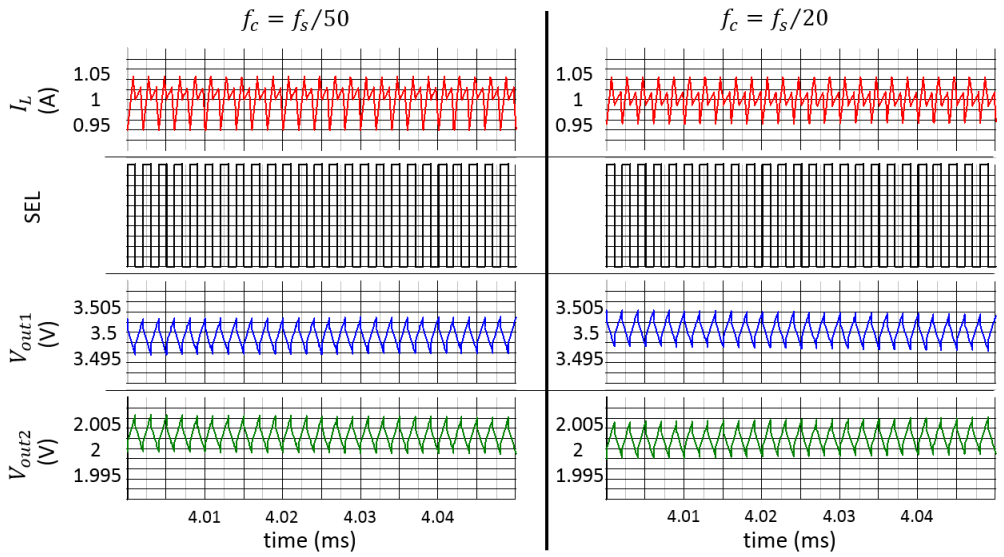
Similar to SISO VMC buck converter, Type 3 compensators can be designed for each sub-converter to follow the design procedure in Chapter 3. The difference is that the SIDO compensator design is limited by the possible low SEL switching frequency. Consider the sampling effect, the crossover frequency must be lower than $f_{SEL}/2$. It means that the bandwidth of SIDO buck converter is always lower than SISO converter which is limited by the GBP of op-amp.

Let us consider a SIDO buck converter with exclusive control. The parameters are listed in Table. 5.1. Type 3 compensators are designed to provide $f_s/20$ and $f_s/50$ bandwidth respectively. Supposing the maximum load current ratio between sub-converters is 10 (or $1/10$), the simulation results are shown in Fig. 5.4.

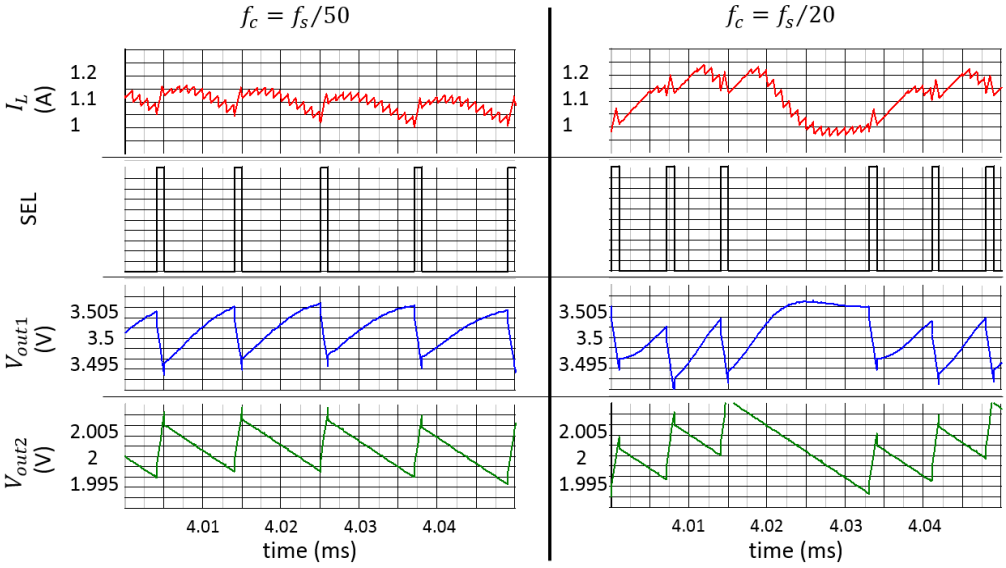
Table. 5.1 Parameters of SIDO buck converter with exclusive control

Common	Sub-converter 1	Sub-converter 2
$V_{in} = 5V$	$V_{out1} = 3.5V$	$V_{out2} = 2V$
$f_s = 1MHz$	$C_1 = 100\mu F$	$C_1 = 100\mu F$
$\mathrm{L} = 20\mu H$	$R_{ESR} = 2m\Omega$	$R_{ESR} = 2m\Omega$
$\mathrm{R}' = 50m\Omega$	$I_{out1} = 100mA \sim 1A$	$I_{out1} = 100mA \sim 1A$
	$V_D = 0.8V$	$R_{on\_Q2} = 2m\Omega$

If the load currents are the same, as Fig. 5.4(a), $f_{SEL} = f_s/2$, so that the maximum crossover frequency can be set at $f_c = f_s/4$. Therefore, either $f_s/50$ bandwidth or $f_s/20$ bandwidth, the system is stable. However, with the maximum load current ratio as Fig. 5.4(b), $f_{SEL} \approx f_s/11$, and then the crossover frequency is much lower than $f_s/22$. The consequence is that the $f_s/20$ bandwidth system is unstable, and an intricate fluctuation appears in the output voltage. While, if the bandwidth is low enough, for example $f_s/50$, the system is stable. But at the same time, we will have to endure the worse dynamic performance.



(a) $I_{out1}/I_{out2} = 500mA/500mA$



(b) $I_{out1}/I_{out2} = 1A/100mA$

Fig. 5.4 Simulation result of compensator design

5.3 CROSS-REGULATION IMPROVEMENT

5.3.1 Cross-regulation phenomenon

The cross-regulation phenomenon is common in SIDO and SIMO switching converters. It is the main drawback what causes SIDO and SIMO techniques have not been widely applied. The cross-regulation means that if the load current of one sub-converter is changed, not only this sub-converter occurs a load transient response, but also another sub-converter is affected. To distinguish the sub-converters, the load changed one is named as active sub-converter, the affected one is named as passive sub-converter.

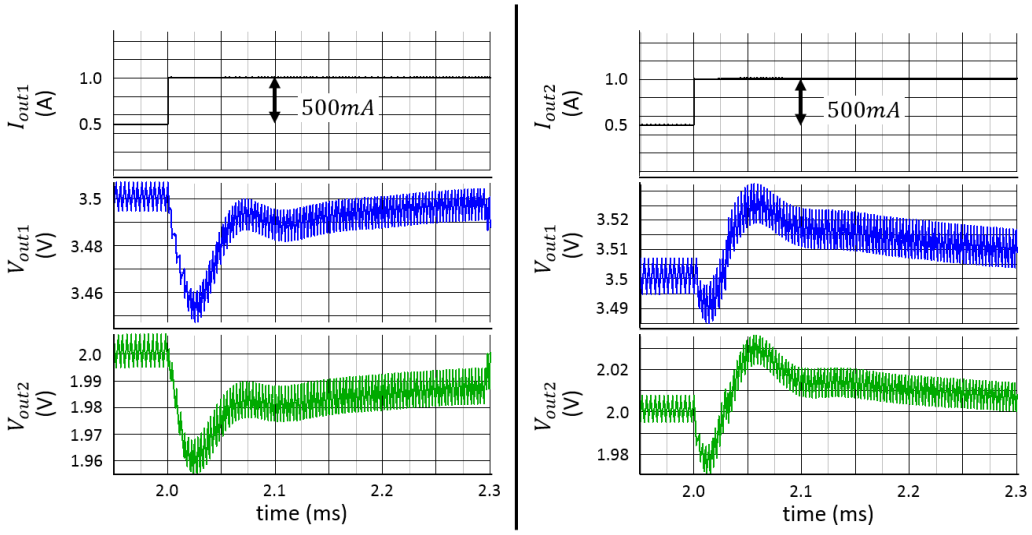


Fig. 5.5 Multifarious cross-regulation phenomenon

The cross-regulation phenomenon is multifarious. It is also possible that the passive sub-converter affects the active sub-converter in turn during the cross-regulation. Even if the same load current variations occur in different sub-converter, the fluctuations in the output voltage may be different. For example, as shown in Fig. 5.5, the sub-converter 1 is active in the left figure. The load current increase from 500mA to 1A, and two output voltages are both presented undershoot. While, in the right figure, the sub-converter 2 is active, and the load current also increases from 500mA to 1A. But two outputs are both presented overshoot after a short undershoot process. What kind of fluctuations depends

on the circuit configuration, the difference between two output voltages, the compensator, and so on.

5.3.2 SATWG for SIDO buck converter

So many factors are possible to affect the cross-regulation performance. We need a comprehensive and effective method to improve the cross-regulation, otherwise, even if we obtain improvement under certain conditions, but it may not be applicable to other conditions.

The proposed triangular wave slope modulation can be also applied in SIDO buck converter, and it is a simple-yet-effective solution for cross-regulation problem. It because that the triangular wave generator is only concerned with the variation in the input and output voltage. The variations are detected, and then the slope is regulated accordingly, without having to consider more details. When the variation is large, the additional modulation effect is strong. We just need to make sure that when the output deviation becomes small, the triangular wave timely return to steady state.

The SIDO buck converter with the slope adjustable TWG is shown in Fig. 5.6. Similar to the application in SISO buck converter, the additional op-amps sense and amplify the deviations of output voltage, and the outputs of op-amp, V_{con1} and V_{con2}, work as control variable for the triangular wave generator. Finally, the fix triangular wave is replaced by the slope adjustable triangular wave.

Since the SEL switching frequency, the load transient response of sub-converters are both poor, they require to be improved at the same time. In addition, because the sub-converters are discontinuously served by the inductor, the ripple of output voltage are large; hence the ripple of control variables V_{con1} and V_{con2} are very large. But since V_{con1} and V_{con2} always inversely change, the average of V_{con1} and V_{con2} can be used to control the voltage controlled resistance in TWG. This ensures that the triangular wave is stable when the system is under steady state. After a simple modification in the voltage adder, as shown in Fig. 5.7, the triangular wave can be expressed as

$$V_{tri} = \frac{G_3}{C_C R_{CS} R_b K_n} \cdot V_g \cdot \left(\frac{2}{V_{con1} + V_{con2}} - \frac{1}{V_{con\_max}} \right) \cdot t \qquad (5.2)$$

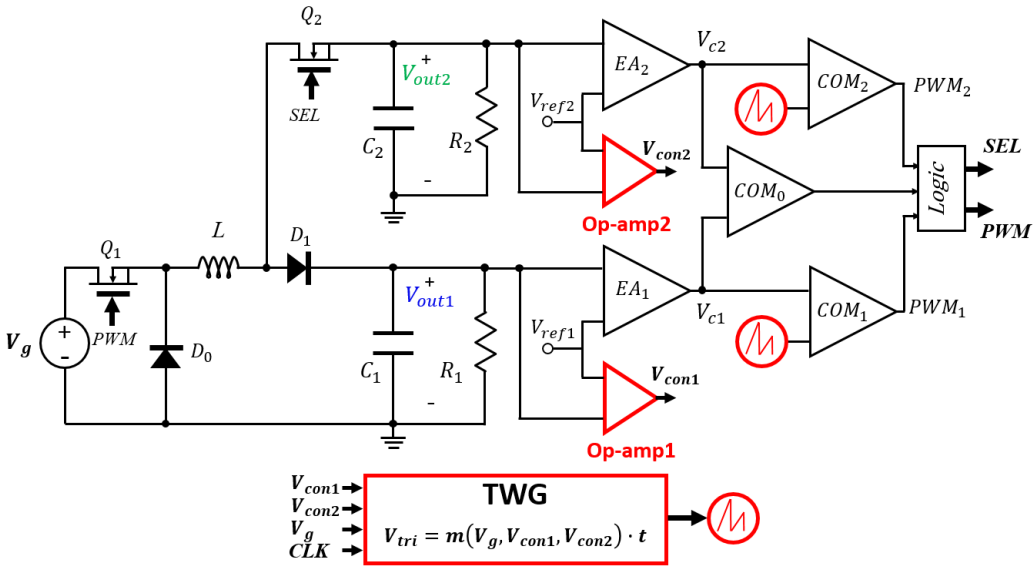
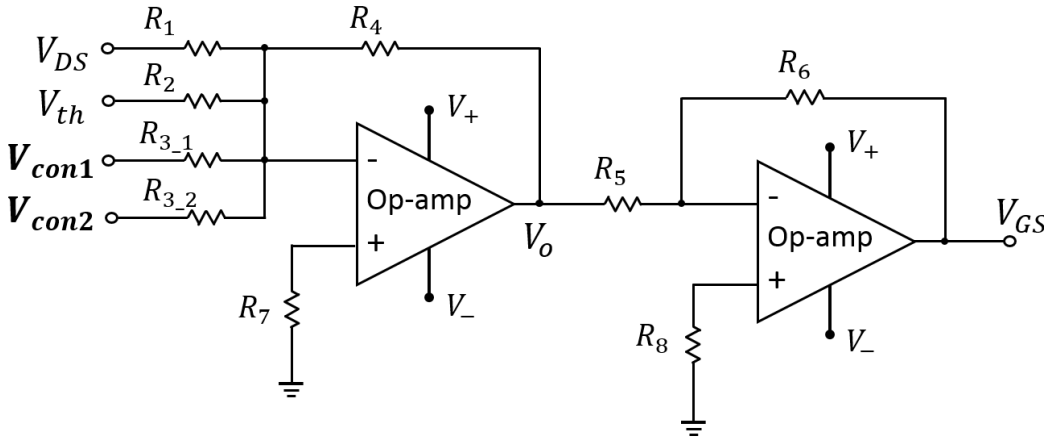


Fig. 5.6 SIDO buck converter with SATWG

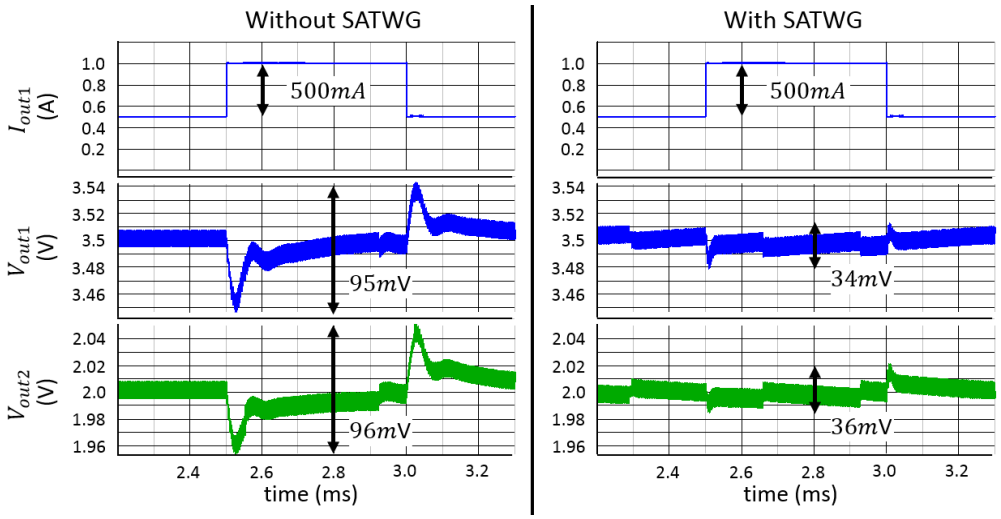


$$R_1 : R_2 : R_{3\_1} : R_{3\_2} : R_4 = 2 : 1 : 2 : 2 : 1$$

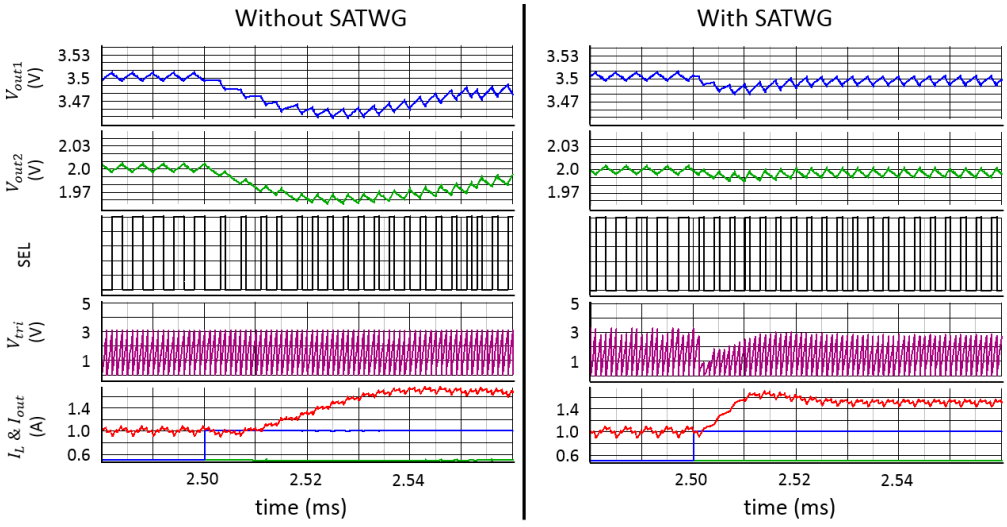
Fig. 5.7 Voltage adder modification for SIDO buck converter

5.3.3 Simulation result

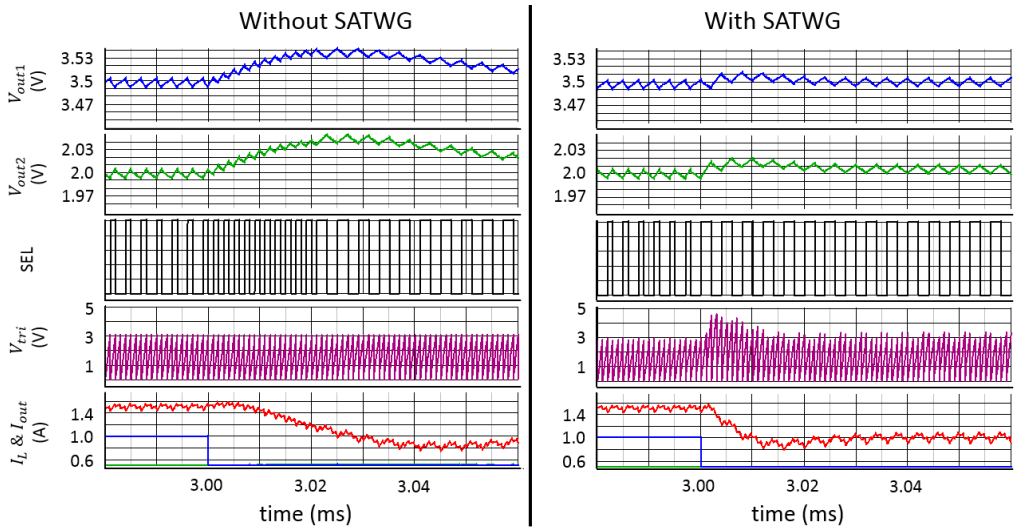
The parameters of SIDO buck converter will follow Table. 5.1. The compensators will provide $f_s/50$ bandwidth for each sub-converter. The triangular wave generator setting will follow Table 4.1, only the voltage adder and the phase compensation zero are modified correspondingly.



(a) Sub-converter 1 active, sub-converter 2 passive



(b) I_{out1}: $500mA \rightarrow 1A$; I_{out2}: $500mA$

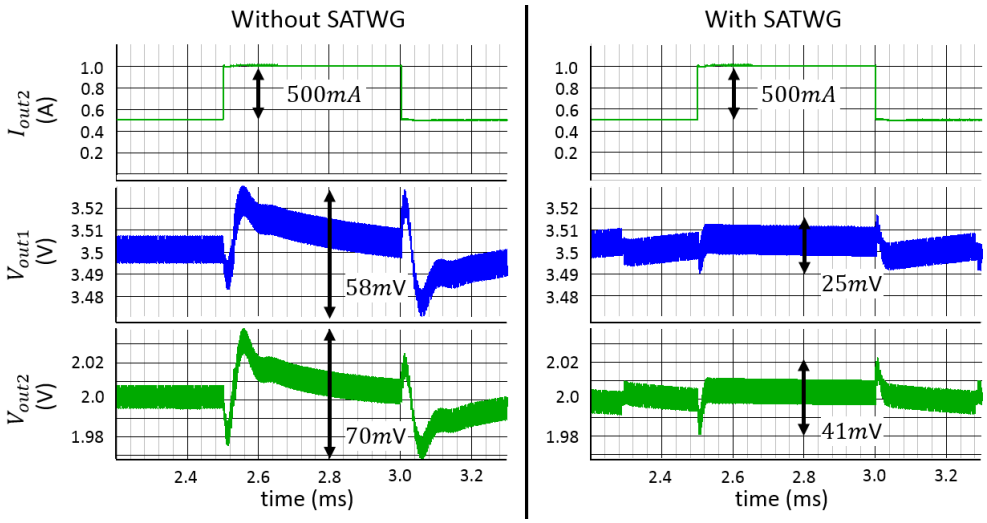


(c) I_{out1}: $1A \rightarrow 500\text{m}A$; I_{out2}: $500mA$

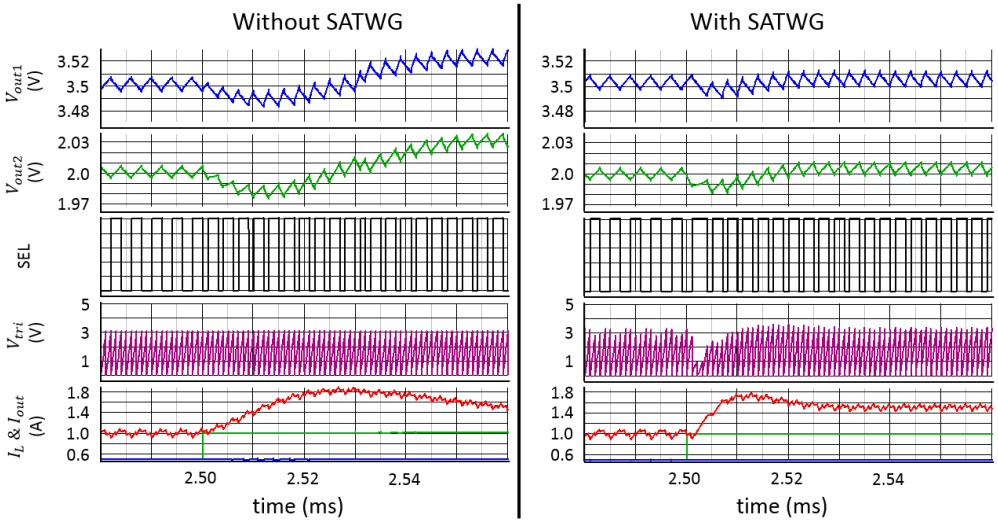
Fig. 5.8 Cross-regulation under I_{out1}: $500mA \leftrightarrow 1A$

First, consider the sub-converter 1 as the active sub-converter, and assume that its load current is stepwise changed between 500mA and 1A. Also, suppose that the load current of sub-converter 2 keeps at 500mA. The simulation result is shown in Fig. 5.8

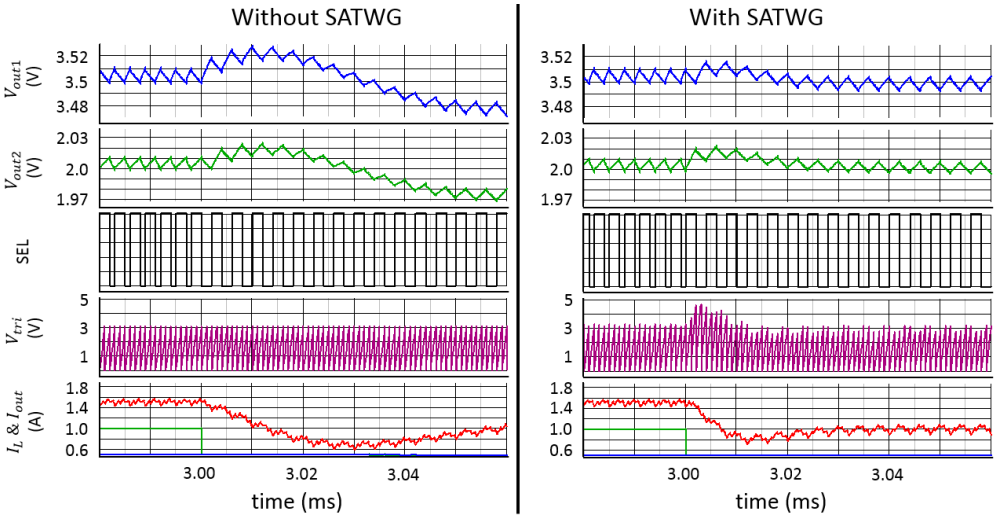
With the proposed triangular wave generator, the load transient response of sub-converter 1 is improved and the peak-to-peak voltage decreases from 95mA to 34mA. At the same time, the cross-regulation in the sub-converter 2 is also improved from 96mA to 36mA.



(a) Sub-converter 1 passive, sub-converter 2 active



(b) I_{out1}: 500mA; I_{out2}: 500m$A \rightarrow 1A$



(c) I_{out1}: 500mA; I_{out2}: $1A \rightarrow$ 500mA

Fig. 5.9 Cross-regulation under I_{out2}: $500mA \leftrightarrow 1A$

In the second simulation, consider sub-converter 2 as the active sub-converter, where its load current is stepwise changed between 500mA and 1A, and the load current of sub-converter 1 keeps at 500mA. The simulation result is shown in Fig. 5.9

The load transient response of active sub-converter and the cross-regulation of passive sub-converter both are improved by the proposed method.

CHAPTER VI
CONCLUSION

6.1 CONCLUSION

In order to improve the dynamic performance of dc-dc buck converter, I try to find out the relationship between transient response and the frequency characteristic, and then the theoretical compensator design method is introduced. However, whether it is voltage-mode control or current-mode control, the control method has its own drawbacks. Overall, voltage-mode control is simpler than current-mode control, but it is hard to get wide band since the limitation from the gain-bandwidth product of op-amp. In addition, not as current-mode control which has an inherent line feed-forward control. Line transient response of voltage-mode control is very slow.

I propose a novel control method for voltage-mode control buck converter. A slope adjustable triangular wave generator is designed. The triangular wave slope is related to the input voltage and the deviation of output voltage. This triangular wave not only provides a line feed-forward control function, but also provides an additional non-linear duty cycle modulation. Of course, line feed-forward control can improve the line transient response. While, the non-linear duty cycle modulation leads a large loop gain when the output voltage deviates largely from the reference signal. And when the output voltage returns and close to the reference signal, the loop gain non-linearly decreases to a constant. All of these mean fast response and stable system.

Then, SIMetrix simulations are used to prove the feasibility and effectiveness of the proposed control method. For line transient response, not only comparing to conventional VMC buck converter without line feed-forward control, but also comparing to the buck converter with line feed-forward control. Since the

proposed method can detect the variation in output voltage, the line transient response improvement is better than the previously proposed line feed-forward control which only considers the variation of input voltage. For load transient response, the proposed method can get comparable result with the wideband buck converter. However, the wideband buck converter requires a ultra wideband op-amp to design the compensator which can push the crossover frequency of loop gain to the highest possible frequency. But the proposed method only requires a normal op-amp for the compensator, and the crossover frequency does not need very high. And the proposed method is compared to hysteretic control. From the simulation result, we can see that they have comparable dynamic performance. The hysteretic control is simpler and a little faster than the proposed method, but the variable switching frequency of hysteretic control is still a problem, especially during the transient response.

Finally, the proposed control method is applied in single-inductor dual-output buck converter. SIDO technique is helpful for increasing efficiency and reducing system volume and chip area. The main drawback is the cross-regulation phenomenon. With the proposed control method, the cross-regulation is improved.

6.2 FUTURE WORK

In this research, I only do the system-level design and simulation by SIMetrix. In order to implement the slope adjustable triangular wave generator, I need to analyze and design the details on component-level, especially the voltage adder and the NMOS transistor that works as a voltage controlled resistance.

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Patent

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