学 位 論 文 の 要 旨

論文題目：ΔΣ ADC Linearity Testing Technology and
Floating-Point Arithmetic Algorithms with Taylor-Series Expansion

（和訳）ΔΣADC 線形性テスト技術とテイラー級数展開を用いた
浮動小数点演算アルゴリズム

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This dissertation consists of three parts, and all of the technical contents are related to the design and analysis of electronic circuits and systems for integrated circuit testing.

The first part deals with a high precision ΔΣ Digital-to-Analog Converter (DAC) technique for high-linearity signal generation. For ΔΣ DA conversion a limit cycle is generated for a small input signal, which causes the accuracy degradation during DA conversion. To overcome this problem, we propose a technique to add a random signal at one of the comparator inputs inside the modulator. In a conventional modulator, one input of the quantizer is grounded, but in our proposed method it is changed by adding a random signal. Then generation of limit cycles is suppressed there and the accuracy of DA conversion is improved. We have also compared the effects of adding random signals to the quantizer in different ranges to obtain the best range of input random signals. Another conventional method uses the dither signal addition at the ΔΣ DAC input, which may affect the signal component and cause the signal-to-noise ratio degradation as well as scarify the allowable input signal full-scale range; our proposed method can solve these problems. It is verified in system-level simulation that the proposed method is effective for low-pass, band-pass and multi-bandpass type ΔΣ DACs, used in electronic measuring equipment.

The second one describes a fast testing method for the integral nonlinearity (INL) of a high-resolution low-sampling-rate ΔΣ Analog-to-Digital Converter (ADC) targeted for reliable and low-cost IoT systems. The INL testing of the high-resolution low-sampling-rate ΔΣ ADC takes extraordinary long time if it is performed in a direct manner, so that it is usually omitted at the shipping stage of the ΔΣ ADC. However, due to the recent demands for high-reliability, the INL testing of the ΔΣ ADC in IoT systems are required, but it must be done in short time for low-cost.

We consider its INL testing by separating its analog and digital parts: ΔΣ AD modulator and digital filter. The digital filter part can be tested with a conventional scan-path method. Then we have focused on the ΔΣ AD modulator part. We consider a polynomial model of the ΔΣ AD modulator input-output characteristics and estimate its coefficient values. We apply a cosine wave as a modulator analog input, and performs Fast Fourier Transform (FFT) to the modulator 1-bit digital output steam. Then we can obtain its power spectrum of the fundamental and harmonics components. Then we can estimate the polynomial coefficients from these powers, and obtain its INL. This can be done in short time and hence the INL testing time can be drastically reduced, which leads to significant reduction of its mass production test cost.; with some reasonable assumption by the industry collaborator, the INL testing time can be reduced from 110 days (conventional method) to 32 seconds (proposed method). The effectiveness of the proposed method has been verified in simulations and experiments.

The third one discusses the study of hardware-efficient and fast arithmetic algorithms for floating-point numbers using Taylor series expansion, used for automatic test equipment as well as general digital signal processing systems. Our contributions are two-fold in the floating-point arithmetic algorithms using the Taylor-series; One is the clarification of the Taylor-series expansion calculation algorithm trade-offs among accuracy, numbers of multiplications/additions/subtractions and Look-Up Table (LUT) sizes, which leads to its systematic design. There are already the floating-point arithmetic algorithms using the Taylor-series, but their design trade-off was not clear. The other is the floating-point digital arithmetic algorithms to deal with division, inverse square root, logarithm and exponential calculation, using Taylor-series expansion with our three proposed methods: (i) mantissa region uniform division, (ii) mantissa region non-uniform division and (iii) mantissa region conversion. It is shown in simulation and theory that our proposed methods can reduce the required hardware, and again trade-offs among accuracy, numbers of multiplications/additions/subtractions and Look-Up Table (LUT) sizes are clarified in these cases.

It is believed that all of these three results can contribute to academia and industry in electronic circuits and systems area.